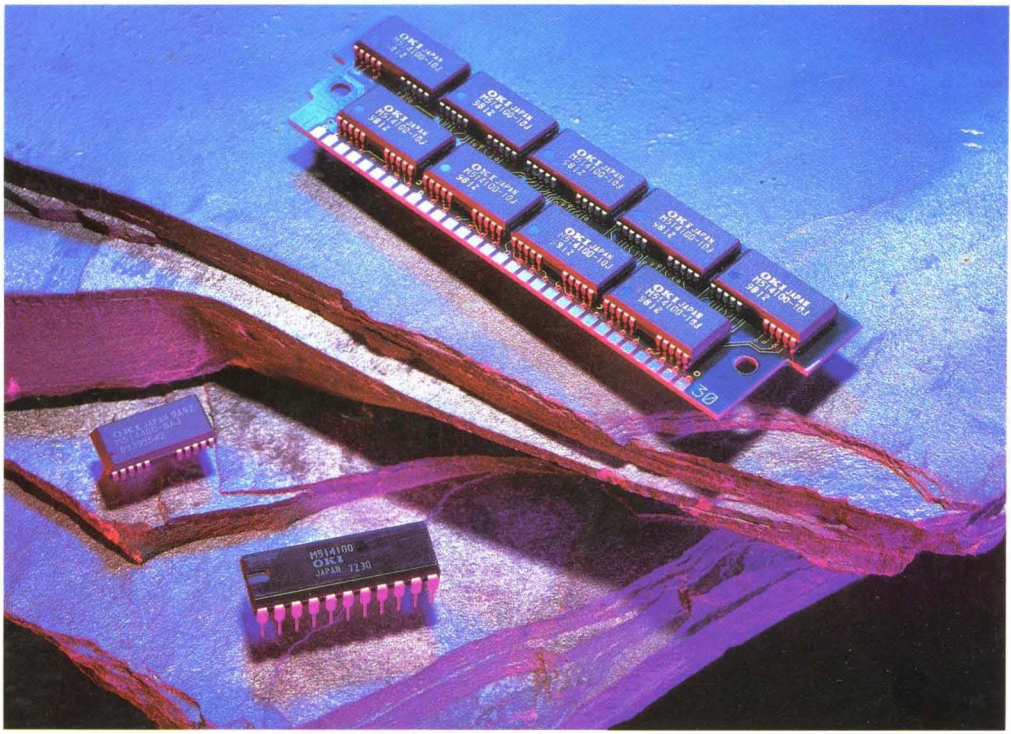
DATA BOOK

OKI

MEMORY



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MEMORY DATABOOK 1990/1991

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   MSM511002A
   MSM514256A
   MSM514258A
   MSM514100
   MSM514102
   MSM514400
   MSM514402

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   MSC2320A-XXYS9
   MSC2321A-XXYS18
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IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS

1

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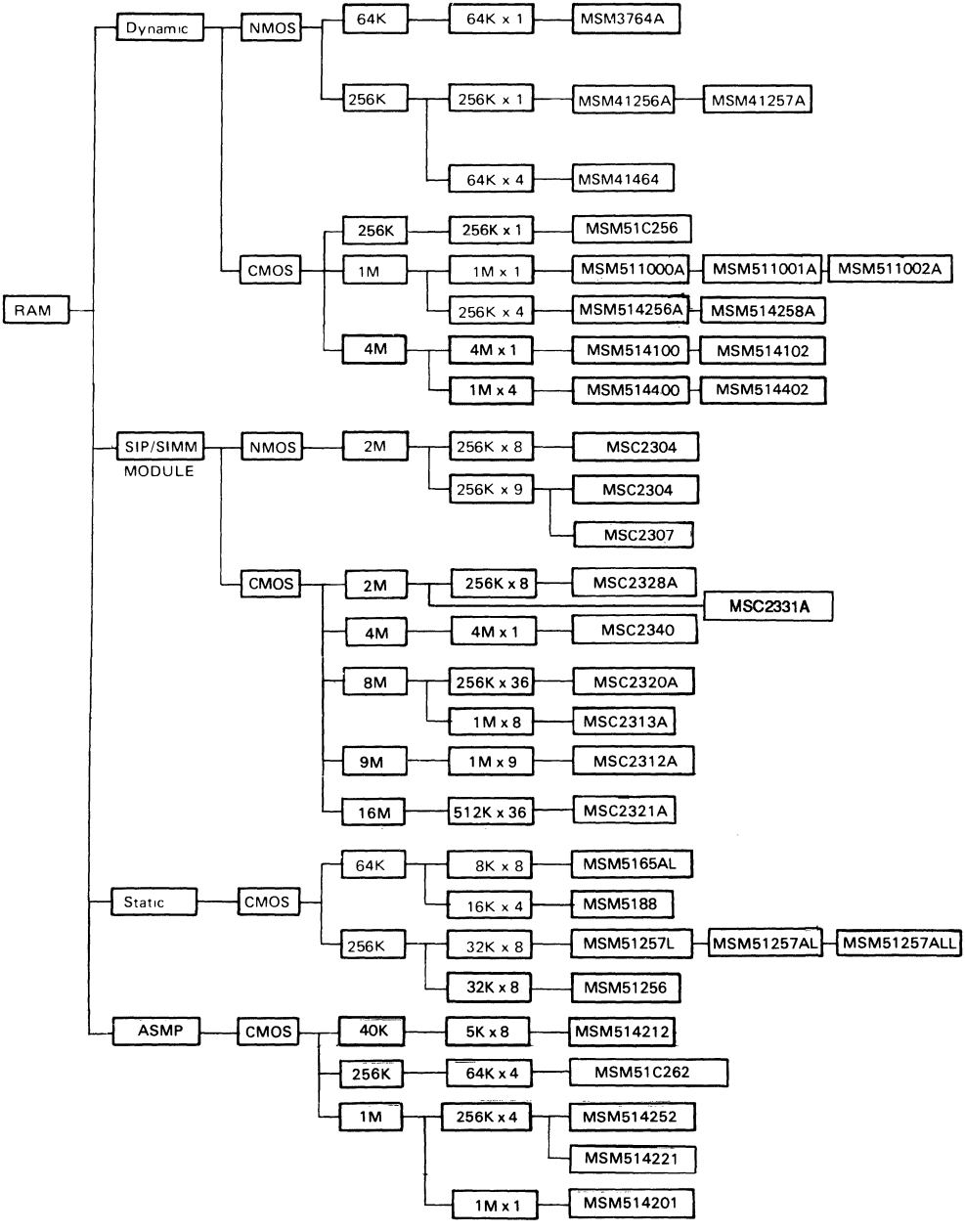
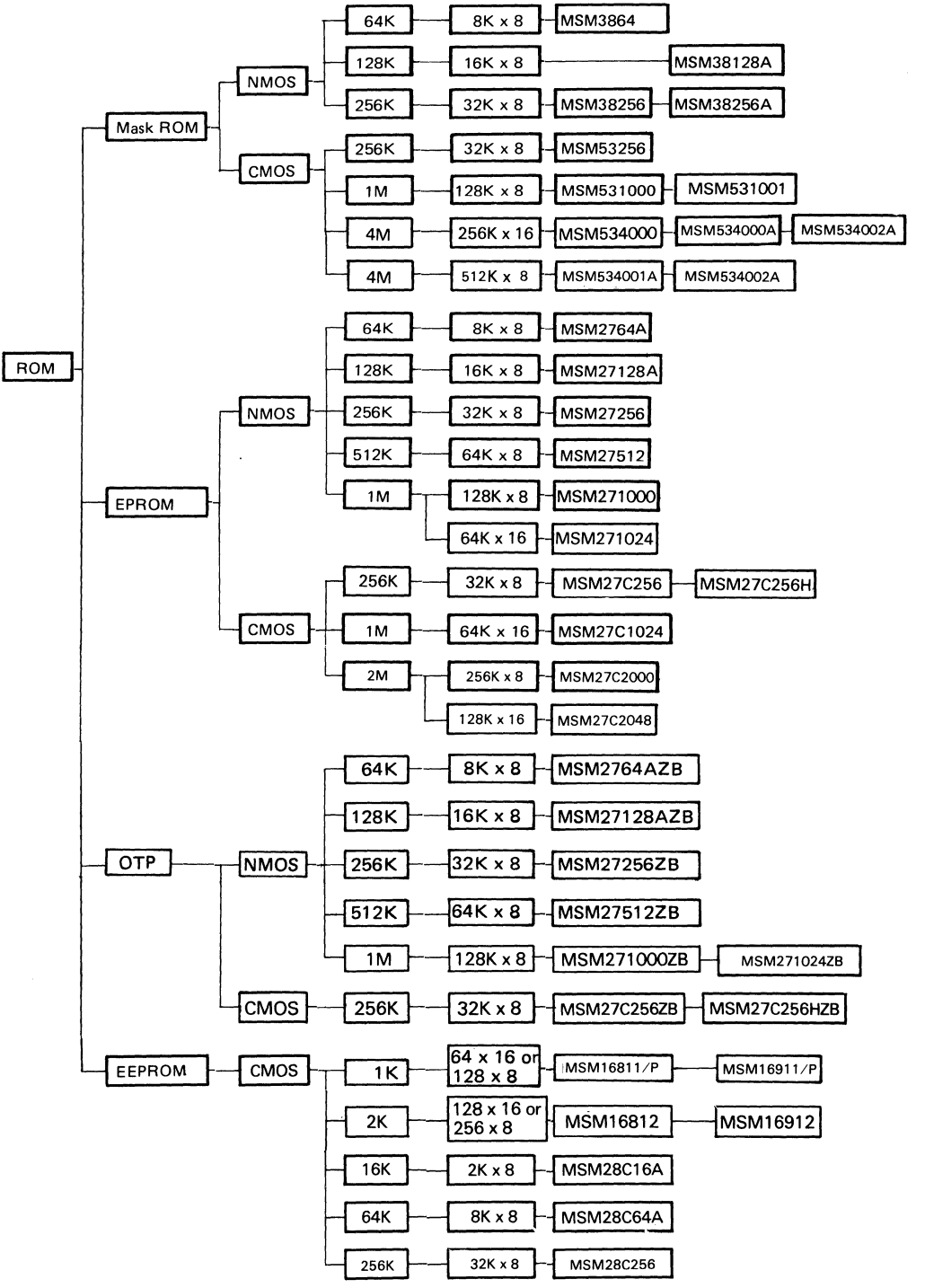
IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS



■ IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS ■



• DYNAMIC RAMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM3764A-12	64k	Dynamic	65,536x1	16	120	230	330/28	+5	
MSM3764A-15					150	260	303/28		
MSM41256A-10	256k	Dynamic	262,144x1	16	100	200	303/28	+5	
MSM41256A-12					120	220	275/28		
MSM41256A-15					150	260	248/28		
MSM41257A-10	256k	Dynamic	262,144x1	16	100	200	330/28	+5	
MSM41257A-12					120	220	303/28		
MSM41257A-15					150	260	275/28		
MSM41464-10	256k	Dynamic	65,536x4	18	100	200	385/28	+5	
MSM41464-12					120	230	358/28		
MSM41464-15					150	260	330/28		
MSM51C256-80	256k	Dynamic	262,144x1	16	80	145	330/20	+5	
MSM51C256-10					100	175	275/20		
MSM51C256-12					120	205	248/20		
MSM511000A-70	1M	Dynamic	1,048,576x1	18	70	140	468/5.5	+5	
MSM511000A-80					80	160	413/5.5		
MSM511000A-10				26	100	190	358/5.5		
MSM511000A-8A				20	80	160	413/5.5		
MSM511000A-1A					100	190	358/5.5		
MSM511001A-70	1M	Dynamic	1,048,576x1	18	70	140	468/5.5	+5	
MSM511001A-80					80	160	413/5.5		
MSM511001A-10				26	100	190	358/5.5		
MSM511001A-8A				20	80	160	413/5.5		
MSM511001A-1A					100	190	358/5.5		
MSM511002A-70	1M	Dynamic	1,048,576x1	18	70	140	468/5.5	+5	
MSM511002A-80					80	160	413/5.5		
MSM511002A-10				26	100	190	358/5.5		
MSM511002A-8A				20	80	160	413/5.5		
MSM511002A-1A					100	190	358/5.5		
MSM514256A-70	1M	Dynamic	262,144x4	20	70	140	468/5.5	+5	
MSM514256A-80					80	160	413/5.5		
MSM514256A-10					100	190	358/5.5		
MSM514256A-8A				26	80	160	413/5.5		
MSM514256A-1A					100	190	358/5.5		

■ IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS ■

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM514258A-70	1M	Dynamic	262,144x4	20	70	140	468/5.5	+5	
MSM514258A-80					80	160	413/5.5		
MSM514258A-10				26	100	190	358/5.5		
MSM514258A-8A				20	80	160	413/5.5		
MSM514258A-1A					100	190	358/5.5		
MSM514100-80	4M	Dynamic	4,194,304x1	18	80	160	495/5.5	+5	
MSM514100-8A				26	80	160	495/5.5		
MSM514100-10				20	100	190	440/5.5		
MSM514102-80	4M	Dynamic	4,194,304x1	18	80	160	495/5.5	+5	
MSM514102-8A				26	80	160	495/5.5		
MSM514102-10				20	100	190	440/5.5		
MSM514400-80	4M	Dynamic	1,048,576x4	20	80	160	495/5.5	+5	
MSM514400-8A				26	80	160	495/5.5		
MSM514400-10				20	100	190	440/5.5		
MSM514402-80	4M	Dynamic	1,048,576x4	20	80	160	495/5.5	+5	
MSM514402-8A				26	80	160	495/5.5		
MSM514402-10				20	100	190	440/5.5		

• SIP/SIMM MODULE

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSC2304-10 YS8/KS8	2M	Socket Insertable Module	262,144x8	30	100	200	2640/220	+5	
MSC2304-12 YS8/KS8					120	220	2420/220		
MSC2304-15 YS8/KS8					150	260	2200/220		
MSC2304-10 YS9/KS9	2M	Socket Insertable Module	262,144x8	30	100	200	2970/248	+5	
MSC2304-12 YS9/KS9					120	220	2723/248		
MSC2304-15 YS9/KS9					150	260	2475/248		
MSC2307-10 YS9/KS9	2M	Socket Insertable Module	262,144x8	30	100	200	2970/248	+5	
MSC2307-12 YS9/KS9					120	220	2723/248		
MSC2307-15 YS9/KS9					150	260	2475/248		
MSC2312A-80	9M	Socket Insertable Module	1,048,576x9	30	80	160	3713/49.5	+5	
MSC2312A-10					100	190	3218/49.5		
MSC2312A-8A					80	160	3713/49.5		
MSC2312A-1A					100	190	3218/49.5		
MSC2313A-80	8M	Socket Insertable Module	1,048,576x8	30	80	160	3300/44.0	+5	
MSC2313A-10					100	190	2860/44		
MSC2313A-8A					80	160	3300/44		
MSC2313A-1A					100	190	2860/44		
MSC2320A-80	8M	Socket Insertable Module	262,144x36	72	80	160	4410/99	+5	
MSC2320A-10					100	190	3780/99		
MSC2320A-8A					80	160	4410/99		
MSC2320A-1A					100	190	3780/99		
MSC2321A-80	16M	Socket Insertable Module	524,288x36	72	80	160	4568/198	+5	
MSC2321A-10					100	190	3938/198		
MSC2321A-8A					80	160	4568/198		
MSC2321A-1A					100	190	3938/198		
MSC2328A-80	2M	Socket Insertable Module	262,144x8	30	80	160	825/198	+5	
MSC2328A-10					100	190	715/198		
MSC2328A-8A					80	160	825/198		
MSC2328A-1A					100	190	715/198		
MSC2340-80 YS9/KS9	4M	Socket Insertable Module	4,194,304x9	30	80	160	4455/49.5	+5	
MSC2340-8A YS9/KS9					80	160	4455/49.5		
MSC2340-10 YS9/KS9					100	190	3960/49.5		

■ IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS ■

• CMOS STATIC RAMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM5165AL-10	64k	Fully Static Common I/O	8,192x8	28	100	100	230/0.55	+5	
MSM5165AL-12					120	120	303/0.55		
MSM5165AL-15					150	150	375/0.55		
MSM5188-45	64k	Fully Static Common I/O	16,384x4	22	45	45	605/11	+5	
MSM5188-55					55	55	605/11		
MSM5188-70					70	70	605/11		
MSM51257L-85	256k	Fully Static Common I/O	32,768x8	28	85	85	440/0.55	+5	
MSM51257L-100					100	100	385/0.55		
MSM51257L-120					120	120	385/0.55		
MSM51257AL-85	256k	Fully Static Common I/O	32,768x8	28	85	85	440/0.55	+5	
MSM51257AL-100					100	100	385/0.55		
MSM51257AL-120					120	120	385/0.55		
MSM51257ALL-85	256k	Fully Static Common I/O	32,768x8	28	85	85	440/0.11	+5	
MSM51257ALL-100					100	100	385/0.11		
MSM51257ALL-120					120	120	385/0.11		
MSM51256-10	256k	Fully Static Common I/O	32,768x8	28	100	100	385/0.0055	+5	
MSM51256-120					120	120	385/0.0055		

• MASK ROMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM3864	64k	Fully Static	8,192x8	28	250	250	550/165	+5	
MSM38128A	128k	Fully Static	16,384x8	28	250	250	550/165	+5	
MSM38256	256k	Fully Static	32,768x8	28	250	250	660/165	+5	
MSM38256A	256k	Fully Static	32,768x8	28	150	150	330/33	+5	
MSM53256	256k	Fully Static	32,768x8	28	150	150	83/0.55	+5	
MSM531000	1M	Fully Static	131,072x8	28	250	250	83/0.55	+5	
MSM531001	1M	Fully Static	131,072x8	32	120	120	110/0.28	+5	
MSM534000	4M	Fully Static	262,144x16	40	200	200	275/0.55	+5	
MSM534000A	4M	Fully Static	262,144x16	40	150	150	274/0.28	+5	
MSM534001A	4M	Fully Static	524,288x8	32	150	150	275/0.28	+5	
MSM534002A	4M	Fully Static	262,144x16	40	150	150	275/0.28	+5	

• EPROMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM2764A	64k	EPROM	8,192x8	28	120	120	525/184	+5	276A
MSM27128A	128k	EPROM	16,384x8	28	120	120	525/184	+5	27128A
MSM27256	256k	EPROM	32,768x8	28	150	150	525/184	+5	27256
MSM27512	512k	EPROM	65,536x8	28	150	150	525/184	+5	27512
MSM271000	1M	EPROM	131,072x8	32	120	120	525/184	+5	27010
MSM271024	1M	EPROM	65,536x16	40	120	120	630/184	+5	27210
MSM27C256	256k	EPROM	32,768x8	28	100	100	165/0.55	+5	27C256
MSM27C256H	256K	EPROM	32,768x8	28	55	55	525/184	+5	27HC256
MSM27C1024	1M	EPROM	65,536x16	40	100	100	175/0.55	+5	27C210
MSM27C2000-10	2M	EPROMS	262,144x8	32	100	100	385/28	+5	27C020
MSM27C2000-12					120	120	385/28		
MSM27C2000-15					150	150	385/28		
MSM27C2048-10	2M	EPROMS	131,072x6	40	100	100	550/28	+5	27C220
MSM27C2048-12					120	120	550/28		
MSM27C2048-15					150	150	550/28		
MSM2764AZB	64k	EPROMS	8,192x8	28	150	150	525/184	+5	P2764A
MSM27128AZB	128k	EPROMS	16,984x8	28	150	150	525/184	+5	P27128A
MSM27256	256k	EPROMS	32,768x8	28	170	170	525/184	+5	P27256A
MSM27512ZB	512k	EPROMS	65,536x8	28	200	200	525/184	+5	P27512
					150	150	525/184		
MSM271000ZB	1M	EPROMS	131,072x8	32	150	150	525/184	+5	P27010
MSM271024ZB	1M	EPROMS	65,536x16	40	170	170	630x184	+5	P27210
MSM27C256HZB	256k	EPROMS	32,768x8	28	70	70	525x184	+5	

■ IC MEMORY LINE-UP AND TYPICAL CHARACTERISTICS ■

• E²PROMS

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM16811	1k	E²PROM	64x16 or 128x8	8	*250	**1.0	16.5/0.55	+5	CAT93C46
MSM16811P	1k	E²PROM	64x16 or 128x8	8	*250	**1.0	16.5/0.55	+5	CAT93C46I
MSM16911	1k	E²PROM	64x16 or 128x8	8	*250	**1.0	16.5/0.55	+5	CAT59C11
MSM16911P	1k	E²PROM	64x16 or 128x8	8	*250	**1.0	16.5/0.55	+5	CAT59C11I
MSM16812	2k	E²PROM	128x16 or 256x8	8	*1000	**0.25	16.5/0.55	+5	CAT35C102
MSM16912	2k	E²PROM	128x16 or 256x8	8	*1000	**0.25	16.5/0.55	+5	CAT35C202
MSM28C16A-15	16k	E²PROM	2,048x8	24	150	150	165/0.55	+5	X2816A
MSM28C16A-20					200	200	165/0.55		
MSM28C64A-15	64k	E²PROM	8,192x8	28	150	150	165/0.55	+5	X28C64A
MSM28C64A-20					200	200	165/0.55		
MSM28C256	256k	E²PROM	32x8	28	200	200	165/0.55	+5	

*: Clock Frequency MAX (kH)
**: Clock Pulse MIN (μs)

• ASMP

Model Name	Memory Capacity	Circuit Function	Memory Configuration	Number of Pins per Package	Access Time MAX (ns)	Cycle Time MIN (ns)	Power Consumption MAX (mw) Operating/ Standby	Power Supply Voltage (V)	Equivalent Device
MSM514212-28	40k	ASMP	5,048x8	28	28	28	600/28	+5	
MSM514212-34					34	34	600/28		
MSM514212-50					50	50	600/28		
MSM514221-3	1M	ASMP	262,263x4	16	25	30	275/28	+5	
MSM514221-6					30	60	275/28		
MSM514252-10	1M	ASMP	262,144x4	28	100	190	660/28	+5	
MSM514252-12					120	220	550/28		
MSM51C262-80	256k	ASMP	65,536x4	24	80	145	660/44	+5	
MSM51C262-10					100	175	550/44		
MSM51C262-12					120	205	468/44		
MSM514201	1M	ASMP	1,048,576x1	18	3000	4000	28/0.5	+4.5	

MOS MEMORY HANDLING PRECAUTIONS

1 MOS MEMORY HANDLING PRECAUTIONS

1. STATIC ELECTRICITY COUNTER-MEASURES

Since voltage is generally controlled by means of the transistor gate oxide film in MOS memories, the input impedance is high and the insulation tends to be destroyed more readily by static electricity.

Although Oki MOS memories incorporate built-in protector circuits to protect all input terminals from such destruction, it is not considered possible to give complete protection against heat destruction due to overcurrents and insulation film destruction due to irregular high voltages. It is, therefore, necessary to observe the following precautionary measures.

1) Under no circumstances must voltages or currents in excess of the specified ratings be applied to any input terminal.
2) Always use an electrically conductive mat or shipping tubes for storage and transporting purposes.
3) Avoid wearing apparel made of synthetic fiber during operations. The wearing of cottons which do not readily generate static electricity is desirable. Also avoid handling devices with bare hands. If handling with bare hands cannot be avoided, make sure that the body is grounded, and that a 1MΩ resistor is always connected between the body and ground in order to prevent the generation of static electricity.
4) Maintaining the relative humidity in the operation room at 50% helps to prevent static electricity. This should be remembered especially during dry seasons.
5) When using a soldering iron, the iron should be grounded from the tip. And as far as possible, use low power soldering irons (12 V or 24 V irons).

2. POWER SUPPLY AND INPUT SIGNAL NOISE

2.1 Power supply noise absorption

In dynamic memories, the flow of power supply current differs greatly between accessing and standby modes.

Although very little power is consumed by CMOS memories during standby mode, considerable current is drawn for charging and discharging (instantaneous current requirements) during access mode. In order to absorb the "spike noise" generated by these current requirements, the use of relatively large capacitance capacitors (about one 10μF capacitor for every 8 to 10 RAMs) is recommended along with good high frequency response capacitors of about 0.1μF for each memory element. Power line wiring with as little line impedance as possible is also desirable.

2.2 Input signal noise absorption

Overshooting and undershooting of the input signal should be kept to a bare minimum. Undershooting in particular can result in loss of cell data stability within the memory. For this reason,

(1) Avoid excessive undershooting when using an address common bus for memory board RAMs and ROMs.
(2) Since noise can be generated very easily when using direct drive for applying memory board RAM addresses from other driver boards, it is highly recommended that these addresses be first received by buffer.
(3) Methods available for eliminating undershooting generated in the address line include
   a) Clamping of the undershooting by including a diode.
   b) Connect 10~20Ω in series with driver outputs.
   c) Smooth the rising edge and falling edge waveforms.

3. CMOS MEMORY OPERATING PRECAUTIONS

3.1 Latch-Up

If the CMOS memory input signal level exceeds the Vcc power line voltage by +0.3 V, or drops below the ground potential by −0.3 V, the latch-up mechanism may be activated. And once this latch-up mode has been activated, the memory power has to be switched off before normal operating mode can be restored. Destruction of the memory element is also possible if the power is not switched off.

Although Oki CMOS memories have been designed to counter these tendencies, it is still recommended that input signal overshooting and undershooting by avoided.

3.2 Battery Back-Up

Take special note of the following 4 points when designing battery back-up systems.

(1) Do not permit the input signal H level to exceed Vcc +0.3 V when the memory Vcc power is dropped. To achieve this, it is recommended that a CMOS driver using a Vcc power common with the CMOS memory, or an open collector buffer or open drain buffer pulled-up by a Vcc power common with the CMOS memory be used for driving purposes.
(2) Set the chip select input signal CE to the same H level as the CMOS memory Vcc power line. And in order to minimize memory power consumption, set the write enable input $\overline{WE}$ level, the address input and the data input to either ground level or to the same H level as the CMOS memory Vcc power line.
(3) Make sure that the CMOS memory Vcc power line is increased without "ringing" or temporary breaks when restoring the battery back-up mode.
(4) When using synchronous type CMOS memories (MSM5115, MSM5104), make sure that accessing occurs after elapse of the chip enable off time (t_{CC}) prescribed in the catalog after the Vcc power line has reached the guaranteed operating voltage range.

For further details, refer to "CMOS Memory Battery Back-up" at the end of this manual.

MASK ROM CUSTOMER PROGRAM SPECIFICATIONS

1

MASK ROM CUSTOMER PROGRAM SPECIFICATIONS

The mask ROM custom program code programming method is outlined below.

1. USABLE MEDIA

(1) Magnetic tape
(2) EPROM

Magnetic tape and EPROM are used as standard.

2. MAGNETIC TAPE SPECIFICATIONS

2.1 Use the following types of magnetic tape in magnetic tape units compatible with IBM magnetic tape units.

(1) Length: 2400 feet, 1200 feet or 600 feet
(2) No label
(3) Width: 1/2 feet
(4) Channels: 9 channels
(5) Bit density: 800BPI standard, although 1600BPI can also be employed.
(6) Block size: Integer multiples of 256 bytes possible with 256 bytes as standard. 1 block, 1 record is standard.

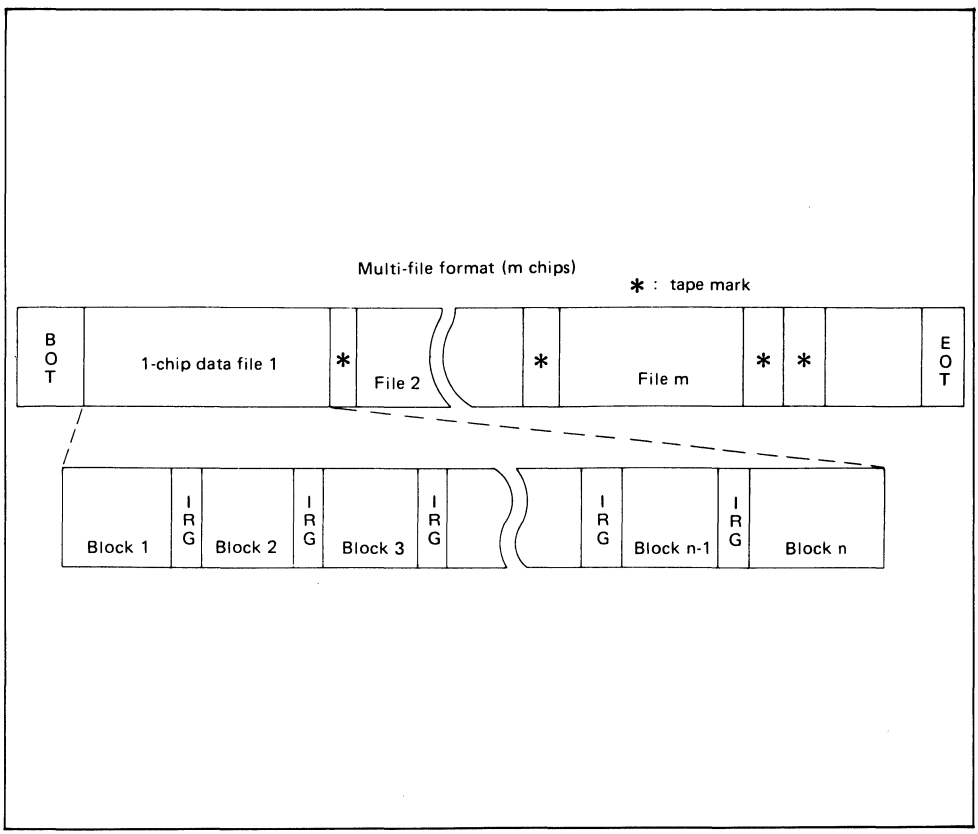
2.2 Magnetic tape format

(1) The data for a single chip should not extend into several tapes. Data for several chips are allowed to be included in a single magnetic tape, multiple file format being permitted. In this case, include the data of a single chip in one file.
(2) Use tape marks for file partitions when employing multiple file formats.
(3) Denote the completion of a magnetic tape file by two successive tape marks.

2.3 Magnetic tape data format

(1) The data contained in a single file on magnetic tape must be inserted from the head address $(0000)_{hex}$ of the device up to the final address in succession for a single chip.
(2) In this case, the LSB of the data should correspond to D_0, and the MSB to D_7.
(3) "1" bits in the data denote high device output, while "0" denotes low output.

2.4 Magnetic tape examples



3. EPROM SPECIFICATIONS

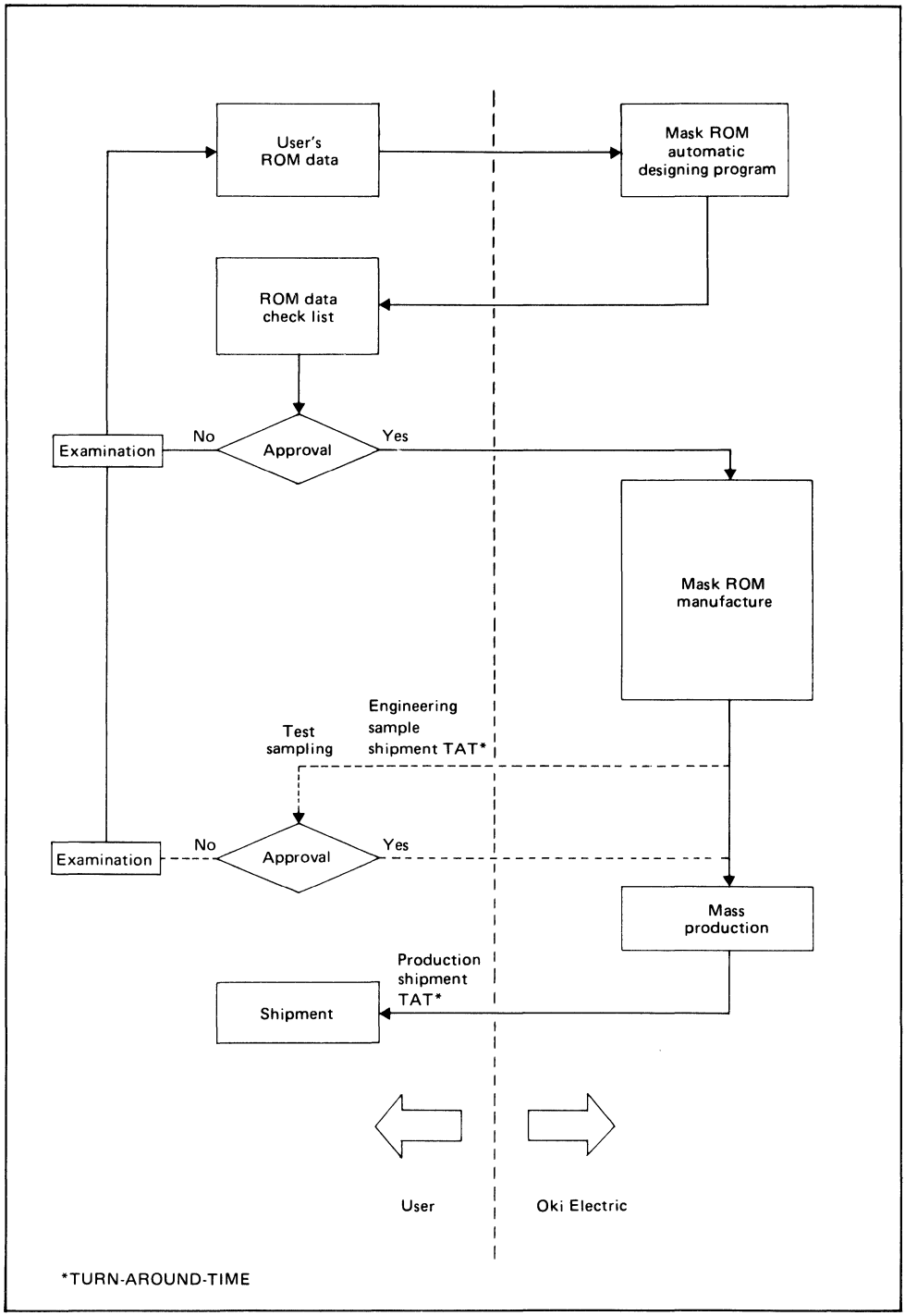
(1) MSM2764A, MSM27128A, MSM27256 or Intel 2764A, 27128A, 27256 equivalent device may be used.

(2) Prepare 2 EPROMs containing identical data.

MASK ROM DEVELOPMENT FLOWCHART

1

MASK ROM DEVELOPMENT FLOWCHART



*TURN-AROUND-TIME

1

TERMINOLOGY AND SYMBOLS

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TERMINOLOGY AND SYMBOLS

1. PIN TERMINOLOGY

Term	EPROM	Mask ROM	EEPROM	Static RAM	Dynamic RAM
Power Supply Voltage Pin	V_{CC}, V_{PP}	V_{CC}	V_{CC}	V_{CC}	V_{DD}, V_{CC}
Address Input Pin	$A_0 \sim A_{16}$	$A_0 \sim A_{17}$	$A_0 \sim A_{12}$	$A_0 \sim A_{14}$	$A_0 \sim A_{10}$
Data Input Pin				DI	DIN, D9
Data Output Pin	$O_0 \sim O_{15}$	$D_0 \sim D_{15}$		DO	D OUT, Q9
Data Input/Output Pin			I/O0 ~ I/O7	$I/O_1 \sim I/O_8$	$DO_1 \sim DQ_8$
Chip Enable Pin	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}_1$, CE_2	
Output Enable Pin	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
Address Enable Pin					
Chip Select Pin		$\overline{CS}$		$\overline{CS}$	
Write Enable Pin			$\overline{WE}$	$\overline{WE}$	$\overline{WE}$
Row Address Strobe Pin					$\overline{RAS}$
Column Address Strobe Pin					$\overline{CAS}$
Program Enable Pin	$\overline{PGM}$, V_{PP}				
Data Valid Pin					
Clock Input Pin					
Ground Pin	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
Vacant Terminal	NC	NC	NC		

2. ABSOLUTE MAXIMUM RATINGS

Term	EPROM	Mask ROM	EEPROM	Static RAM	Dynamic RAM
Power supply voltage	V_{CC}, V_{PP} V_{SS}	V_{CC} V_{SS}	V_{CC} V_{SS}	V_{CC} V_{SS}	V_{DD}, V_{CC} V_{SS}
Terminal voltage	V_T			V_T	V_T
Input voltage	V_I	V_I	V_I	V_I	V_I
Output voltage	V_O	V_O	$V_{\overline{O}}$	V_O	V_O
Input current					
Output current				I_O	
Output short circuit current					I_{OS}
Load capacitance					
Power dissipation	P_D	P_D	P_D	P_D	P_D
Operating temperature	Topr	Topr	T_{opr}	Topr	Topr
Storage temperature	Tstg	Tstg	T_{stg}	Tstg	Tstg

3. RECOMMENDED OPERATION CONDITIONS

Term	EPROM	Mask ROM	EEPROM	Static RAM	Dynamic RAM
Power Supply Voltage	V_{CC}, V_{PP} V_{SS}	V_{CC} V_{SS}	V_{CC} V_{SS}	V_{CC} V_{SS}	V_{DD}, V_{CC} V_{BB} V_{SS}
"H" Clock Input Voltage					V_{IHC}
"H" Input Voltage	V_{IH}	V_{IH}	V_{IH}	V_{IH}	V_{IH}
"L" Input Voltage	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}
Data Retention Voltage				V_{CCH}	
Load Capacitance	C_L	C_L	C_L	C_L	
Fan-out		N	N	N	
Operating Temperature	Topr	Topr	T_{opr}	Topr	Topr

4. DC CHARACTERISTICS

Term	EPROM	Mask ROM	EEPROM	Static RAM	Dynamic RAM
"H" output voltage	V_{OH}	V_{OH}	V_{OH}	V_{OH}	V_{OH}
"L" output voltage	V_{OL}	V_{OL}	V_{OL}	V_{OL}	V_{OL}
"H" output current	I_{OH}	I_{OH}	I_{OH}	I_{OH}	I_{OH}
"L" output current	I_{OL}	I_{OL}	I_{OL}	I_{OL}	I_{OL}
Input leakage current	I_{LI}	I_{LI}	I_{LI}	I_{LI}	I_{LI}
Output leakage current	I_{LO}	I_{LO}	I_{LO}	I_{LO}	I_{LO}
I/O leak current				I_{LO}	
Program terminal current	I_{PP1}, I_{PP2}				
Peak power on current		I_{PO}			
Power supply current	I_{CC}, I_{CC1}, I_{CC2}	I_{CCA}, I_{CCS} I_{CCS1}	I_{CCA}, I_{CCS}, I_{CCS1}	I_{CCS}, I_{CCS1} I_{CCA}	I_{DD1}, I_{CC1}, I_{BB1} I_{DD2}, I_{CC2}, I_{BB2} I_{DD3}, I_{CC3}, I_{BB3} I_{DD4}, I_{CC4}, I_{BB4}

5. AC CHARACTERISTICS

(1) Read cycle

Term	EPROM	Mask ROM	EEPROM	Static RAM	Dynamic RAM
Read cycle time		t_C	t_{RC}	t_{RC}	t_{RC}
Address access time	t_{ACC}	t_{AA}	t_{AA}	t_{AC}	t_{AA}
Chip select access time		t_{CS}		t_{CO}	
Chip enable access time	t_{CE}	t_{ACE}	t_{CE}	t_{CD}	
Output enable access time	t_{OE}	t_{CO}	t_{OE}	t_{OE}	t_{OEA}
Output setting time		t_{LZ}	t_{LZ}, t_{OLZ}	t_{CX}, t_{OX}	
Output valid time		t_{OH}	t_{OH}	t_{OHA}	
Output disable time	t_{DF}	t_{HZ}	t_{HZ}, t_{OHZ}	t_{OTD}, t_{CTD}	t_{OFF}, t_{OEZ}
Address set-up time				t_{AS}	t_{ASR}, t_{ASC}
Address hold time					t_{RAH}, t_{CAH}
Chip enable off time					
Chip enable pulse width					
Power-up time		t_{PU}			
Power-down time		t_{PD}			
Address enable pulse width					
Data valid access time					
Data valid delay time					
Clock delay time					
Clock pule width					t_{RAS}, t_{CAS}, t_{WP}
Clock delay time					t_{RCD}, t_{RAD}
Output delay time					
Output access time					
Output hold time					
Address enable set-up time					

(2) Write Cycle

Term	EPROM	EEPROM	Static RAM	Dynamic RAM
Write cycle time		t_{WC}	t_{WC}	t_{RC}
Address set-up time	t_{AS}	t_{AS}	t_{AS}	t_{ASR}, t_{ASC}
Write pulse width	t_{PW}, t_{OPW}	t_{WP}, t_{CW}	t_{W}	t_{WP}
Write recovery time			t_{WR}	
Data set-up time	t_{DS}	t_{DS}	t_{DS}	t_{DS}
Data hold time	t_{DH}	t_{DH}	t_{DH}	t_{DH}
Output off-time	t_{DFP}		t_{OTW}	t_{OFF}
Address hold time	t_{AH}	t_{AH}		t_{RAH}, t_{CAH}
Chip enable off time				
Chip enable pulse width			t_{CW}	
Write enable set-up time		t_{CS}		
Write enable read time				
Write enable hold time		t_{CH}		
Address/write enable setting time				
Write enable output activation				
$\overline{CE}$ set-up time	t_{CES}	t_{CS}		
$\overline{OE}$ set-up time	t_{OES}	t_{OES}		
Data valid from $\overline{OE}$	t_{OE}			
V_{PP} power set up time	t_{VS}			
Output enable hold time		t_{OEH}		
Data latch time		t_{DL}		
Data load time		t_{PL}		

PACKAGING 1

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- 30 PIN SIMP (FOR MSC2312AKS9) 49
- 30 PIN SIMM (FOR MSC2313AYS8) 50
- 30 PIN SIMP (FOR MSC2313AKS8) 50

PACKAGING

Name	PACKAGES					
	RS	GS	JS	ZS	AS	KS/YS
	PLASTIC DIP/PLASTIC SKINNY DIP	PLASTIC SOP/ PLASTIC QFP	QFJ (PLCC)/ PLASTIC SOJ	PLASTIC DIP	CERDIP	MODULE
MSM3764A	DIP16-P-300	–	QFJ18-P-R290	–	–	–
MSM41256A	DIP16-P-300	–	QFJ18-P-R290	–	–	–
MSM41257A	DIP16-P-300	–	QFJ18-P-R290	–	–	–
MSM41464	DIP18-P-300	–	"	–	–	–
MSM51C256	DIP16-P-300	–	"	–	–	–
MSM511000A	DIP18-P-300-W1	–	SOJ26-P-300	ZIP20-P-400	–	–
MSM511001A						
MSM511002A						
MSM514256A	DIP20-P-300-W1	–	SOJ26-P-300	ZIP20-P-400	–	–
MSM514258A						
MSM514100	DIP18-P-400	–	SOJ26-P-350	ZIP20-P-400-W1	–	–
MSM514102						
MSM514400	DIP20-P-400	–	SOJ26-P-350	ZIP20-P-400-W1	–	–
MSM514402						
MSC2304(8)	–	–	–	–	–	30 PIN SIMM/SIMP
MSC2304(9)	–	–	–	–	–	30 PIN SIMM/SIMP
MSC2307(9)						
MSC2312A(9)	–	–	–	–	–	30 PIN SIMM/SIMP
MSC2313A(8)						
MSC2320A(9)	–	–	–	–	–	72 PIN SIMM
MSC2321A(18)						
MSC2328A(2)	–	–	–	–	–	30 PIN SIMM/SIMP
MSC2340(9)	–	–	–	–	–	30 PIN SIMM/SIMP
MSM5165AL	DIP28-P-600	SOP28-P-430-K	–	–	–	–
MSM5188	DIP22-P-300-S1	–	–	–	–	–

2

Name	PACKAGES					
	RS	GS	JS	ZS	AS	KS/YS
	PLASTIC DIP/PLASTIC SKINNY DIP	PLASTIC SOP/ PLASTIC QFP	QFJ (PLCC)/ PLASTIC SOJ	PLASTIC DIP	CERDIP	MODULE
MSM51257L	DIP28-P-600	SOP28-P-430-K	–	–	–	–
MSM51257AL						
MSM51257ALL						
MSM51256						
MSM3864	DIP28-P-600	–	–	–	–	–
MSM38128A						
MSM38256						
MSM38256A						
MSM53256	DIP28-P-600	–	–	–	–	–
MSM531000	DIP28-P-600	QFP60-P-1519-VK	–	–	–	–
MSM531001	DIP32-P-600	–	–	–	–	–
MSM534000	DIP40-P-600	–	–	–	–	–
MSM534000A						
MSM534001A	DIP32-P-600					
MSM534002A	DIP40-P-600					
MSM2764A	–	–	–	–	WDIP28-G-600	–
MSM27128A						
MSM27256						
MSM27512						
MSM271000	–	–	–	–	WDIP32-G-600	–
MSM271024	–	–	–	–	WDIP40-G-600	–
MSM27C256	DIP28-P-600	–	–	–	WDIP28-G-600	–
MSM27C256H						
MSM27C1024	–	–	–	–	WDIP40-G-600	–
MSM27C2000	–	–	–	–	WDIP32-G-600	–
MSM27C2048	–	–	–	–	WDIP40-G-600	–
MSM2764AZB	DIP28-P-600	–	–	–	–	–
MSM27128AZB						
MSM27256ZB						
MSM27512ZB						

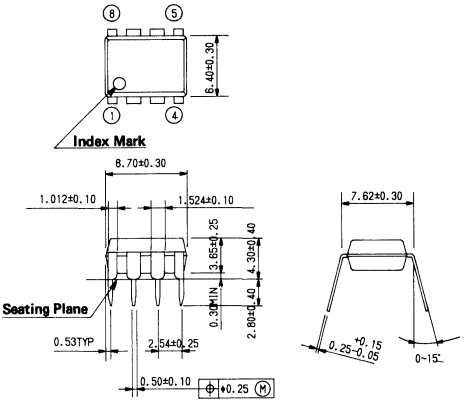
Name	PACKAGES					
	RS	GS	JS	ZS	AS	KS/YS
	PLASTIC DIP/PLASTIC SKINNY DIP	PLASTIC SOP/ PLASTIC QFP	QFJ (PLCC)/ PLASTIC SOJ	PLASTIC DIP	CERDIP	MODULE
MSM271000ZB	DIP32-P-600	–	–	–	–	–
MSM271024ZB	DIP40-P-600	–	–	–	–	–
MSM27C256ZB	DIP28-P-600	–	–	–	–	–
MSM27C256 HZB						
MSM16811	DIP8-P-300	SOP8-P-250-K	–	–	–	–
MSM16811P						
MSM16911						
MSM16911P						
MSM16812	DIP8-P-300	8 PIN PLASTIC SOP *	–	–	–	–
MSM16912						
MSM28C16A	DIP24-P-600	–	–	–	–	–
MSM28C64A	DIP28-P-600	SOP28-P-430-K	–	–	–	–
MM28C256	DIP28-P-600	–	–	–	–	–
MSM514212	–	–	–	ZIP28-P-400	–	–
MSM514221	DIP16-P-300-W1	–	SOJ26-P-300	ZIP20-P-400	–	–
MSM514252	–	–	–	ZIP28-P-400	–	–
MSM51C262	–	–	–	24 PIN * PLASTIC ZIP	–	–
MSM514201	–	–	QFJ18-P-R290	–	–	–

PLASTIC DIP

2

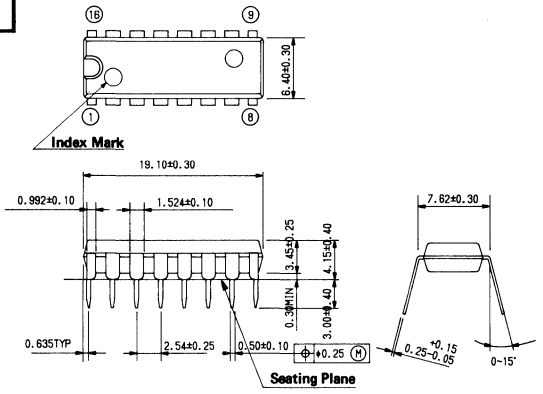
8 PIN PLASTIC DIP

DIP18-P-300



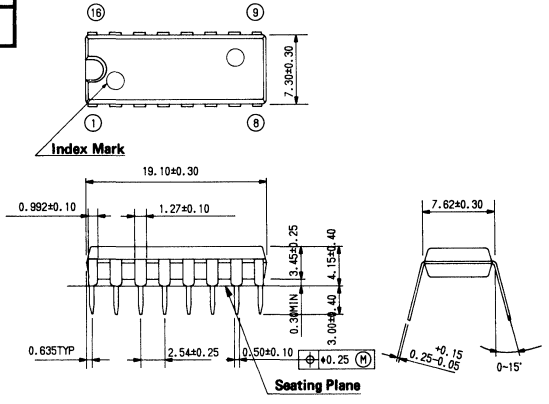
16 PIN PLASTIC DIP

DIP16-P-300



16 PIN PLASTIC DIP

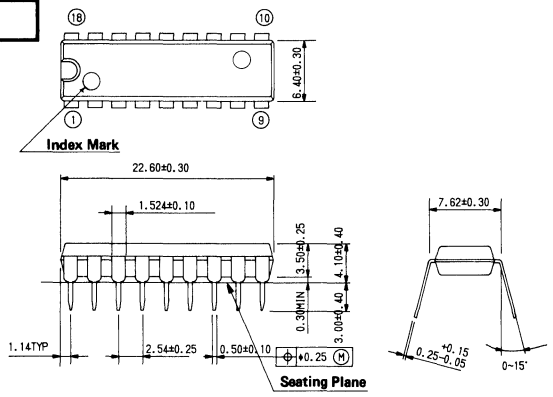
DIP16-P-300-W1



PLASTIC DIP

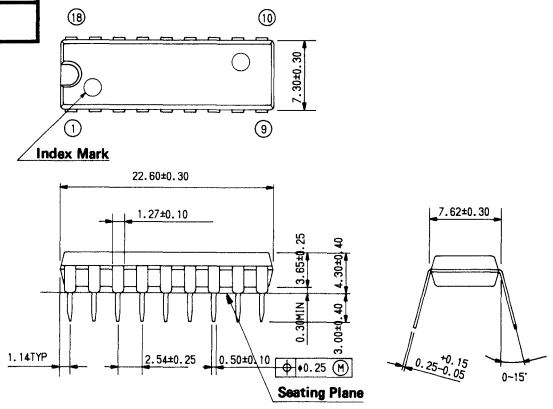
18 PIN PLASTIC DIP

DIP18-P-300



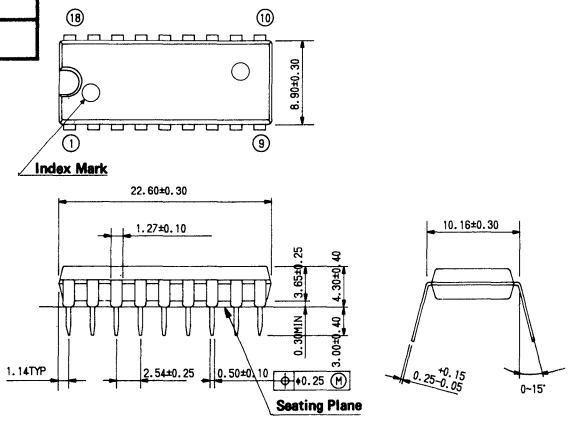
18 PIN PLASTIC DIP

DIP18-P-300-W1



18 PIN PLASTIC DIP

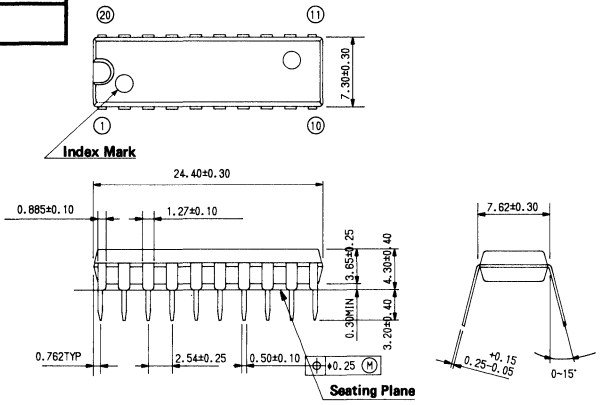
DIP18-P-400



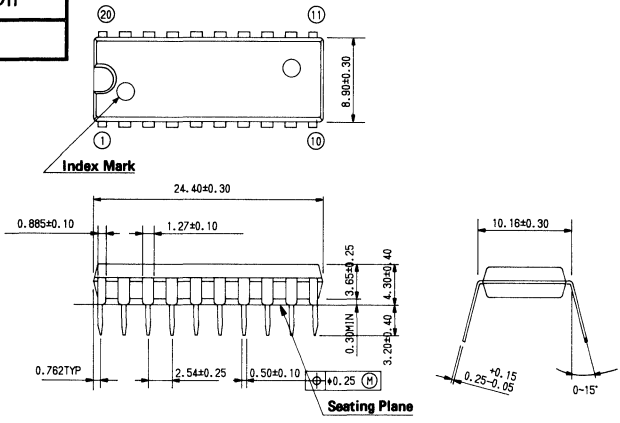
2

PLASTIC DIP

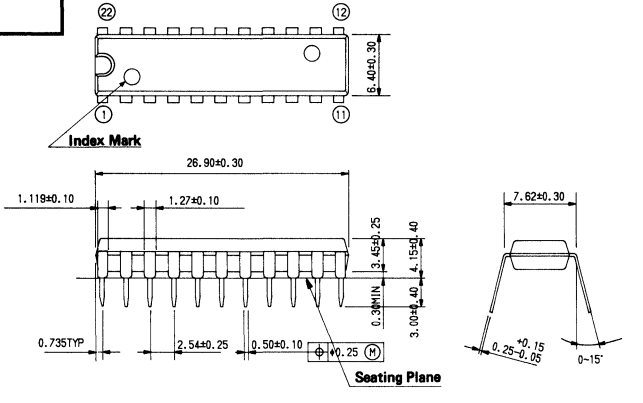
20 PIN PLASTIC DIP
DIP20-P-300-W1



20 PIN PLASTIC DIP
DIP20-P-400



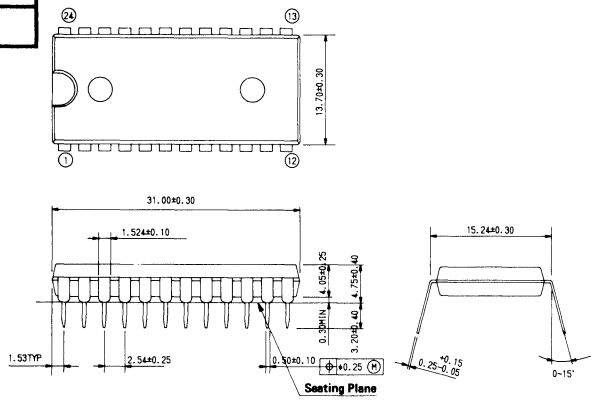
22 PIN PLASTIC SKINNY DIP
DIP22-P-300-S1



PLASTIC DIP

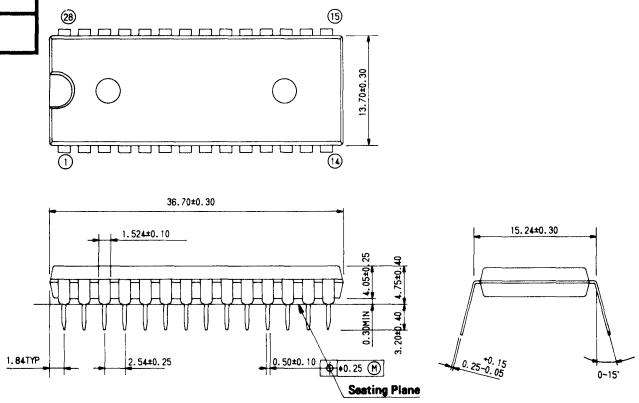
24 PIN PLASTIC DIP

DIP24-P-600



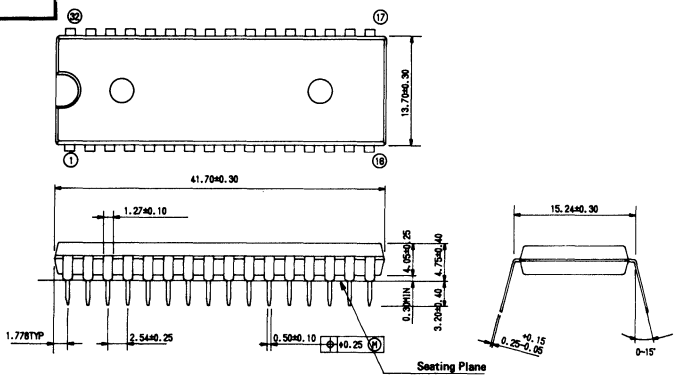
28 PIN PLASTIC DIP

DIP28-P-600



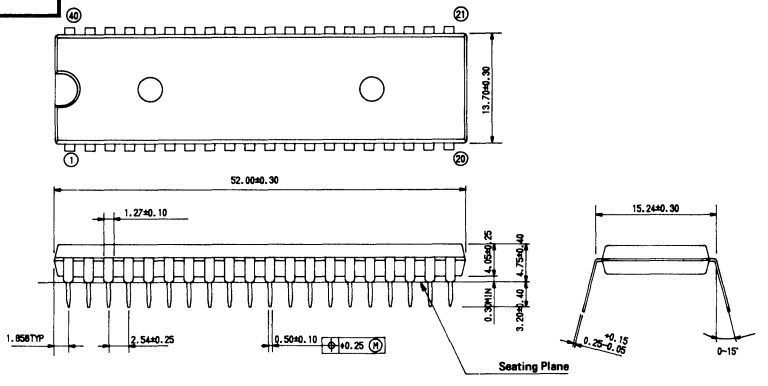
32 PIN PLASTIC DIP

DIP32-P-600



PLASTIC DIP

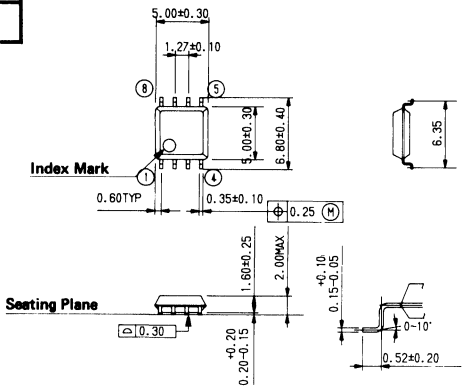
40 PIN PLASTIC DIP
DIP40-P-600



PLASTIC SOP/QFP

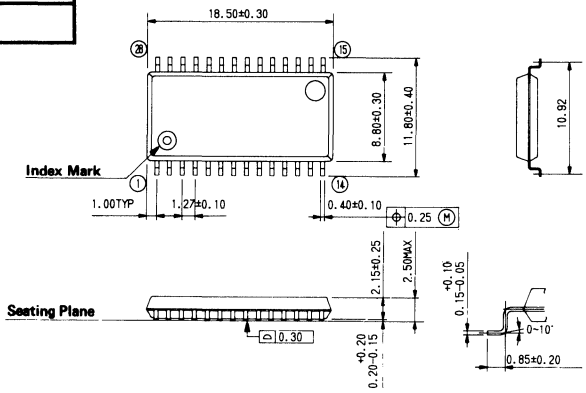
8 PIN PLASTIC SOP

SOP8-P-250-K



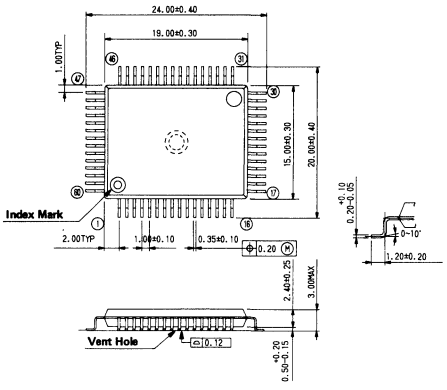
28 PIN PLASTIC SOP

SOP28-P-430-K



60 PIN-V PLASTIC QFP

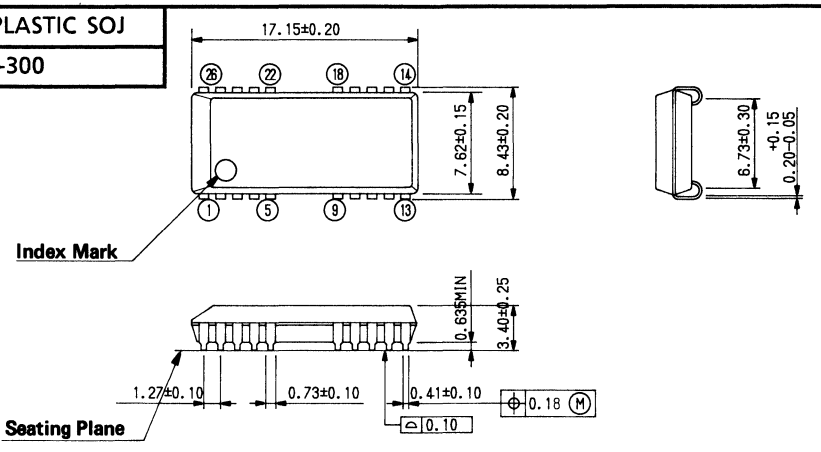
QFP60-P-1519-VK



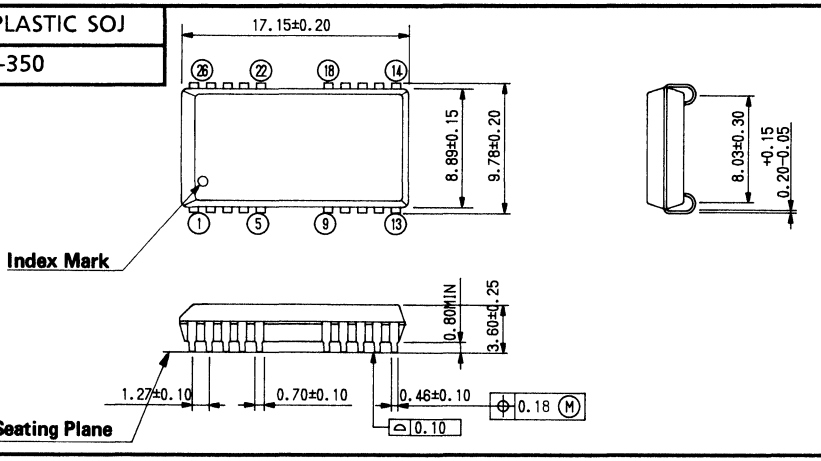
2

PLASTIC SOJ

26 PIN PLASTIC SOJ
SOJ26-P-300

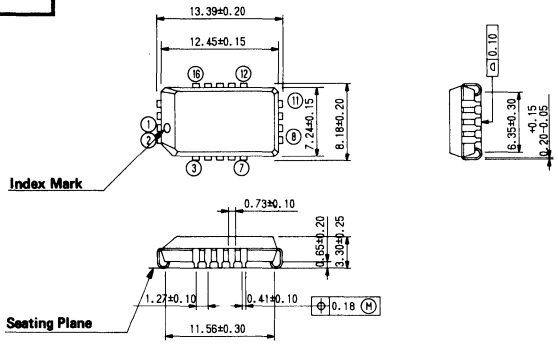


26 PIN PLASTIC SOJ
SOJ26-P-350



PLASTIC QFJ (PLCC)

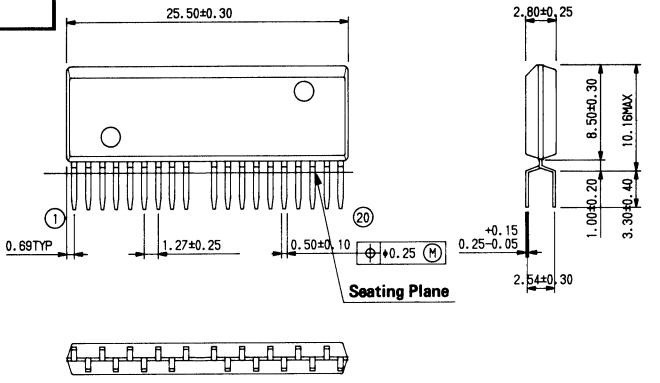
18 PIN PLCC
QFJ18-P-R290



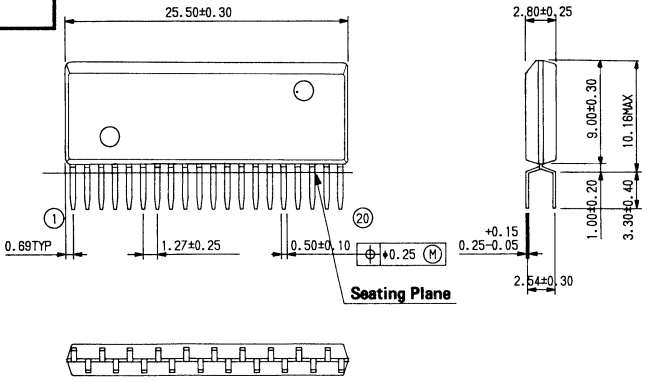
2

PLASTIC ZIP

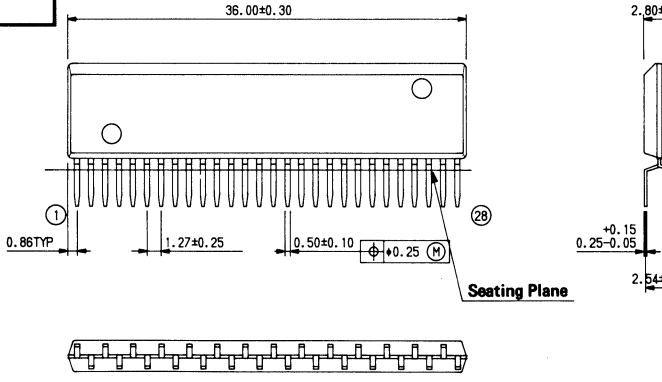
20 PIN PLASTIC ZIP
ZIP20-P-400



20 PIN PLASTIC ZIP
ZIP20-P-400-W1



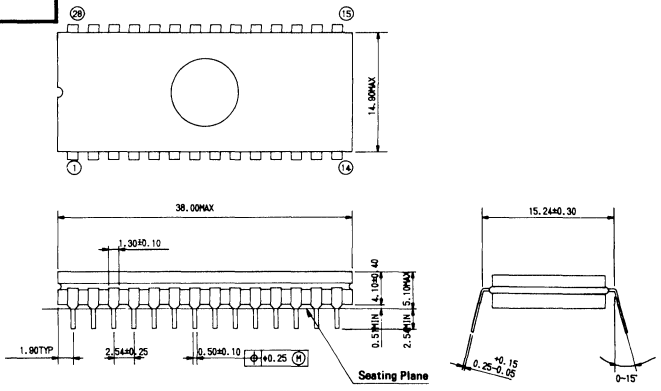
28 PIN PLASTIC ZIP
ZIP28-P-400



CERDIP

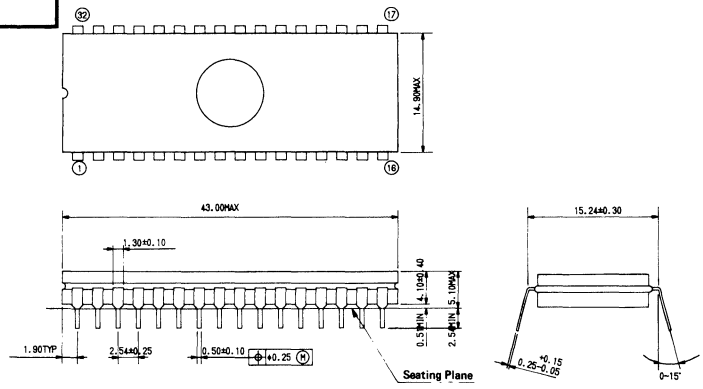
28 PIN CERDIP

WDIP28-G-600



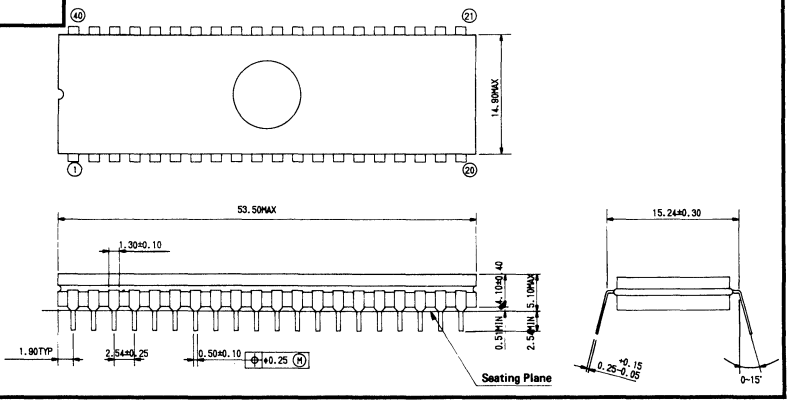
32 PIN CERDIP

WDIP32-G-600



40 PIN CERDIP

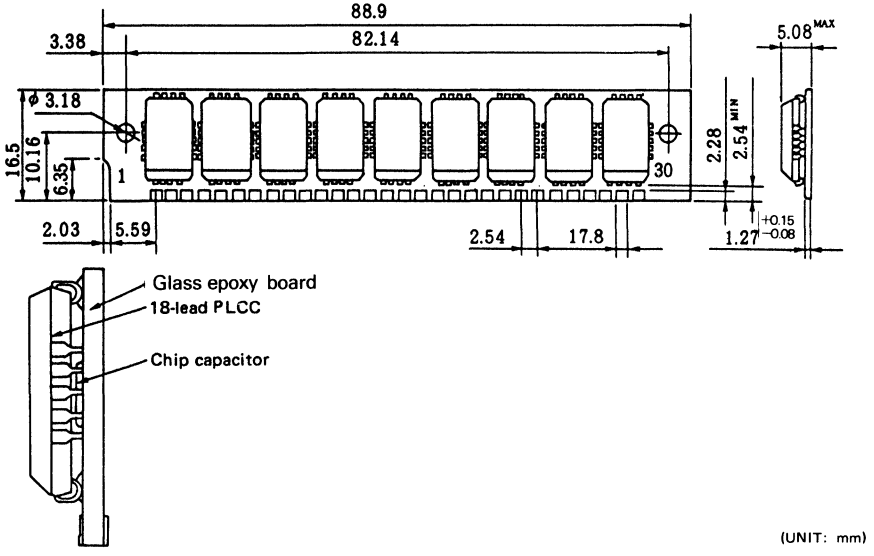
WDIP40-G-600



2

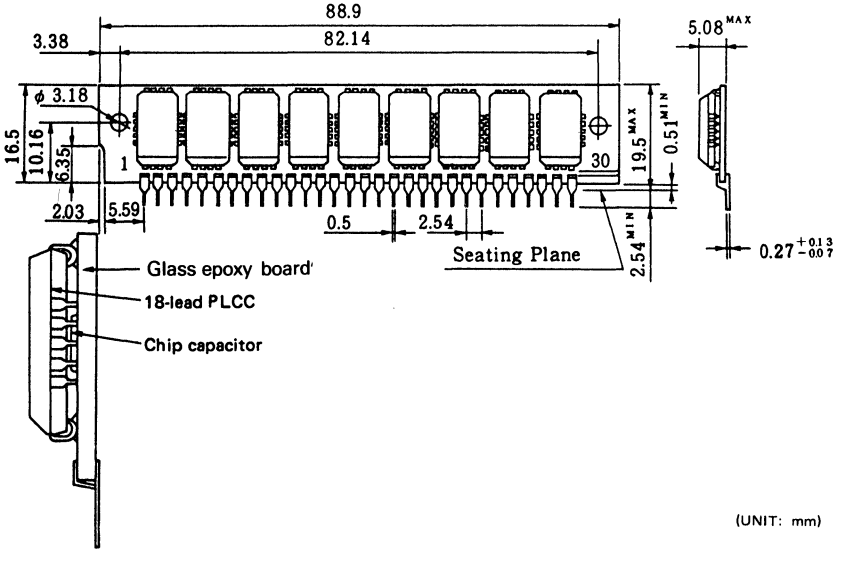
MODULE SIMM/SIMP

30 PIN SIMM (FOR MSC2304/2307YS(9))



(UNIT: mm)

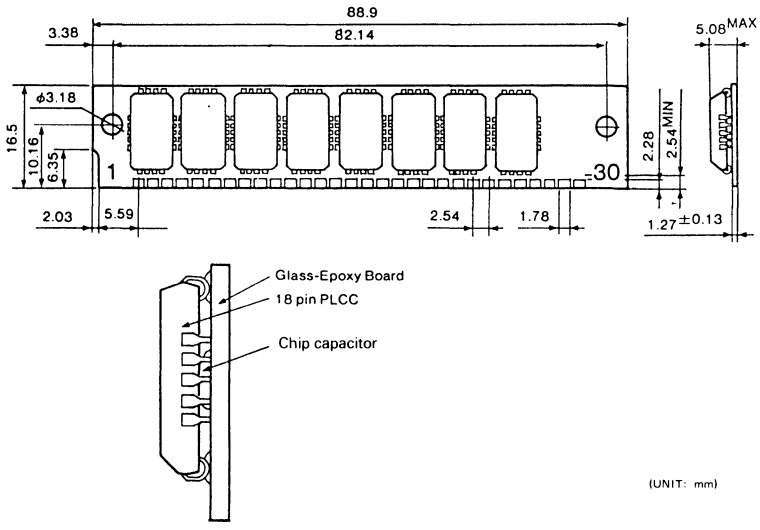
30 PIN SIMM (FOR MSC2304/2307KS(9))



(UNIT: mm)

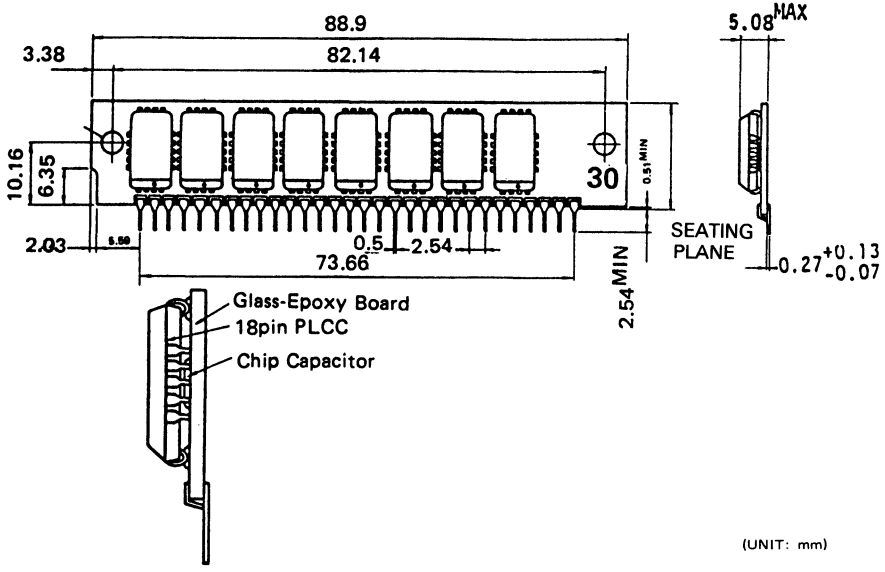
MODULE SIMM/SIMP

30 PIN SIMM (FOR MSC2304YS(8))



(UNIT: mm)

30 PIN SIMP (FOR MSC2304KS(8))

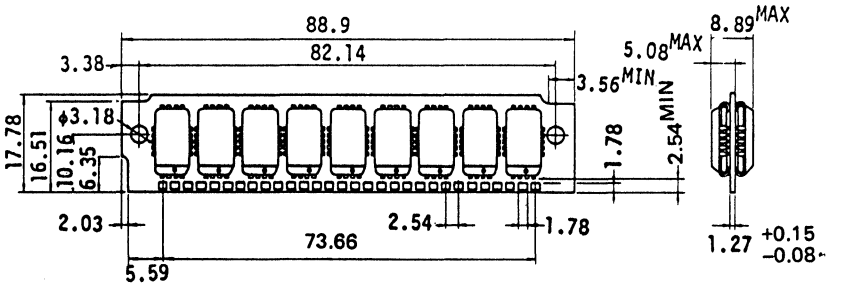


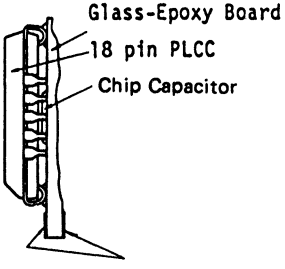
(UNIT: mm)

2

MODULE SIMM/SIMP

30 PIN SIMM (FOR MSC2305YS18A



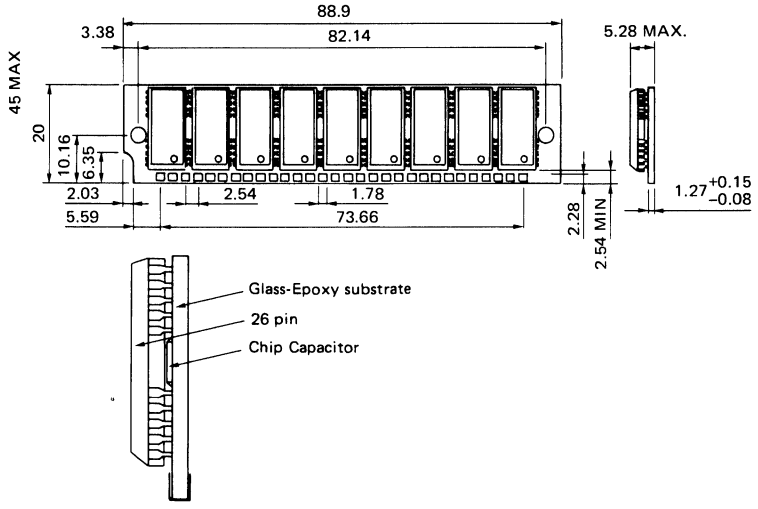


(UNIT:mm)

MODULE SIMM/SIMP

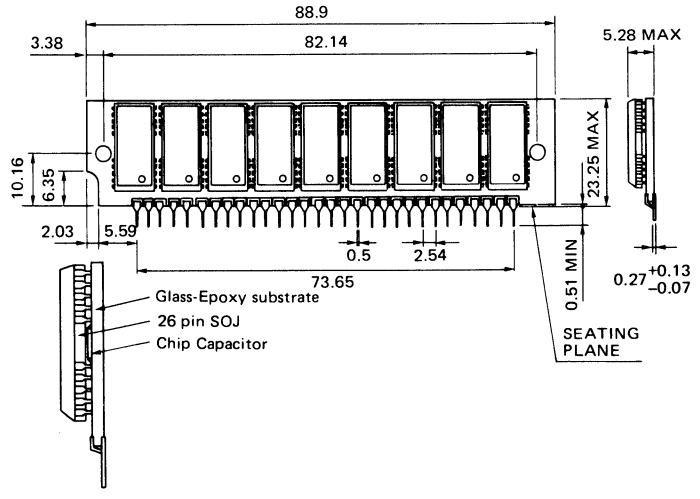
30 PIN SIMM (FOR MSC2312AYS9)

(UNIT: mm)



30 PIN SIMP (FOR MSC2312AKS9)

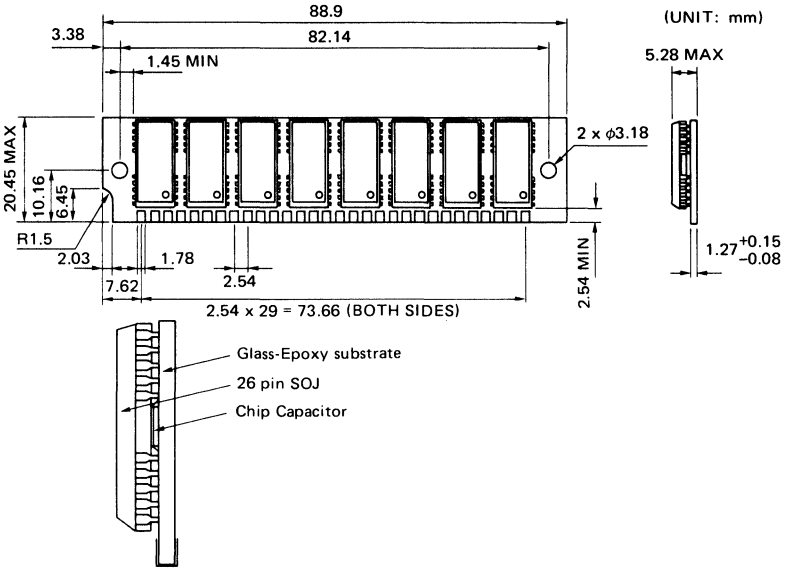
(UNIT: mm)



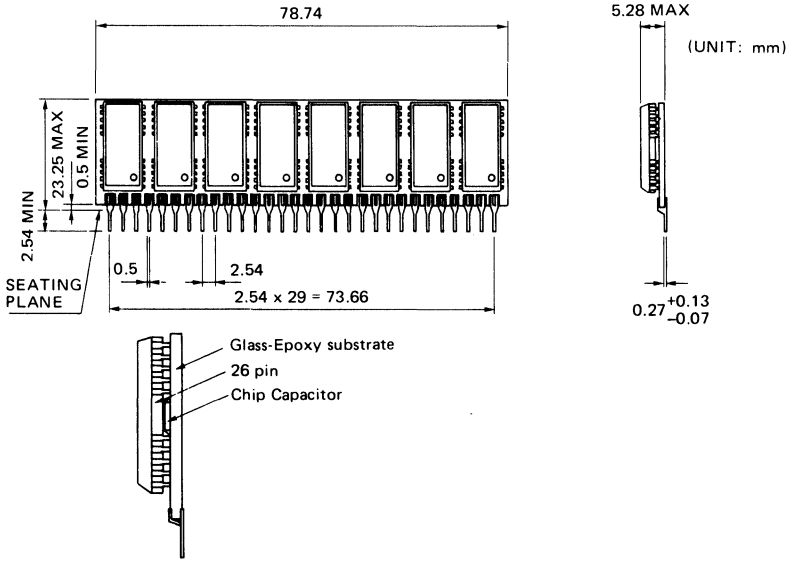
2

MODULE SIMM/SIMP

30 PIN SIMM (FOR MSC2313AYS8)

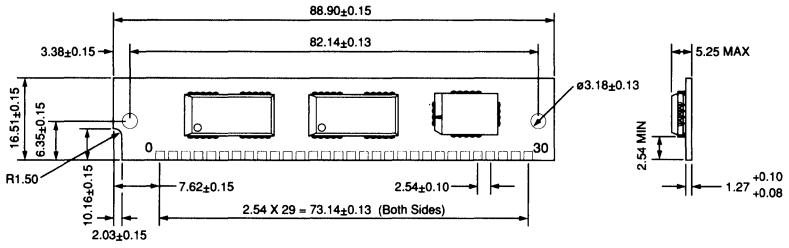


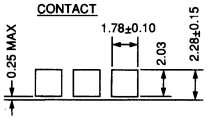
30 PIN SIMP (FOR MSC2313AKS8)



MODULE SIMM/SIMP

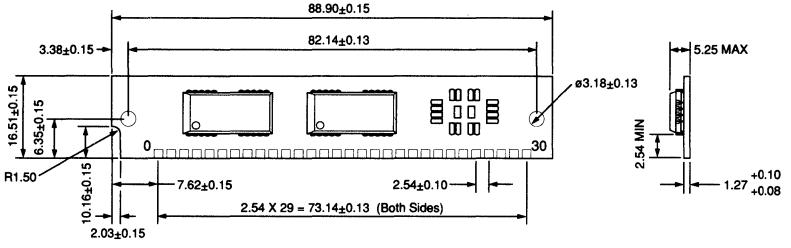
30 PIN SIMM (FOR MSC2331AYS3 OR MSC2329AYS3)

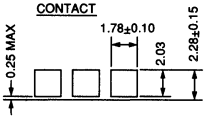




Note:
1) Substrate: Glass-Epoxy (FR-4)
2) Chip Capacitor: Under Component (0.22 x3pcs)
3) Contact Finish: 2.54um Min PB/Sn Over 1.9um Min Ni
4) Contacts are on both sides of PC Board
5) Thickness includes plating

30 PIN SIMM (FOR MSC2328AXXYS2)

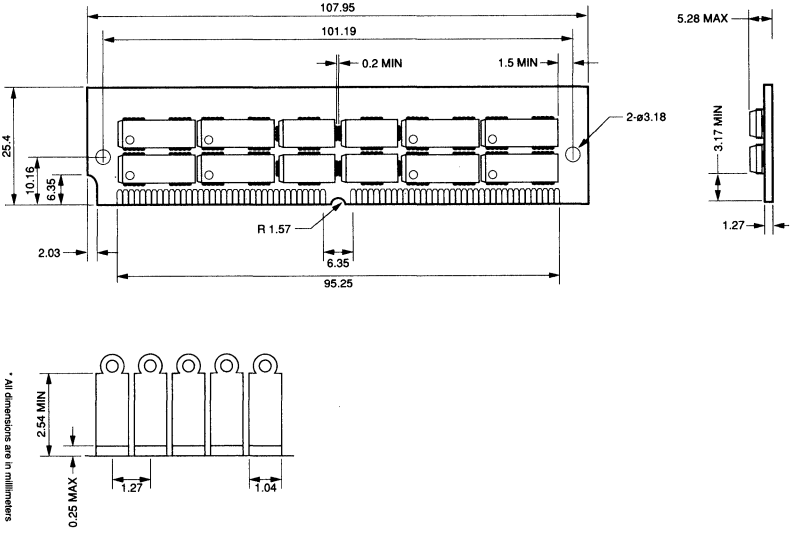




Note:
1) Substrate: Glass-Epoxy (FR-4)
2) Chip Capacitor: Under Component (0.22 x2pcs)
3) Contact Finish: 2.54um Min PB/Sn Over 1.9um Min Ni
4) Contacts are on both sides of PC Board
5) Thickness includes plating

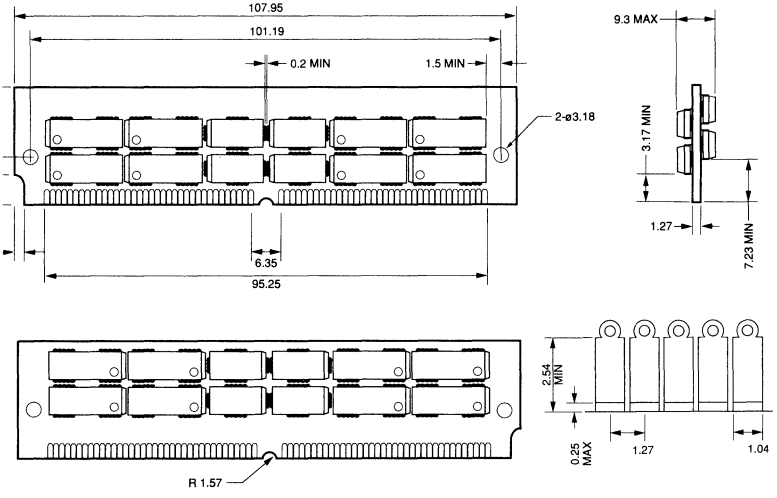
MODULE SIMM/SIMP

72 PIN SIMM (FOR MSC2320AYS9)



MODULE SIMM/SIMP

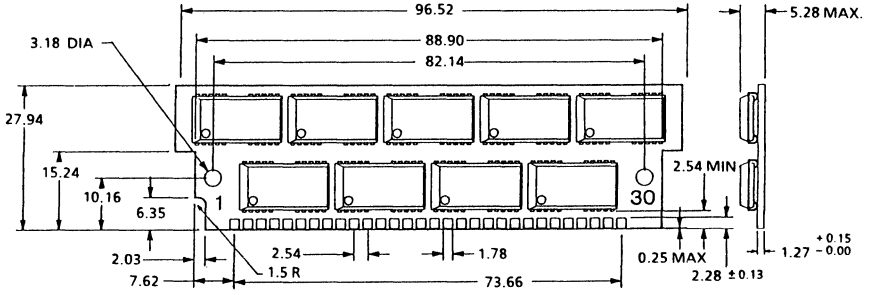
72 PIN SIMM (FOR MSC2321AYS18)



MODULE SIMM/SIMP

30 PIN SIMM (FOR MSC2340YS9)

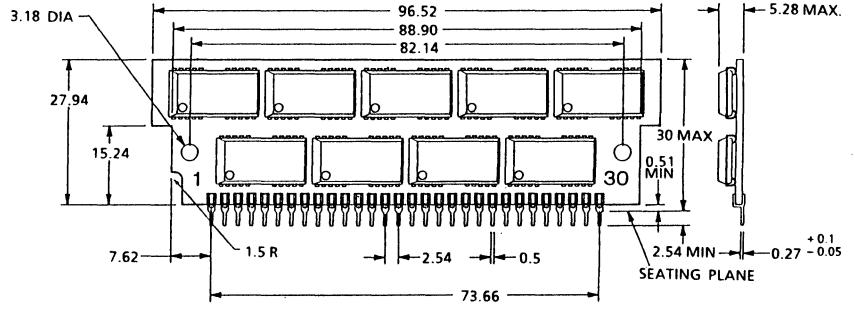
MSC2340YS9



NOTE 1) SUBSTRATE ..... GLASS EPOXY (FR-4)
2) CONTACT PADS .... Pb / Sn or Au PLATING
3) 4M x 1 DRAM x 9 pcs

30 PIN SIMP (FOR MSC2340KS9)

MSC2340KS9



NOTE 1) SUBSTRATE ..... GLASS EPOXY (FR-4)
2) CONTACT LEAD .... Pb / Sn SOLDER
3) SEATING PLANE (PAI 0.83, PITCH 2.54)
4) 4M x 1 DRAM x 9 pcs

RELIABILITY INFORMATION

3

3 RELIABILITY INFORMATION

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RELIABILITY INFORMATION

1. INTRODUCTION

Semiconductor devices play a leading role in the explosive progress of semiconductor technology. They use some of the most advanced design and manufacturing technology developed to date. With greater integration, diversity and reliability, their applications have expanded enormously. Their use in large scale computers, control equipment, calculators, electronic games and in many other fields has increased at a fast rate.

A failure in electronic banking or telephone switching equipment, for example, could have far reaching effects and can cause incalculable losses. So, the demand, for stable high quality memory devices is strong.

We, at Oki are fully aware of this demand. So we have adopted a comprehensive quality assurance system based on the concept of consistency in development, manufacturing and sales.

With the increasing demand for improvement in function, capability and reliability, we will expand our efforts in the future. Our quality assurance system and the underlying concepts are outlined briefy below.

2. QUALITY ASSURANCE SYSTEM AND UNDERLYING CONCEPTS

The quality assurance system employed by Oki can be divided into four major stages: device planning, developmental prototype, production prototype, and mass production. This system is outlined in the following block diagram (Fig. 1).

1) Device planning stage

To manufacture devices that meet market demands and satisfy customer needs, we carefully consider functional and failure rate requirements, utilization form, environment and other conditions. Once we determine the proper type, material and structure, we check the design and manufacturing techniques, and the line processing capacity. Then we prepare the development planning and time schedule.

2) Developmental prototype stage

We determine circuits, pattern design, process settings, assembly techniques and structural requirements during this stage. At the same time, we carry out actual prototype reliability testing.

Since device quality is largely determined during the designing stage, Oki pays careful attention to quality confirmation during this stage.

This is how we do it:

(1) After completion of circuit design (or pattern design), personnel from the design, process technology, production technology, installation technology and reliability departments get together for a thorough review to ensure design quality and to anticipate problems that may occur during mass production. Past experience and know-how guide these discussions.

(2) Since many semiconductor memories involve new concepts and employ high level manufacturing technology, the TEG evaluation test is often used during this stage.

Note: TEG (Test Element Group) refers to the device group designed for stability evaluation of MOS transistors, diodes, resistors, capacitors and other circuit component element used in LSI memories.

(3) Prototypes are subjected to repeated reliability and other special evaluation tests. In addition, the stability and capacity of the manufacturing process are checked.

3) Production prototype stage

During this stage, various tests check the reliability and other special features of the production prototype at the mass production factory level. After confirming the quality of a device, we prepare the various standards required for mass production, and then start production. Although reliability and other special tests performed on the production prototype are much the same as those performed on the developmental prototype, the personnel, facilities and production site differ for the two prototypes, necessitating repeated confirmation tests.

4) Mass production

During the mass production stage, careful management of purchased materials, parts and facilities used during the manufacturing process, measuring equipment, manufacturing conditions and environment is necessary to ensure device quality first stipulated during the designing stages. The manufacturing process (including inspection of the completed device) is followed by a lot guarantee inspection to check that the specified quality is maintained under conditions identical to those under which a customer would actually use the device. This lot guarantee inspection is performed in three different forms as shown below.

(1) Group A tests: appearance, labels, dimensions and electrical characteristics inspection

(2) Group B tests: check of durability under thermal and mechanical environmental stresses, and operating life characteristics

(3) Group C tests: performed periodically to check operational life, etc., on a long term basis.

Note: Like the reliability tests, the group B tests conform to the following standards.
MIL-STD-883B, JIS C 7022, EIAJ-IC-121

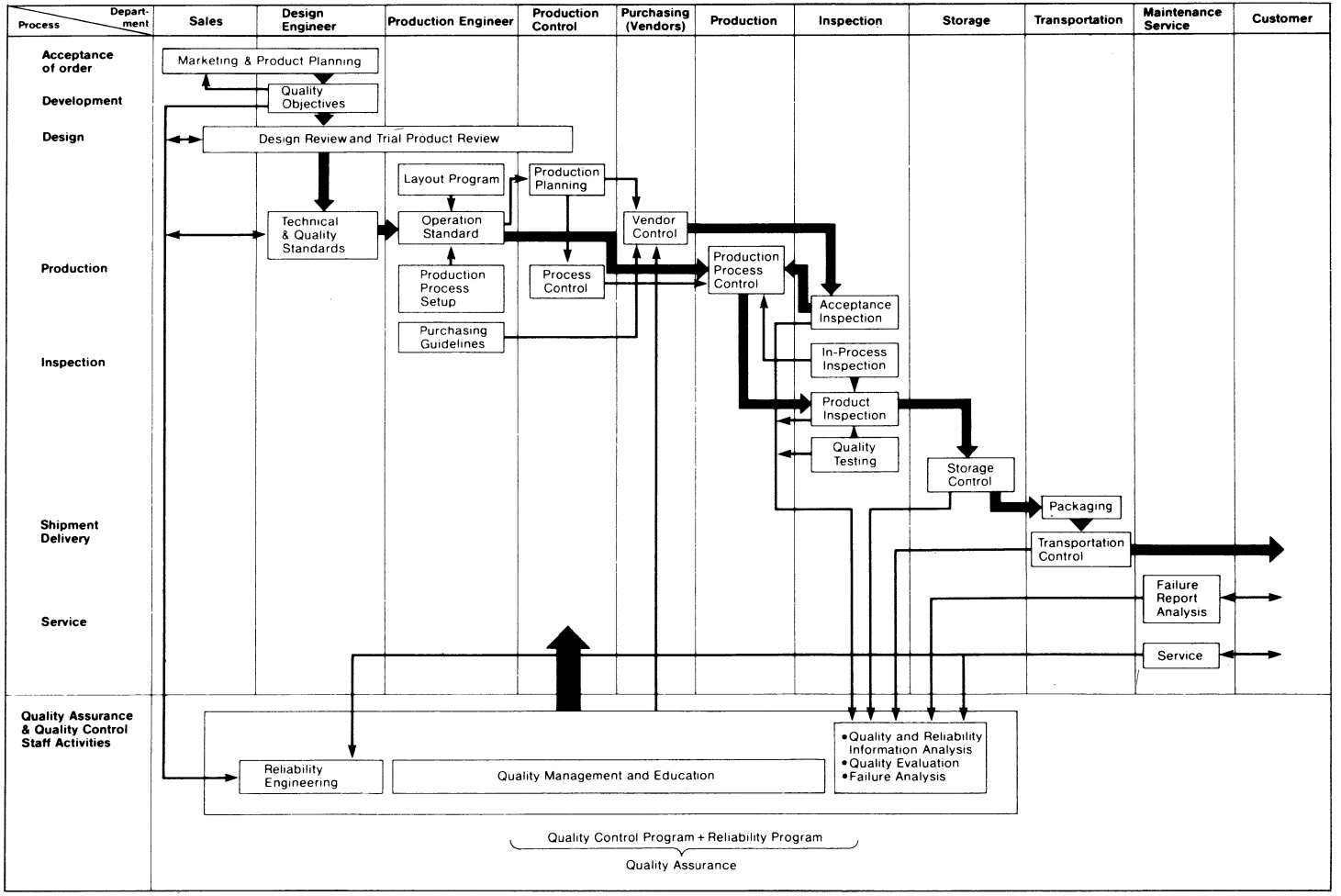


Figure 1 Quality Assurance System

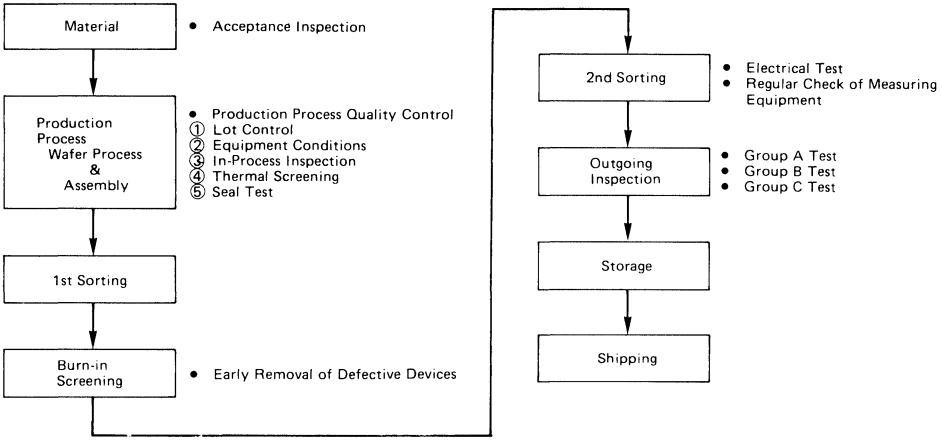


Figure 2 Manufacturing Process

Devices which pass these lot guarantee inspections are stored in a warehouse awaiting shipment to customers. Standards are also set up for handling, storage and transportation during this period, thereby ensuring quality prior to delivery. Figure 2 shows the manufacturing flow of the completed device.

5) At Oki, all devices are subjected to thorough quality checks. If, by chance, a failure does occur after delivery to the customer, defective devices are processed and the problem rectified immediately to minimize the inconvenience to the customer in accordance with the following flowchart.

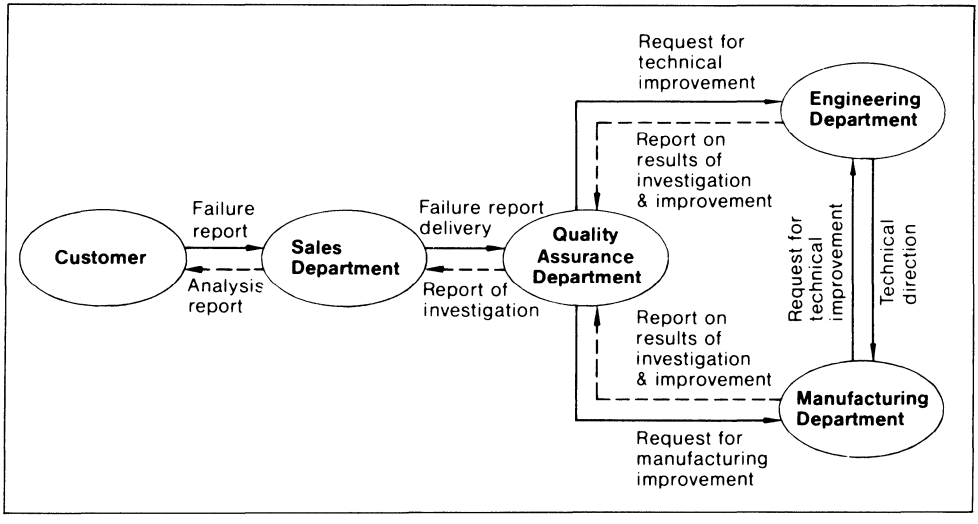
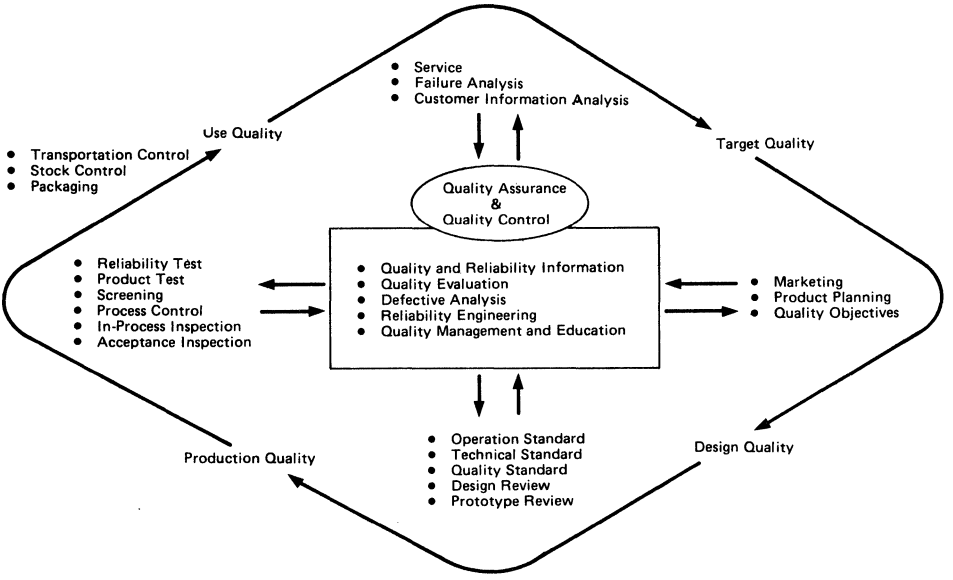


Figure 3 Failure report process



3. EXAMPLE OF RELIABILITY TEST RESULTS

We have outlined the quality assurance system and the underlying concepts employed by Oki. Now, we will give a few examples of the reliability tests performed during the developmental and production prototype stages. All reliability tests performed by Oki conform to the following standards.

MIL-STD-883B, JIS C 7022, EIAJ-IC-121

Since these reliability tests must determine performance under actual working conditions in a short period of time, they are performed under severe test conditions. For example, the 125°C high temperature continuous operation test performed for 1000 hours is equivalent to testing device life from 2 to 300 years of use at Ta = 40°C.
By repeating these accelerated reliability tests, device quality is checked and defects analyzed. The resulting information is extremely useful in improving the manufacturing processes. Some of the more common defects in LSI elements and their analysis are described on next page.

OKI MEMORY LSI LIFE TEST RESULTS

Test item	Test condition	Device name	MSM511000ARS			MSM514256AJS			MSM511000AZS		
		Function	1M × 1 bit DYNAMIC RAM			256K × 4 bit DYNAMIC RAM			1M × 1 bit DYNAMIC RAM		
		Structure	Si gate C-MOS 18P P-DIP			Si gate C-MOS 26P SOJ			Si gate C-MOS 20P ZIP		
			Sample size	Test hours	Failures	Sample Size	Test hours	Failures	Sample size	Test hours	Failures
Operating life test	Ta = 125°C Vcc = 7.0V		200	2000	0	200	2000	1*	100	2000	0
	Ta = 150°V Vcc = 7.0V		100	2000	0	100	2000	0	–	–	–
Temperature humidity test	130°C 85% Vcc = 5.5V		100	120	0	100	120	0	100	120	0
	85°C 85% Vcc = 5.5V		400	2000	0	500	2000	0	200	2000	0
Pressure cooker test	121°C 100% No bias		50	500	0	50	500	0	50	500	0
Low temperature life test	Ta = −10°C Vcc = 7.0V		60	2000	0	22	2000	0	–	–	–
Temperature cycling test	−65°C ~ 25°C ~ 150°C (70min/cycle)		400	1000 cycles	0	300	1000 cycles	0	200	1000 cycles	0

Test item	Test condition	Device name	MSM41256ARS			MSM2312YS9			MSC2304KS		
		Function	256K × 1 bit DYNAMIC RAM			1M × 9 bit DYNAMIC RAM			256K × 9 bit DYNAMIC RAM		
		Structure	Si gate N-MOS 16P P-DIP			Si gate C-MOS 30P SIMM			Si gate N-MOS 30P SIP		
			Sample size	Test hours	Failures	Sample size	Test hours	Failures	Sample size	Test hours	Failures
Operating life test	Ta = 125°C Vcc = 7.0V		500	2000	0	40	1000	0	40	1000	0
	Ta = 150°C Vcc = 7.0V		45	4000	0	–	–	–	–	–	–
Temperature humidity test	130°C 85% Vcc = 5.5V		100	120	0	–	–	–	–	–	–
	85°C 85% Vcc = 5.5V		300	2000	0	40	1000	0	40	1000	0
Pressure cooker test	121°C 100% No bias		100	500	0	–	–	–	–	–	–
Low temperature life test	Ta = −10°C Vcc = 7.0V		60	2000	0	–	–	–	–	–	–
Temperature cycling test	−65°C ~ 25°C 150°C (70min/cycle)		200	1000 cycles	0	40	2000 cycles **	0	40	2000 cycles **	0

*: SINGLE BIT FAIL **: 0°C ~ 125°C 20 min/c

3

OKI MEMORY LSI LIFE TEST RESULTS

Test item	Test condition	Device name	MSM51257ALRS			MSM271000AS			MSM534000RS		
		Function	32K × 8 bit STATIC RAM			128K × 8 bit UV erasable EP ROM			512K × 8 bit Mask ROM		
		Structure	Si gate C-MOS 28P P-DIP			Si gate N-MOS 28P cerdip			Si gate C-MOS 28P P-DIP		
			Sample size	Test hours	Failures	Sample size	Test hours	Failures	Sample size	Test hours	Failures
Operating Life test	Ta = 125°C Vcc = 7.0 V		200	2000	0	88	*2000	0	88	2000	0
High temperature storage life	Ta = 200°C		—	—	—	100	2000	1**	—	—	—
Temperature humidity test	130°C 85% Vcc = 5.5V		50	120	0	—	—	—	22	120	0
	85°C 85% Vcc = 5.5V		200	2000	0	50	*1000	0	80	2000	0
Pressure cooker test	121°C 100% No bias		50	500	0	—	—	—	50	200	0
Low temperature life test	Ta = −10°C Vcc = 7.0V		22	2000	0	22	2000	0	22	2000	0
Temperature cycling test	−65°C ~ 25°C 150°C (70min/cycle)		200	1000 cycles	0	100	500 cycles	0	100	500 cycles	0

Test item	Test Condition	Device Name	MSM51257AGSK			MSM271000ZBRS			MSM28C64ARS		
		Function	32K × 8 bit STATIC RAM			128K × 8 bit OTP			8K × 8 bit EEPROM		
		Structure	Si gate C-MOS 28P SOP			Si gate N-MOS 28P P-DIP			Si gate C-MOS 28P P-DIP		
			Sample size	Test hours	Failures	Sample size	Test hours	Failures	Sample size	Test hours	Failures
Operating Life test	Ta = 125°C Vcc = 5.5V		—	—	—	88	*2000	0	100	2000	0
High temperature storage life	Ta = 155°C		—	—	—	100	2000	0	200	2000	***1
Temperature humidity test	130°C 85% Vcc = 5.5V		50	120	0	50	*120	0	50	120	0
	85°C 85% Vcc = 5.5V		200	2000	0	100	*2000	0	100	2000	0
Pressure cooker test	121°C 100% No bias		50	300	0	22	300	0	22	300	0
Low temperature life test	Ta = −10°C Vcc = 7.0V		—	—	—	22	2000	0	22	2000	0
Temperature cycling test	−65°C ~ 25°C ~ 150°C (70 min/cycle)		200	500	0	100	500	0	100	500	0

* : Vcc = 5.25V ** : Charge loss fail
*** : Charge loss fail (high temperature storage test after 10k W/E cycles test at Ta = 25°C)

OKI MEMORY LSI ENVIRONMENTAL TEST RESULTS

Test item		Device name / Test condition	MSM511000ARS Sample size	MSM511000ARS Failures	MSM514256AJS Sample size	MSM514256AJS Failures	MSM511000AZS Sample size	MSM511000AZS Failures
Thermal environmental test	Soldering heat	260°C 10 sec	22	0	22	0	22	0
	Thermal shock	0°C~100°C 5 min 5 min 10 cycles						
	Temperature cycling	−65°C ~ RT ~ 150°C 30 min 30 min 20 cycles						
Mechanical environmental test	Variable frequency vibration	100Hz~2000Hz 4 min per cycle 4 times in X, Y, Z	22	0	22	0	22	0
	Shock	1500G, 0.5 ms, 5 times in each X, Y, Z						
	Constant acceleration	20000G 1 min in each X, Y, Z						
Electrical Environmental test	ESD	100pF, 1.5kΩ, 5 times ±1000V	10	0	10	0	10	0

Test item		Device name / Test condition	MSM41256ARS Sample size	MSM41256ARS Failures	MSC2312YS9 Sample size	MSC2312YS9 Failures	MSC2304KS9 Sample size	MSC2304KS9 Failures
Thermal environmental test	Soldering heat	260°C 10 sec	22	0	22*	0	22*	0
	Thermal shock	0°C~100°C 5 min 5 min 10 cycles						
	Temperature cycling	−65°C ~ RT ~ 150°C 30 min 30 min 20 cycles						
Mechanical environmental test	Variable frequency vibration	100Hz~2000Hz 4 min per cycle 4 times in X, Y, Z	22	0	—	—	—	—
	Shock	1500G, 0.5 ms, 5 times in each X, Y, Z						
	Constant acceleration	10000G or 20000G 1 min in each X, Y, Z						
Electrical environmental test	ESD	100pF, 1.5kΩ, 5 times ±1000V	10	0	—	—	—	—

*: TEMPERATURE CYCLING: −40°C ~ 25°C ~ 125°C (20 cycles)
(30 min) (30 min)

OKI MEMORY LSI ENVIRONMENTAL TEST RESULTS

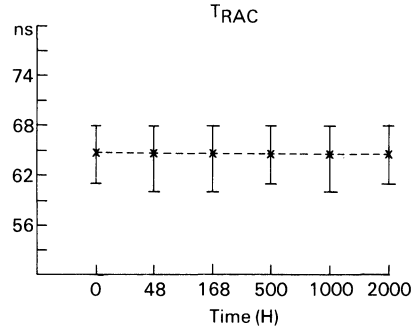
Test item		Test condition	MSM51257ALRS Sample size	MSM51257ALRS Failures	MSM271000AS Sample size	MSM271000AS Failures	MSM534000RS Sample size	MSM534000RS Failures
Thermal environmental test	Soldering heat	260°C 10 sec	22	0	22	0	22	0
	Thermal shock	0°C~100°C 5 min 5 min 10 cycles						
	Temperature cycling	−65°C ~ RT ~ 150°C 30 min 30 min 20 cycles						
Mechanical environmental test	Variable frequency vibration	100Hz~2000Hz 4 min per cycle 4 times in X, Y, Z	22	0	22	0	22	0
	Shock	1500G, 0.5 ms, 5 times in each X, Y, Z						
	Constant acceleration	10000G or 20000G 1 min in each X, Y, Z						
Electrical environmental test	ESD	100pF, 1.5kΩ, 5 times ±1000V	10	0	10	0	—	—

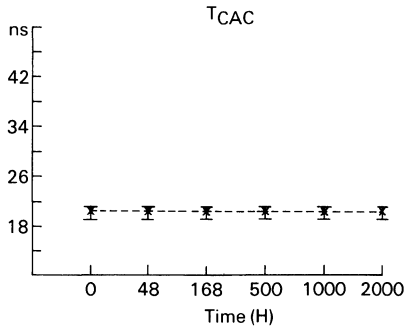
Test item		Test condition	MSM51257AGSK Sample size	MSM51257AGSK Failures	MSM27000ZBRS Sample size	MSM27000ZBRS Failures	MSM28C64ARS Sample size	MSM28C64ARS Failures
Thermal environmental test	Soldering heat	260°C 10 sec	22	0	22	0	22	0
	Thermal shock	0°C ~ 100°C 5 min 5 min 10 cycles						
	Temperature cycling	−65°C ~ RT ~ 150°C 30 min 30 min 20 cycles						
Mechanical environmental test	Variable frequency vibration	100Hz ~ 2000Hz 4 min per cycle 4 times in X, Y, Z	22	0	22	0	22	0
	Shock	1500G, 0.5 ms, 5 times in each X, Y, Z						
	Constant acceleration	10000G or 20000G 1 min in each X, Y, Z						
Electrical environmental test	ESD	100pF, 1.5kΩ, 5 times ±1000V	—	—	—	—	10	0

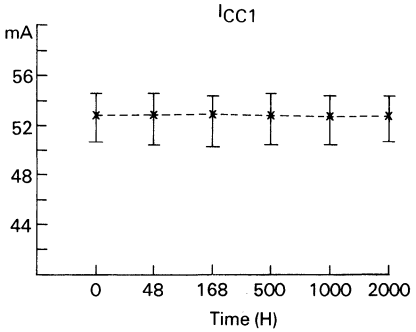
HIGH TEMPERATURE OPERATING LIFE TEST

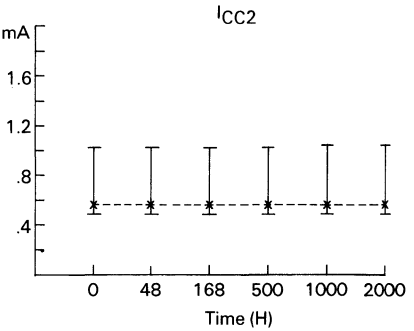
MSM511000ARS Ta = 25°C Sample size 200

			0	48	168	500	1000	2000
I_{CC1}	mA	MAX.	54.60	54.60	54.40	54.60	54.40	54.40
		MIN.	50.60	50.40	50.20	50.40	50.40	50.60
		MEAN	52.85	52.86	52.89	52.87	52.66	52.76
		S.D.	.87	.85	.84	.87	.92	.88
		DEL.	0.00	0.00	0.00	0.00	0.00	0.00
I_{CC2}	mA	MAX.	1.0200	1.0200	1.0200	1.0200	1.0400	1.0400
		MIN.	.4780	.4800	.4800	.4820	.4860	.4800
		MEAN	.5586	.5603	.5626	.5615	.5562	.5627
		S.D.	.0756	.0741	.0732	.0750	.0765	.0747
		DEL.	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000
T_{RAC}	ns	MAX.	68.0	68.0	68.0	68.0	68.0	68.0
		MIN.	61.0	60.0	60.0	61.0	60.0	61.0
		MEAN	64.8	64.6	64.6	64.7	64.5	64.7
		S.D.	1.6	1.7	1.7	1.7	1.7	1.7
		DEL.	0.0	0.0	0.0	0.0	0.0	0.0
T_{CAC}	ns	MAX.	21.0	21.0	21.0	21.0	21.0	21.0
		MIN.	19.0	19.0	19.0	19.0	19.0	19.0
		MEAN	20.4	20.3	20.3	20.3	20.3	20.3
		S.D.	.6	.6	.6	.6	.6	.6
		DEL.	0.0	0.0	0.0	0.0	0.0	0.0





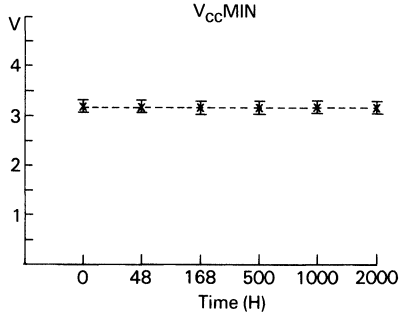


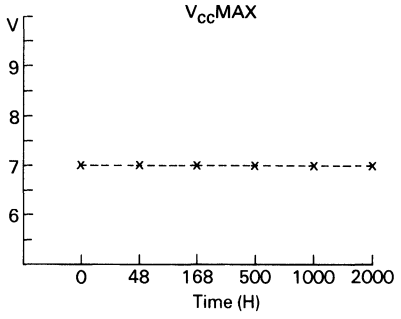


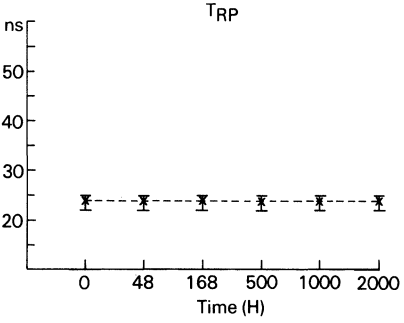
HIGH TEMPERATURE OPERATING LIFE TEST

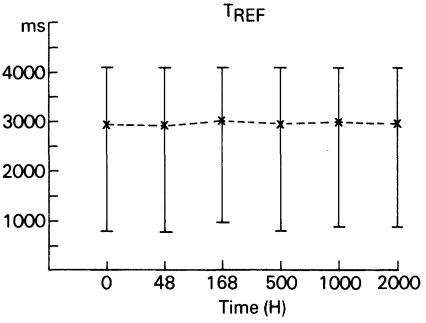
MSM511000ARS Ta = 25°C Sample size 200

		0	48	168	500	1000	2000
T_{RP} ns	MAX.	25.0	25.0	25.0	25.0	25.0	25.0
	MIN.	22.0	22.0	22.0	22.0	22.0	22.0
	MEAN	24.0	24.0	23.9	23.9	23.9	23.9
	S.D.	.8	.8	.9	.8	.9	.8
	DEL.	0.0	0.0	0.0	0.0	0.0	0.0
T_{REF} ms	MAX.	4096.0	4096.0	4096.0	4096.0	4096.0	4096.0
	MIN.	787.0	774.0	983.3	803.0	876.0	844.0
	MEAN	2933.3	2915.1	3015.6	2951.7	3013.6	2988.6
	S.D.	1313.0	1451.9	1246.6	1287.2	1273.4	1290.9
	DEL.	0.0	0.0	0.0	0.0	0.0	0.0
$V_{CC}MIN$ V	MAX.	3.320	3.310	3.290	3.300	3.300	3.290
	MIN.	3.070	3.060	3.050	3.050	3.050	3.050
	MEAN	3.167	3.162	3.156	3.159	3.154	3.155
	S.D.	.056	.057	.056	.055	.055	.055
	DEL.	0.000	0.000	0.000	0.000	0.000	0.000
$V_{CC}MAX$ V	MAX.	7.000	7.000	7.000	7.000	7.000	7.000
	MIN.	7.000	7.000	7.000	7.000	7.000	7.000
	MEAN	7.000	7.000	7.000	7.000	7.000	7.000
	S.D.	0.000	0.000	0.000	0.000	0.000	0.000
	DEL.	0.000	0.000	0.000	0.000	0.000	0.000







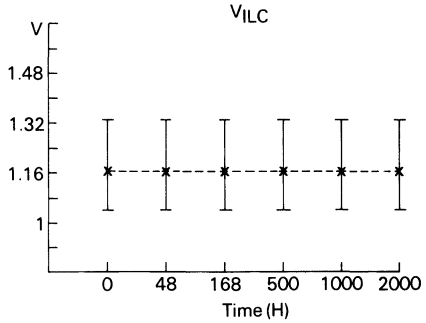


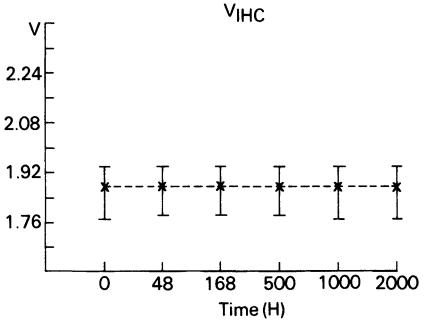
HIGH TEMPERATURE OPERATING LIFE TEST

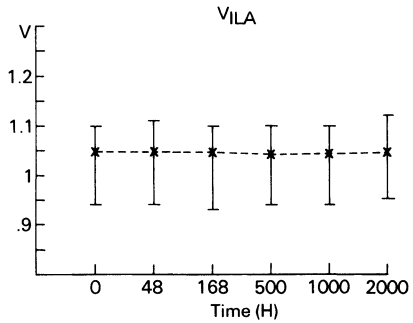
MSM511000ARS Ta = 25°C

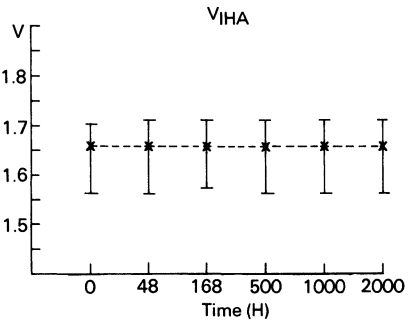
Sample size 200

		0	48	168	500	1000	2000
V_{ILA} V	MAX.	1.100	1.100	1.100	1.100	1.100	1.200
	MIN.	.940	.940	.930	.940	.940	.950
	MEAN	1.047	1.047	1.047	1.042	1.045	1.046
	S.D.	.028	.028	.029	.028	.028	.029
	DEL.	0.000	0.000	0.000	0.000	0.000	0.000
V_{IHA} V	MAX.	1.700	1.710	1.710	1.710	1.710	1.710
	MIN.	1.560	1.560	1.570	1.560	1.560	1.560
	MEAN	1.656	1.656	1.656	1.656	1.658	1.656
	S.D.	.027	.027	.027	.027	.028	.027
	DEL.	0.000	0.000	0.000	0.000	0.000	0.000
V_{ILC} V	MAX.	1.330	1.330	1.330	1.330	1.330	1.330
	MIN.	1.040	1.040	1.040	1.040	1.040	1.040
	MEAN	1.166	1.165	1.168	1.166	1.160	1.163
	S.D.	.061	.062	.062	.060	.057	.060
	DEL.	0.000	0.000	0.000	0.000	0.000	0.000
V_{IHC} V	MAX.	1.940	1.940	1.940	1.940	1.940	1.940
	MIN.	1.770	1.780	1.780	1.780	1.770	1.770
	MEAN	1.876	1.876	1.878	1.877	1.877	1.876
	S.D.	.032	.032	.031	.032	.032	.031
	DEL.	0.000	0.000	0.000	0.000	0.000	0.000









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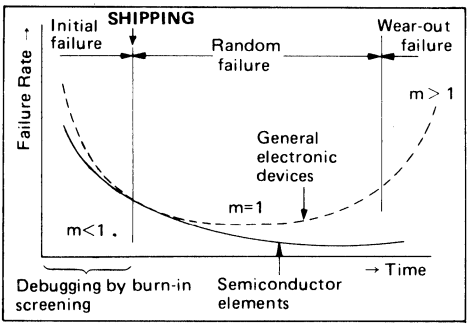
4. SEMICONDUCTOR MEMORY FAILURES

The life-span characteristics of semiconductor elements in general (not only semiconductor IC devices) is described by the curve shown in the diagram below. Although semiconductor memory failures are similar to those of ordinary integrated circuits, the degree of integration (miniaturization), manufacturing complexity and other circuit element factors influence their incidence.

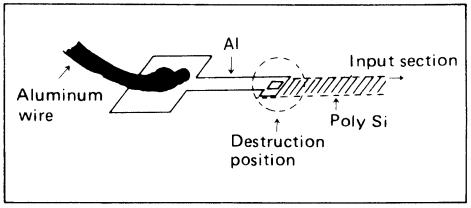
Semiconductor Element Failure Rate Curve



1) Surge Destruction

This is destruction of the input/output stage circuits by external surge currents or static electricity. The accompanying photograph shows a point of contact between aluminum and polysilicon that has been dissolved by a surge current. A hole has formed in the substrate silicon, leading to a short circuit. This kind of failure is traceable in about 30% of defective devices returned to the manufacturer. Despite miniaturization of semiconductor memory component elements (which means the elements themselves are less resistant), these failures usually occur during assembly and other handling operations.

At Oki, all devices are subjected to static electricity intensity tests (under simulated operational conditions) in the development stage to reduce this type of failure. In addition to checking endurance against surge currents, special protective circuits are incorporated in the input and output sections.



2) Oxide Film Insulation Destruction (Pin Holes)

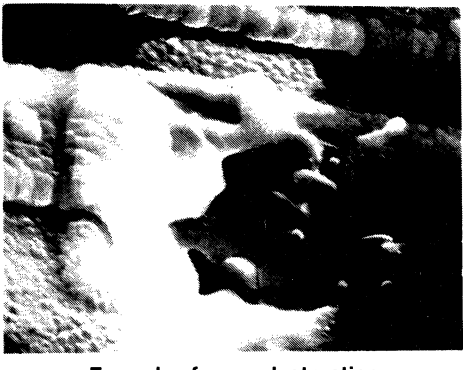
Unlike surge destruction, this kind of failure is caused by manufacturing defects. Local weakened sections are ruptured when subjected to external electrical stress. Although this problem is accentuated by the miniaturization of circuit elements, it can be resolved by maintaining an ultra-clean manufacturing environment and through 100% burn-in screening.

3) Surface Deterioration due to Ionic Impurities

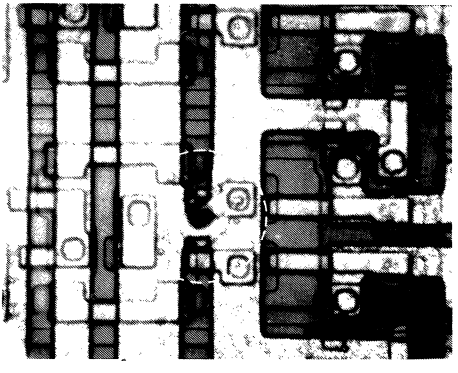
Under some temperature and electric field conditions, charged ionic impurities moving within the oxide film previously resulted in occasional deterioration of silicon surfaces. This problem has been eliminated by new surface stabilization techniques.

4) Photolithographic Defects

Integrated circuits are formed by repeated photographic etching processes. Dust and scratches on the mask (which corresponds to a photographic negative) can cause catastrophic defects. At present, component elements have been reduced in size to the order of 10 cm through miniaturization. However, the size of dust and scratches stays the same. At Oki, a high degree of automation, minimizing human intervention in the process, and unparalleled cleanliness, solves this problem.



Example of surge destruction



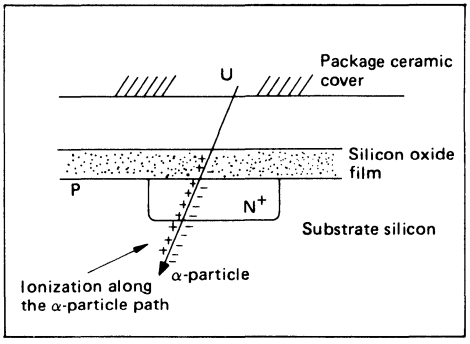
Photolithographic Defect

5) Aluminum Corrosion

Aluminum corrosion is due to electrolytic reactions caused by the presence of water and minute impurities. When aluminum dissolves, lines break. This problem is unique to the plastic capsules now used widely to reduce costs. Oki has carefully studied the possible cause and effect relationship between structure and manufacturing conditions on the one hand, and the generation of aluminum corrosion on the other. Refinements incorporated in Oki LSIs permit superior endurance to even the most severe high humidity conditions.

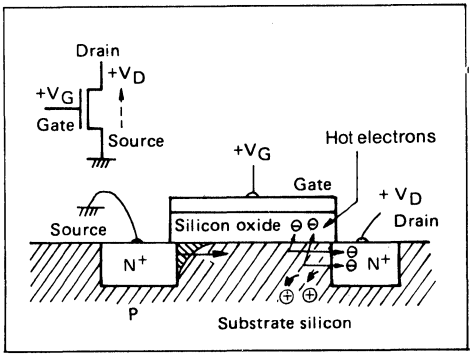
6) Alpha-Particle Soft Failure

This problem occurs when devices are highly miniaturized, such as in 1 megabit RAMs. The inversion of memory cell data by alpha-particle generated by radio-active elements like uranium and thorium (present in minute quantities, measured in ppb) in the ceramic package material causes defects. Since failure is only temporary and normal operation restored quickly, this is referred to as a "soft" failure. At Oki we have eliminated the problem by coating the chip surface of 1 megabit RAMs with a resin which effectively screens out these alpha-particles.



7) Degradation in Performance Characteristics Due to Hot Electrons

With increased miniaturization of circuit elements, internal electric field strength in the channels increases since the applied voltage remains the same at 5V. As a result, electrons flowing in the channels, as shown in the accompanying diagram, tend to enter into the oxide film near the drain, leading to degradation of performance. Although previous low-temperature operation tests have indicated an increase of this failure, we have confirmed by our low-temperature acceleration tests, including checks on test element groups, that no such problem exists in Oki LSIs.



Characteristic deterioration caused by hot electrons

With further progress in the miniaturization of circuit components, failures related to pin hole oxide film destruction and photolithography have increased. To eliminate these defects during manufacturing, Oki has been continually improving its production processes based on reliability tests and information gained from the field. And we subject all devices to high-temperature burn-in screening for 48 to 96 hours to ensure even greater reliability.

3

MOS DYNAMIC RAMS

4 MOS DYNAMIC RAMS

MSM3764A	65,536-Word x 1-Bit RAM (NMOS) <Page Mode>	69
MSM41256A	262,144-Word x 1-Bit RAM (NMOS) <Page Mode>	85
MSM41257A	262,144-Word x 1-Bit RAM (NMOS) <Nibble Mode>	100
MSM41464	65,536-Word x 4-Bits RAM (NMOS) <Page Mode>	116
MSM51C256	262,144-Word x 1-Bit RAM (CMOS)	131
MSM511000A	1,048,576-Word x 1-Bit RAM (CMOS) <Fast Page>	147
MSM511001A	1,048,576-Word x 1-Bit RAM (CMOS) <Nibble Mode>	162
MSM511002A	1,048,576-Word x 1-Bit RAM (CMOS) <Static Column>	177
MSM514256A	262,144-Word x 4-Bits RAM (CMOS) <Fast Page>	191
MSM514258A	262,144-Word x 4-Bits RAM (CMOS) <Static Column>	205
MSM514100	4,194,304-Word x 1-Bit RAM (CMOS) <Fast Page>	220
MSM514102	4,194,304-Word x 1-Bit RAM (CMOS) <Static Column>	234
MSM514400	1,048,576-Word x 4-Bits RAM (CMOS) <Fast Page>	248
MSM514402	1,048,576-Word x 4-Bits RAM (CMOS) <Static Column>	262
MSC2304YS8-KS8	262,144-Word x 8-Bits RAM (NMOS) <Page Mode> (MODULE)	277
MSC2304YS9-KS9	262,144-Word x 9-Bits RAM (NMOS) <Page Mode> (MODULE)	292
MSC2307YS9-KS9	262,144-Word x 9-Bits RAM (NMOS) <Nibble Page Mode> (MODULE)	307
MSC2312A-XXYS9/KS9	1,048,576-Word x 9-Bits RAM (CMOS) (MODULE)	321
MSC2313A-XXYS8/KS8	1,048,576-Word x 8-Bits RAM (CMOS) (MODULE)	331
MSC2320A-XXYS9	262,144-Word x 36-Bits RAM (MODULE)	341
MSC2321A-XXYS18	524,288-Word x 36-Bits RAM (MODULE)	351
MSC2328A-XXYS2/KS2	262,144-Word x 8-Bits RAM (MODULE)	360
MSC2340-XXYS9/KS9	4,159,300-Word x 9-Bits RAM (CMOS) (MODULE)	370

OKI semiconductor

MSM3764A

65,536-BIT DYNAMIC RANDOM ACCESS MEMORY (E3-S-004-32)

GENERAL DESCRIPTION

The Oki MSM3764A is a fully decoded, dynamic NMOS random access memory organized as 65536 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM3764A to be housed in a standard 16 pin DIP or 18 pin PLCC. Pin-outs conform to the JEDEC approved pin out.

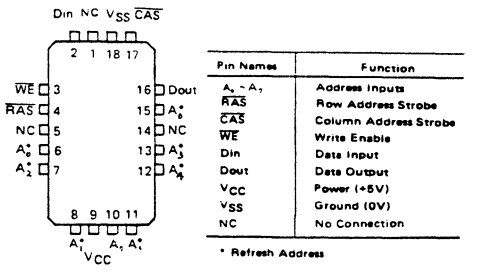
The MSM3764A is fabricated using silicon gate NMOS and Oki's advanced Double-Layer Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

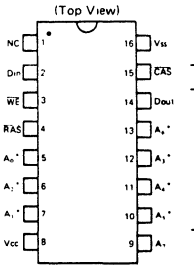
- 65,536 x 1 RAM, 16 or 18 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time,
  120 ns max (MSM3764A-12)
  150 ns max (MSM3764A-15)
- Cycle time,
  220 ns min (MSM3764A-12)
  260 ns min (MSM3764A-15)
- Low power: 330 mW active,
  28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 128 refresh cycles/2 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, and Page-Mode capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance

PIN CONFIGURATION



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)
NC	No Connection

* Refresh Address



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Din	Data Input
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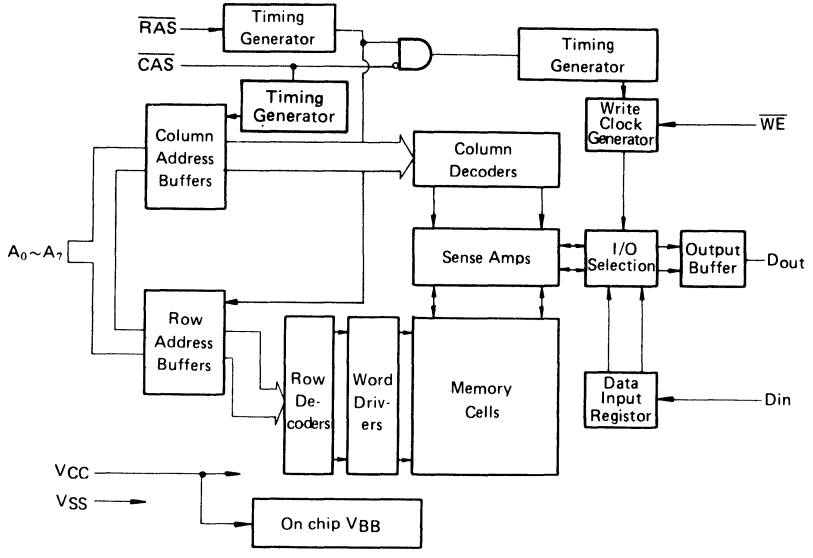
V_{SS}	Ground (0V)

* Refresh Address

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	−1.0	0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Min.	Max.	Unit	Notes
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		60	mA	
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		5.0	mA	
Refresh Current* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		40	mA	
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		60	mA	
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−10	10	μA	
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	μA	
Output Levels Output high voltage (I_{OH} = −5 mA) Output low voltage (I_{OL} = 4.2 mA)	V_{OH} V_{OL}	2.4	 0.4	V V	

Note*: ICC is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(T_a = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance (A_0 ~ A_7, D_{IN})	C_{IN1}	—	5	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	—	8	pF
Output Capacitance (D_{OUT})	C_{OUT}	—	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1,2,3

Parameter	Symbol	Units	MSM3764A-12		MSM3764A-15		Note
			Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		2		2	
Random read or write cycle time	t_{RC}	ns	220		260		
Read-write cycle time	t_{RWC}	ns	245		280		
Page mode cycle time	t_{PC}	ns	120		145		
Access time from $\overline{RAS}$	t_{RAC}	ns		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	35	0	40	
Transition time	t_T	ns	3	35	3	35	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	120	10,000	150	10,000	
$\overline{RAS}$ hold time	t_{RSH}	ns	60		75		
$\overline{CAS}$ precharge time (Page cycle)	t_{CP}	ns	50		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	60	10,000	75	10,000	
$\overline{CAS}$ hold time	t_{CSH}	ns	120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	ns	0		0		
Row Address set-up time	t_{ASR}	ns	0		0		
Row Address hold time	t_{RAH}	ns	15		15		
Column Address set-up time	t_{ASC}	ns	0		0		
Column Address hold time	t_{CAH}	ns	20		20		
Column Address hold time referenced to $\overline{RAS}$	t_{AR}	ns	80		95		
Read command set-up time	t_{RCS}	ns	0		0		
Read command hold time	t_{RCH}	ns	0		0		
Write command set-up time	t_{WCS}	ns	−10		−10		8
Write command hold time	t_{WCH}	ns	40		45		
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	ns	100		120		
Write command pulse width	t_{WP}	ns	40		45		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	40		45		
Data-in set-up time	t_{DS}	ns	0		0		
Data-in hold time	t_{DH}	ns	40		45		
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	ns	100		120		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	40		45		8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	100		120		8
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	0		0		
$\overline{CAS}$ precharge time	t_{CPN}	ns	30		35		

NOTES: 1) An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Examples; $\overline{RAS}$ only) before proper device operation is achieved.

2) AC measurements assume t_T = 5 ns.

3) V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4) Assumes that $t_{RCD} < t_{RCD}$ (max.).
If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

5) Assumes that $t_{RCD} < t_{RCD}$ (max.)

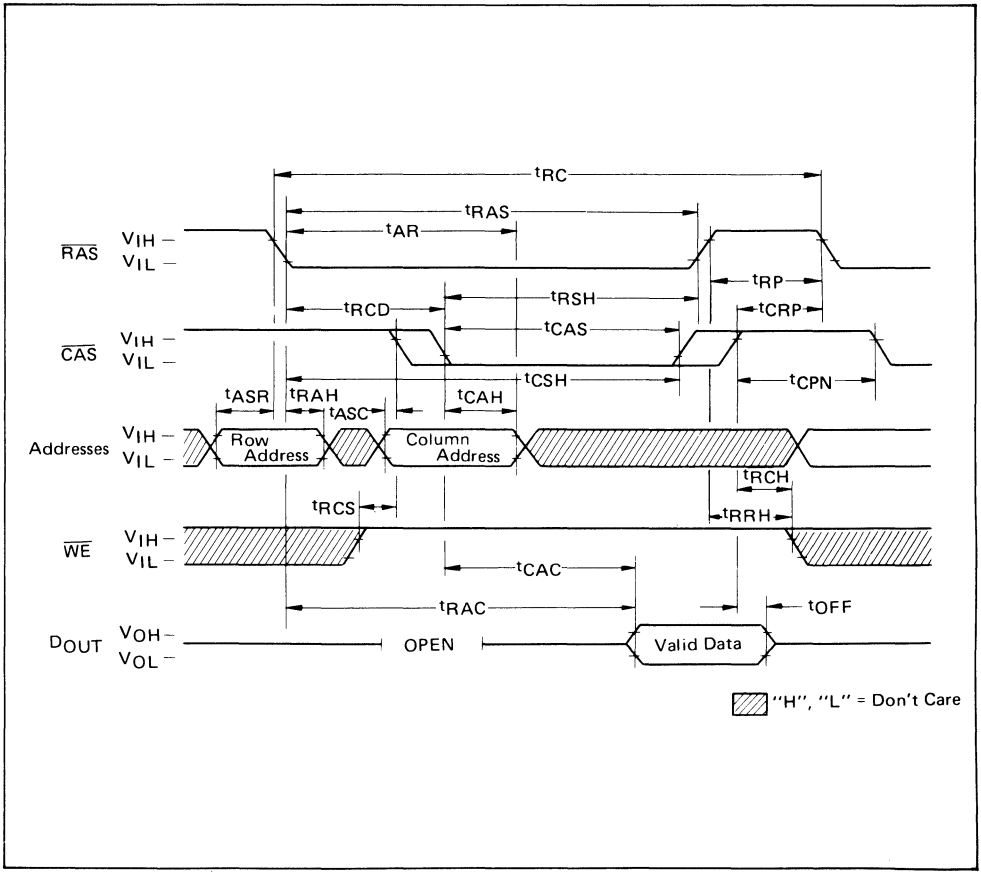
6) Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

7) Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

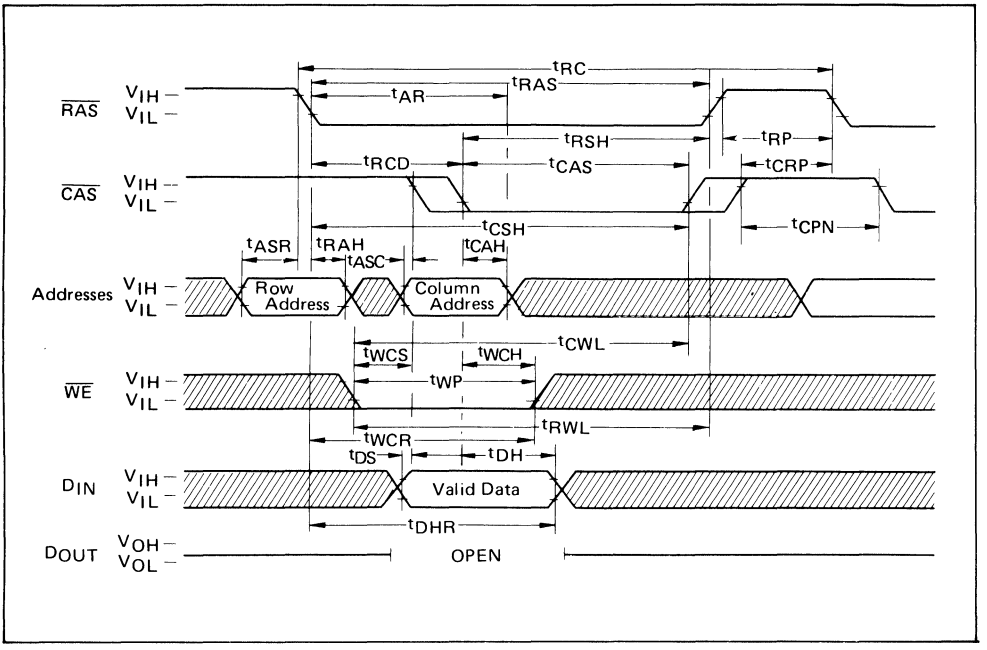
8) t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.) and $t_{RWD} > t_{RWD}$ (min.) the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

4

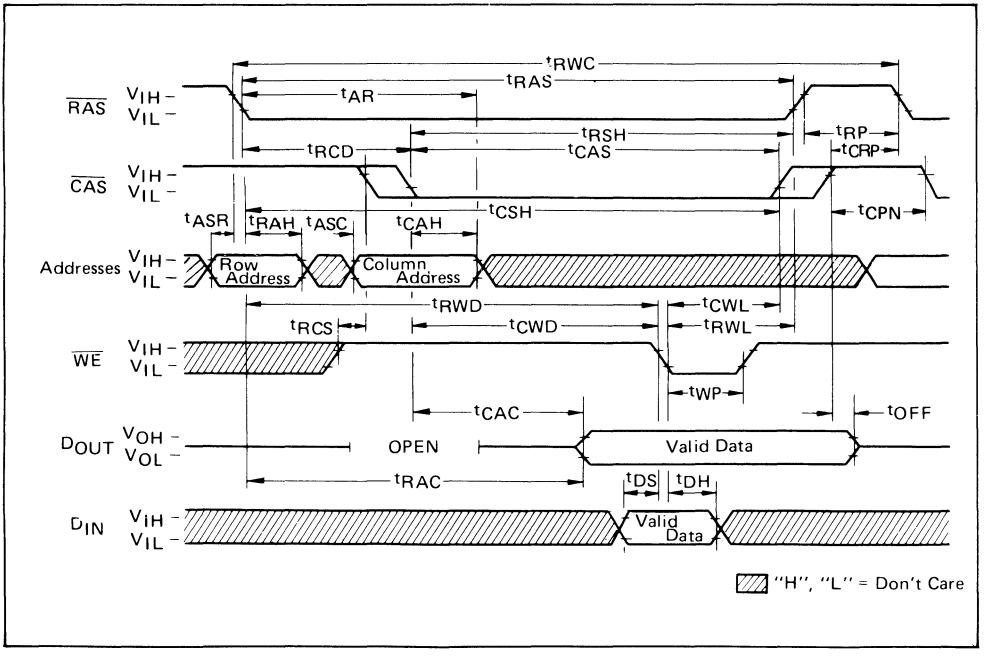
READ CYCLE TIMING



WRITE CYCLE TIMING
(EARLY WRITE)

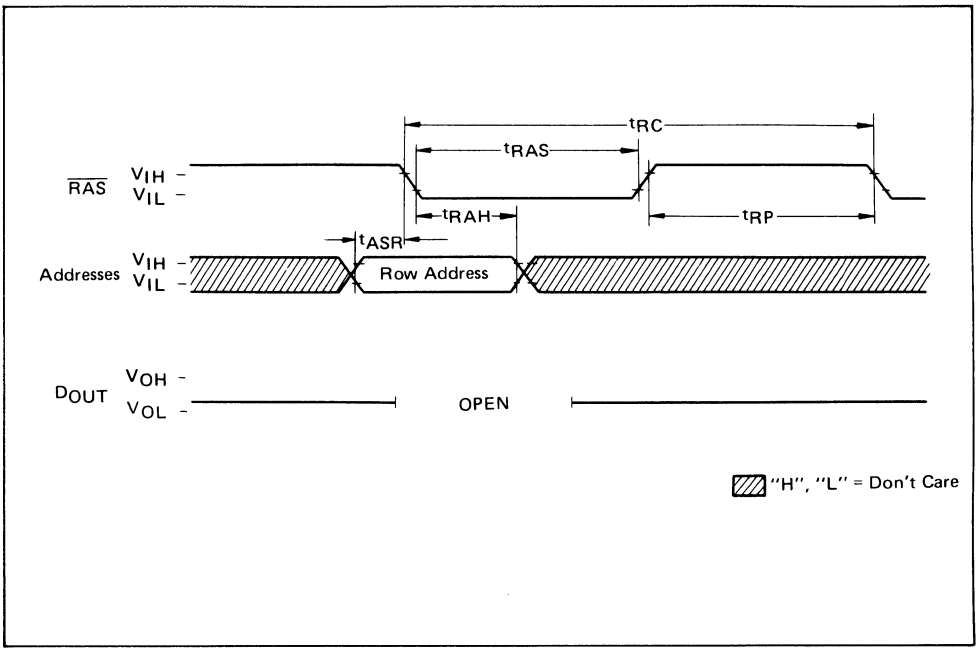


READ-WRITE/READ-MODIFY-WRITE CYCLE

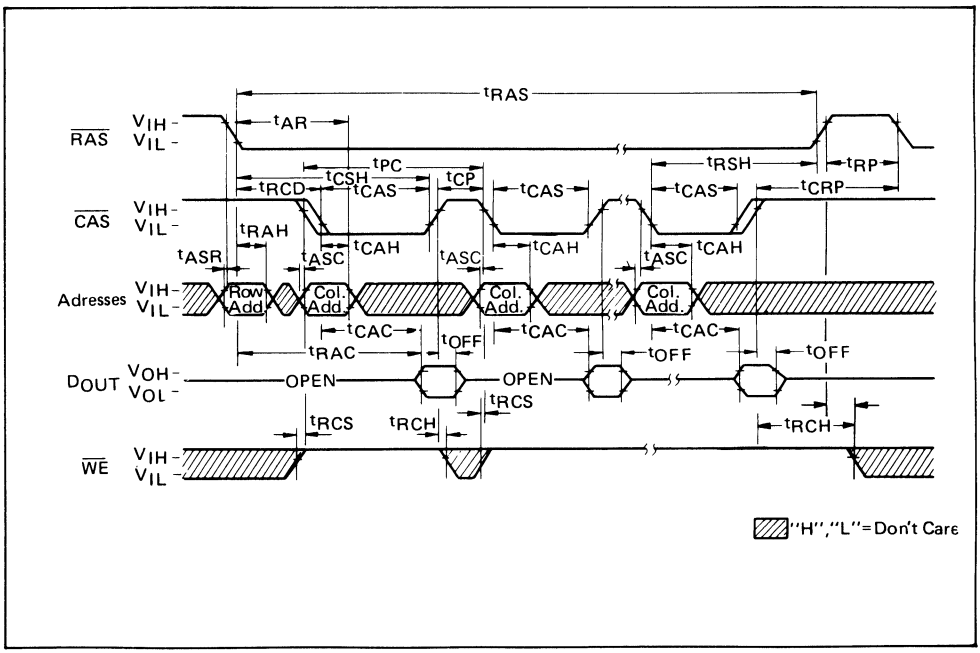


$\overline{RAS}$ ONLY REFRESH TIMING

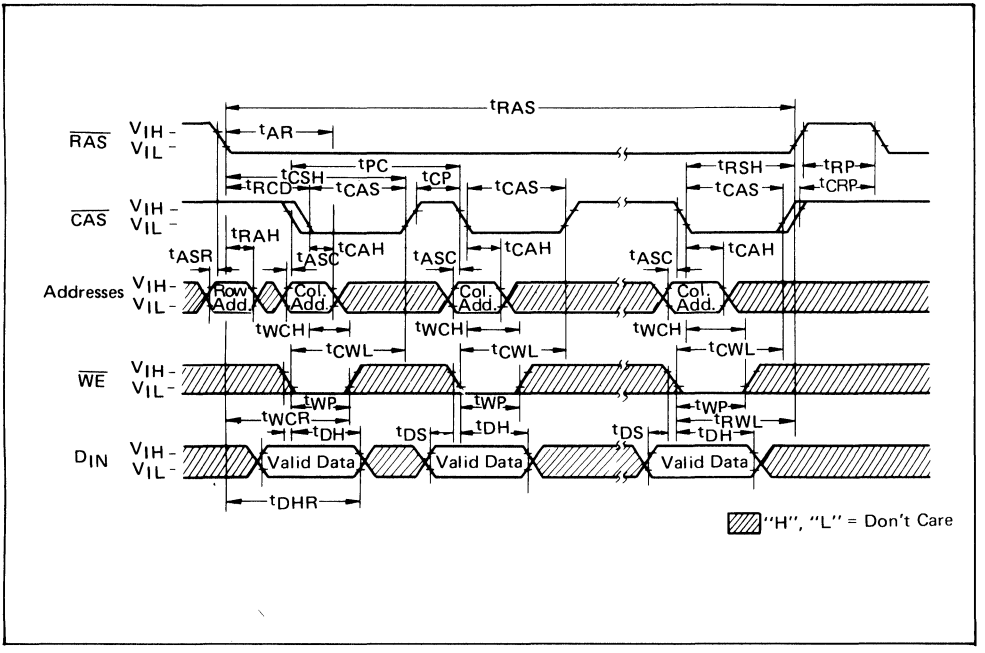
($\overline{CAS}$: V_{IH}, $\overline{WE}$ & D_{IN}: Don't care)



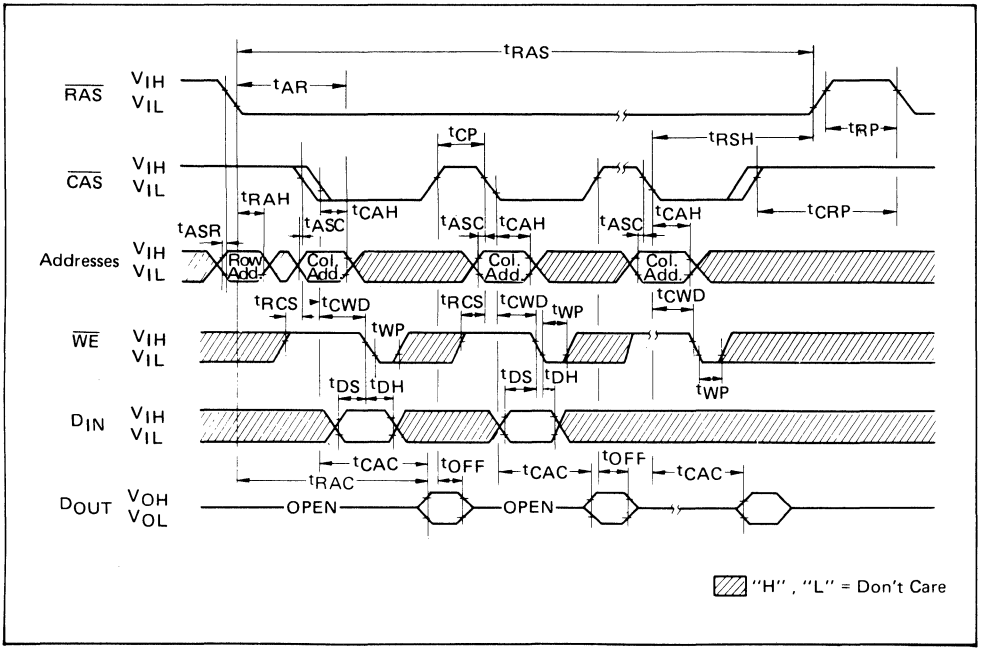
PAGE MODE READ CYCLE



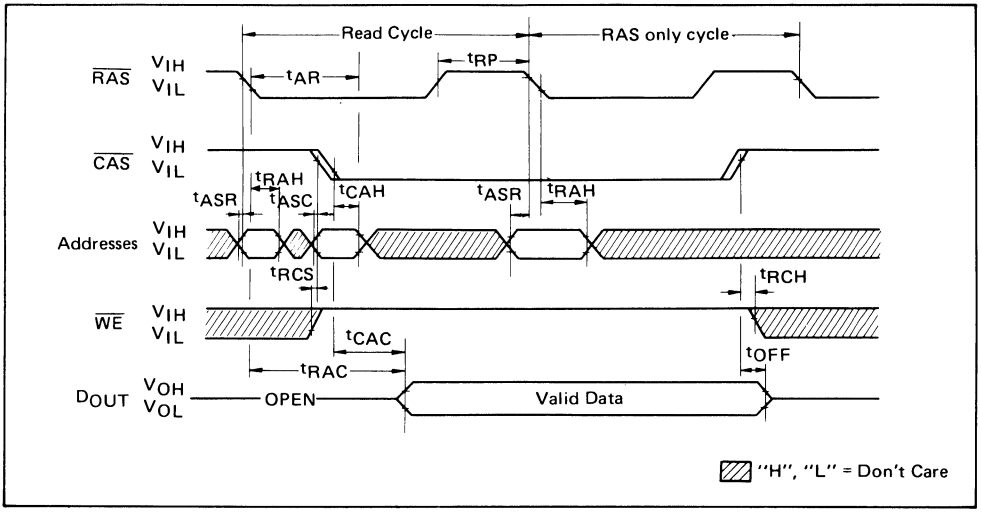
PAGE MODE WRITE CYCLE



PAGE MODE, READ-MODIFY-WRITE CYCLE



HIDDEN REFRESH



DESCRIPTION

Address Inputs:

A total of sixteen binary input address bits are required to decode any 1 of 65536 storage cell locations within the MSM3764A. Eight row-address bits are established on the input pins ($A_0 \sim A_7$) and latched with the Row Address Strobe ($\overline{RAS}$). The eight column-address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. A logic high (1) on $\overline{WE}$ dictates read mode; logic low (0) dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM3764A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transistion. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in a high impedance state until $\overline{CAS}$ is brought low. In a read cycle, or read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max.) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to a high level. In a write cycle the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address into the MSM3764A while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

Refresh:

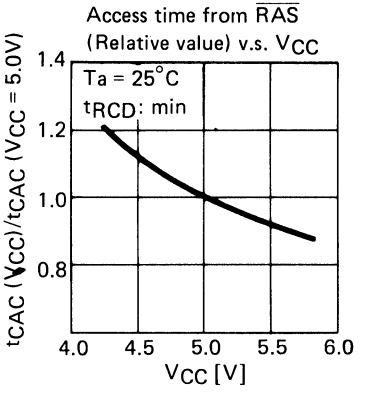
Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 128 row-addresses ($A_0 \sim A_6$) at least every two milliseconds. During refresh, either V_{IL} or V_{IH} is permitted for A_7. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 128 row-addresses with $\overline{RAS}$ will cause all bits in each rwo to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

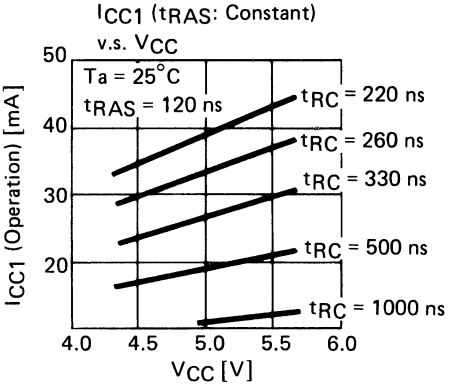
Hidden Refresh:

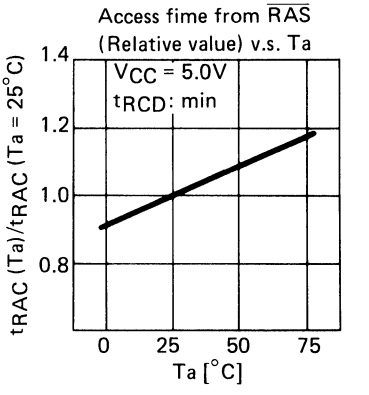
$\overline{RAS}$ ONLY REFRESH CYCLE may take place while maintaining valid output data. This feature is referred to as Hidden Refresh.

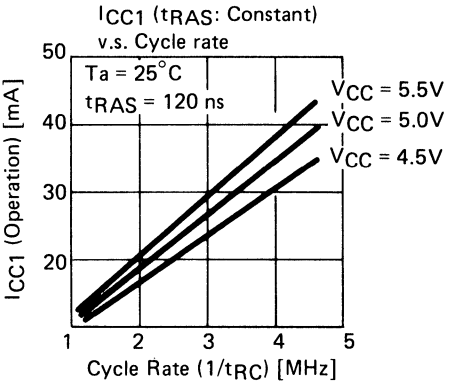
Hidden Refresh is performed by holding $\overline{CAS}$ as V_{IL} from a previous memory read cycle.

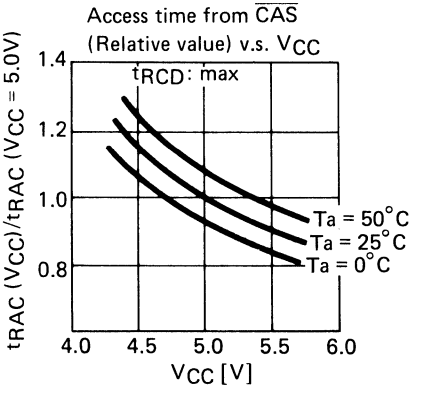
TYPICAL CHARACTERISTICS

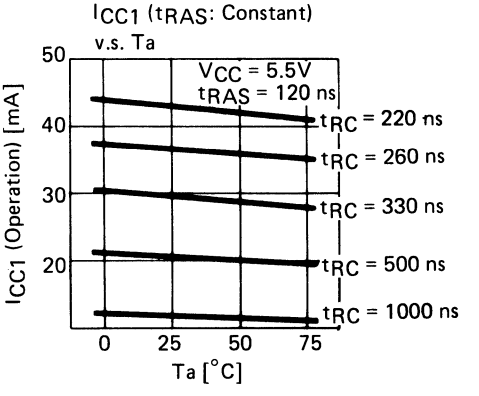


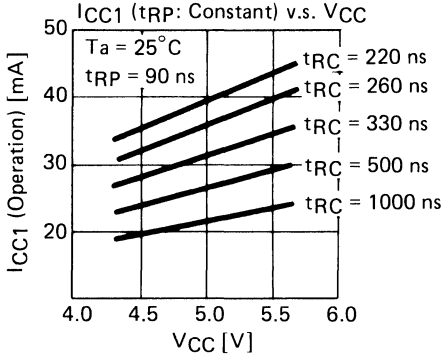


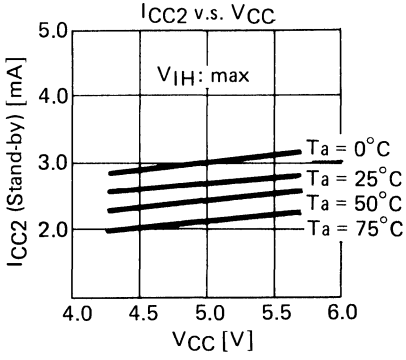


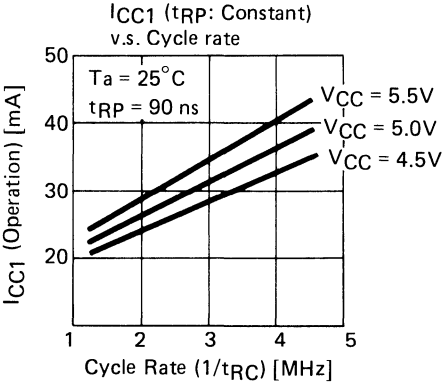


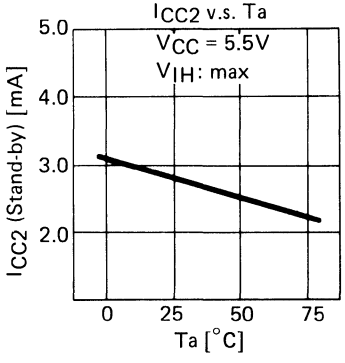


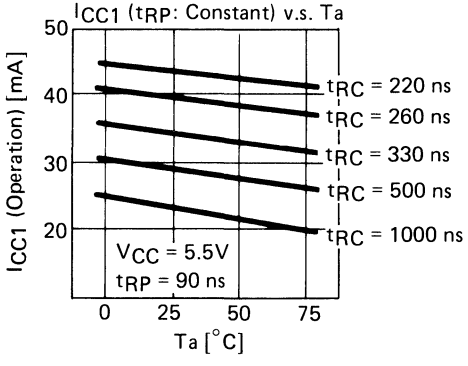



ICC1 (tRP: Constant) v.s. VCC
Ta = 25°C
tRP = 90 ns
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
ICC1 (Operation) [mA]
50
40
30
20
4.0
4.5
5.0
5.5
6.0
VCC [V]

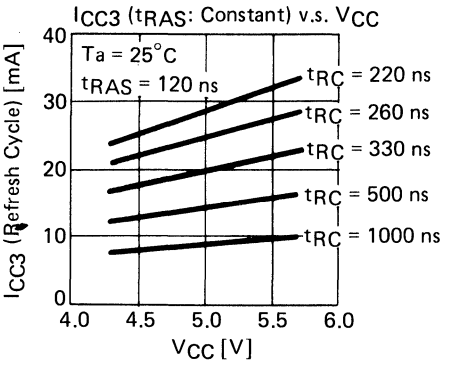

ICC2 v.s. VCC
VIH: max
Ta = 0°C
Ta = 25°C
Ta = 50°C
Ta = 75°C
ICC2 (Stand-by) [mA]
5.0
4.0
3.0
2.0
4.0
4.5
5.0
5.5
6.0
VCC [V]

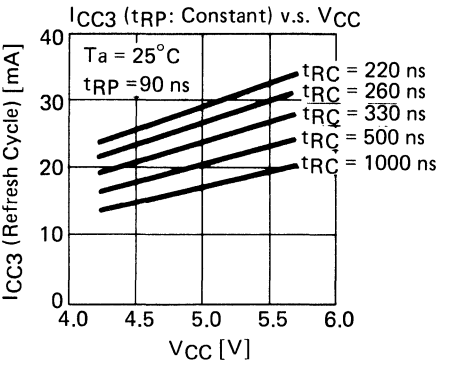

ICC1 (tRP: Constant)
v.s. Cycle rate
Ta = 25°C
tRP = 90 ns
VCC = 5.5V
VCC = 5.0V
VCC = 4.5V
ICC1 (Operation) [mA]
50
40
30
20
1
2
3
4
5
Cycle Rate (1/tRC) [MHz]

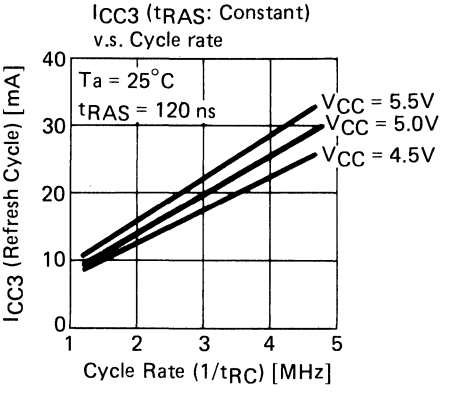

ICC2 v.s. Ta
VCC = 5.5V
VIH: max
ICC2 (Stand-by) [mA]
5.0
4.0
3.0
2.0
0
25
50
75
Ta [°C]

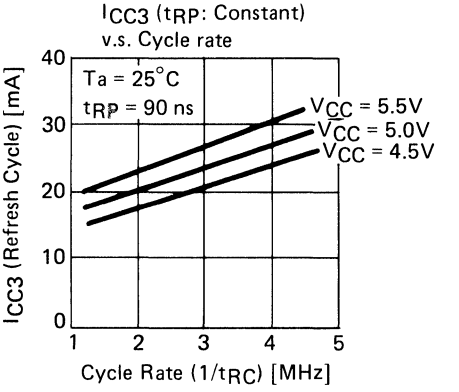

ICC1 (tRP: Constant) v.s. Ta
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
VCC = 5.5V
tRP = 90 ns
ICC1 (Operation) [mA]
50
40
30
20
0
25
50
75
Ta [°C]

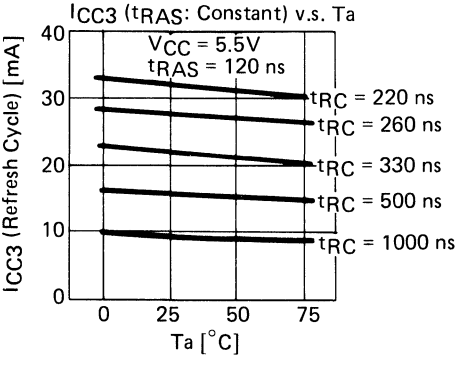
4

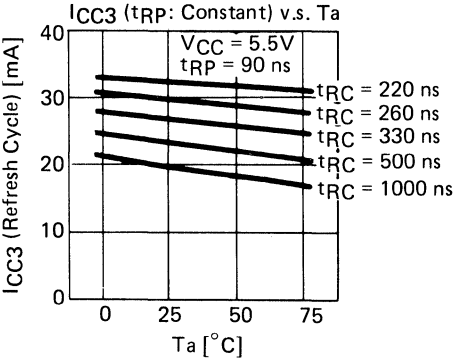

ICC3 (tRAS: Constant) v.s. VCC
Ta = 25°C
tRAS = 120 ns
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
ICC3 (Refresh Cycle) [mA]
VCC [V]


ICC3 (tRP: Constant) v.s. VCC
Ta = 25°C
tRP = 90 ns
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
ICC3 (Refresh Cycle) [mA]
VCC [V]

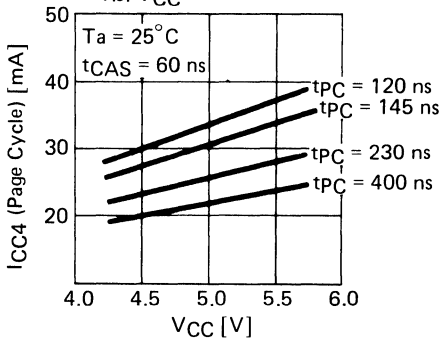

ICC3 (tRAS: Constant)
v.s. Cycle rate
Ta = 25°C
tRAS = 120 ns
VCC = 5.5V
VCC = 5.0V
VCC = 4.5V
ICC3 (Refresh Cycle) [mA]
Cycle Rate (1/tRC) [MHz]


ICC3 (tRP: Constant)
v.s. Cycle rate
Ta = 25°C
tRP = 90 ns
VCC = 5.5V
VCC = 5.0V
VCC = 4.5V
ICC3 (Refresh Cycle) [mA]
Cycle Rate (1/tRC) [MHz]

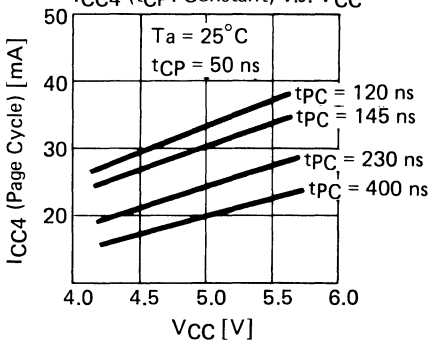

ICC3 (tRAS: Constant) v.s. Ta
VCC = 5.5V
tRAS = 120 ns
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
ICC3 (Refresh Cycle) [mA]
Ta [°C]


ICC3 (tRP: Constant) v.s. Ta
VCC = 5.5V
tRP = 90 ns
tRC = 220 ns
tRC = 260 ns
tRC = 330 ns
tRC = 500 ns
tRC = 1000 ns
ICC3 (Refresh Cycle) [mA]
Ta [°C]

I_{CC4} (t_{CAS}: Constant) v.s. V_{CC}

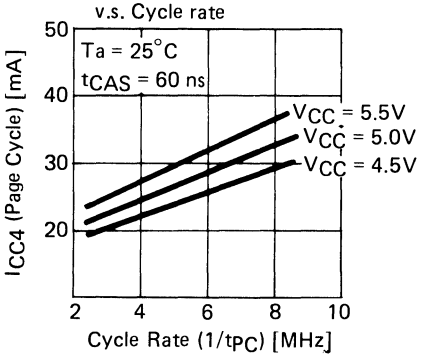


I_{CC4} (t_{CP}: Constant) v.s. V_{CC}

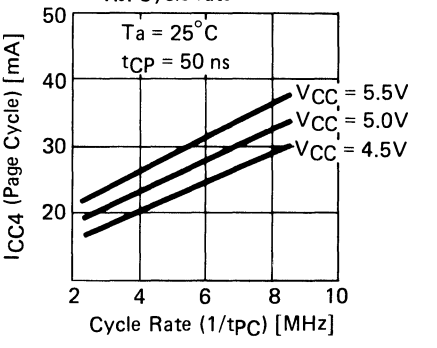


4

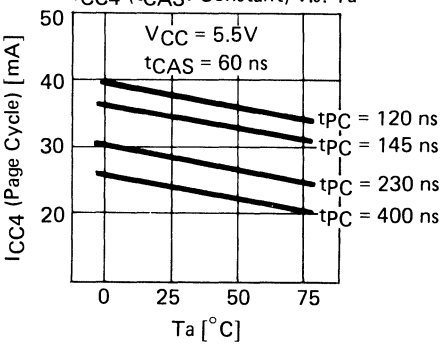
I_{CC4} (t_{CAS}: Constant) v.s. Cycle rate



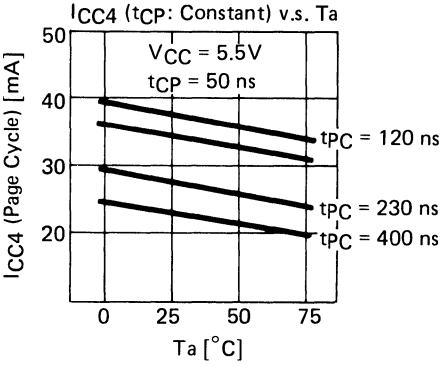
I_{CC4} (t_{CP}: Constant) v.s. Cycle rate



I_{CC4} (t_{CAS}: Constant) v.s. Ta

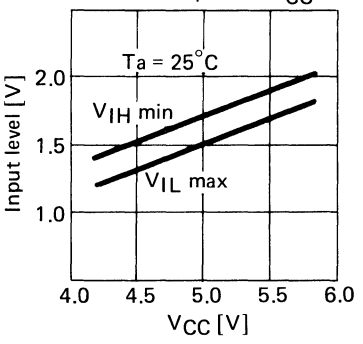


I_{CC4} (t_{CP}: Constant) v.s. Ta

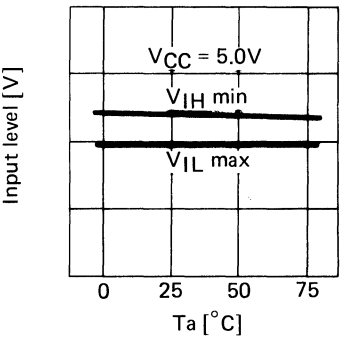


4

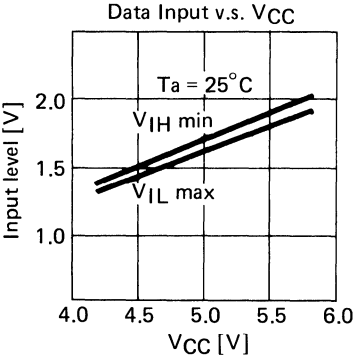
Address Input v.s. V_{CC}



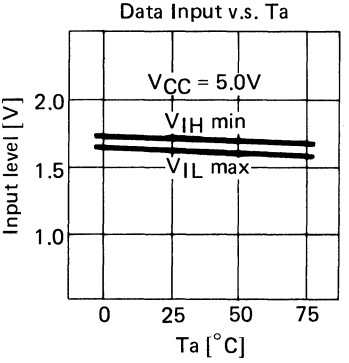
Address Input v.s. Ta



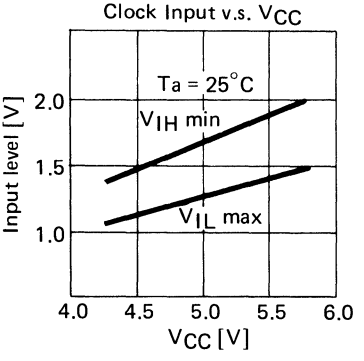
Data Input v.s. V_{CC}



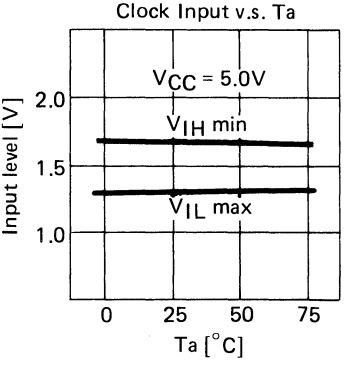
Data Input v.s. Ta



Clock Input v.s. V_{CC}

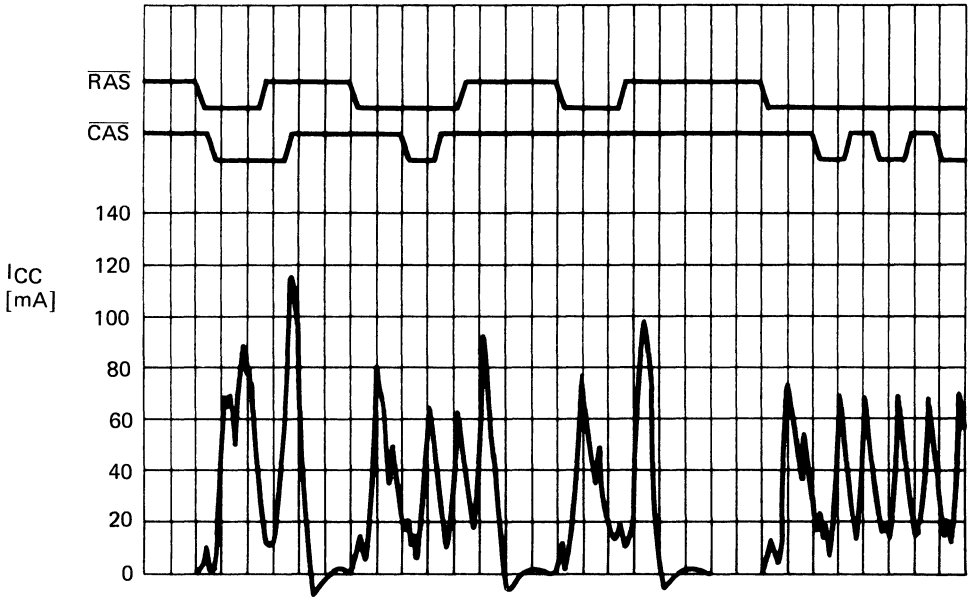


Clock Input v.s. Ta



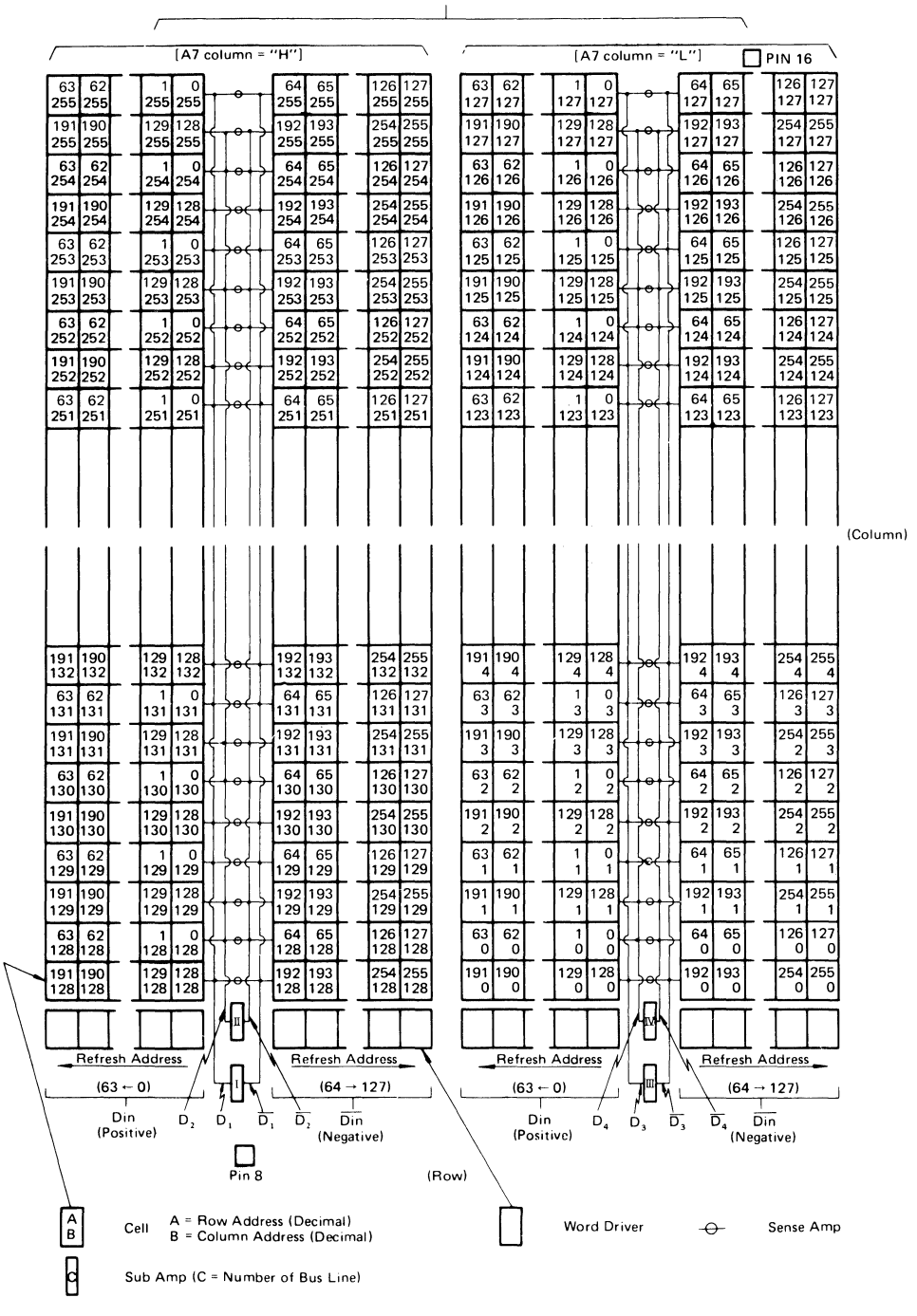
V_{CC} = 5.5V
Ta = 25°C
50 ns/div

RAS/CAS CYCLE, LONG RAS/CAS CYCLE, RASONLY CYCLE, PAGE MODE CYCLE



4

MSM3764A Bit MAP (Physical-Decimal)



OKI semiconductor

MSM41256A

262,144-BIT DYNAMIC RANDOM ACCESS MEMORY <Page Mode Type>

GENERAL DESCRIPTION

The Oki MSM41256A is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM41256A to be housed in a standard 16 pin DIP or 18 pin PLCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM 41256A offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability.

The MSM41256A is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

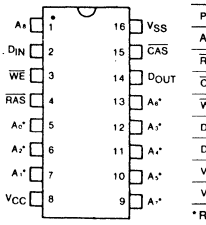
Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

4

FEATURES

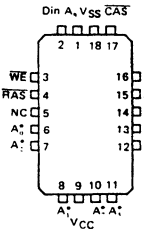
- 262,144 × 1 RAM, 16 or 18 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  - 100 ns max (MSM41256A-10)
  - 120 ns max (MSM41256A-12)
  - 150 ns max (MSM41256A-15)
- Cycle time:
  - 200 ns min (MSM41256A-10)
  - 220 ns min (MSM41256A-12)
  - 260 ns min (MSM41256A-15)
- Low power:
  - 330 mW active (MSM41256A-10)
  - 303 mW active (MSM41256A-12)
  - 275 mW active (MSM41256A-15)
  - 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 256 refresh cycles/4 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Page Mode" capability

PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

* Refresh Address

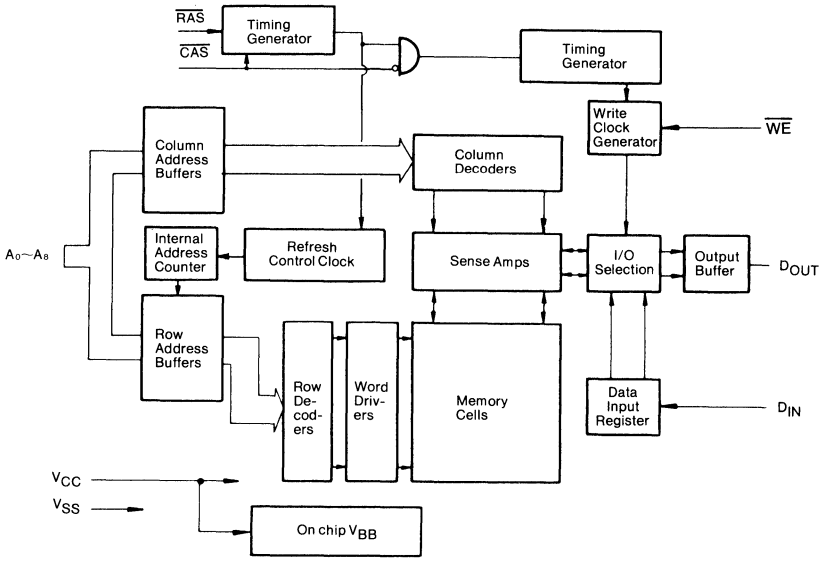


Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)
NC	No Connection

* Refresh Address

4

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Parmanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	MSM41256A-10	I_{CC1}		60	mA	
	MSM41256A-12			55		
	MSM41256A-15			50		
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		5.0	mA	
REFRESH CURRENT 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MSM41256A-10	I_{CC3}		55	mA	
	MSM41256A-12			50		
	MSM41256A-15			45		
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	MSM41256A-10	I_{CC4}		40	mA	
	MSM41256A-12			35		
	MSM41256A-15			30		
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	MSM41256A-10	I_{CC5}		55	mA	
	MSM41256A-12			50		
	MSM41256A-15			45		
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)		I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = −5 mA)		V_{OH}	2.4		V	
Output low voltage (I_{OL} = 4.2 mA)		V_{OL}		0.4	V	

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input capacitance ($A_0 \sim A_8$, D_{IN})	C_{IN1}	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	7	pF
Output capacitance (D_{OUT})	C_{OUT}	–	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSM41256A-10		MSM41256A-12		MSM41256A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Read-write cycle time	t_{RWC}	ns	205		225		260		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	30	0	30	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		0		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		20		20		
Write command set-up time	t_{WCS}	ns	0		0		0		8

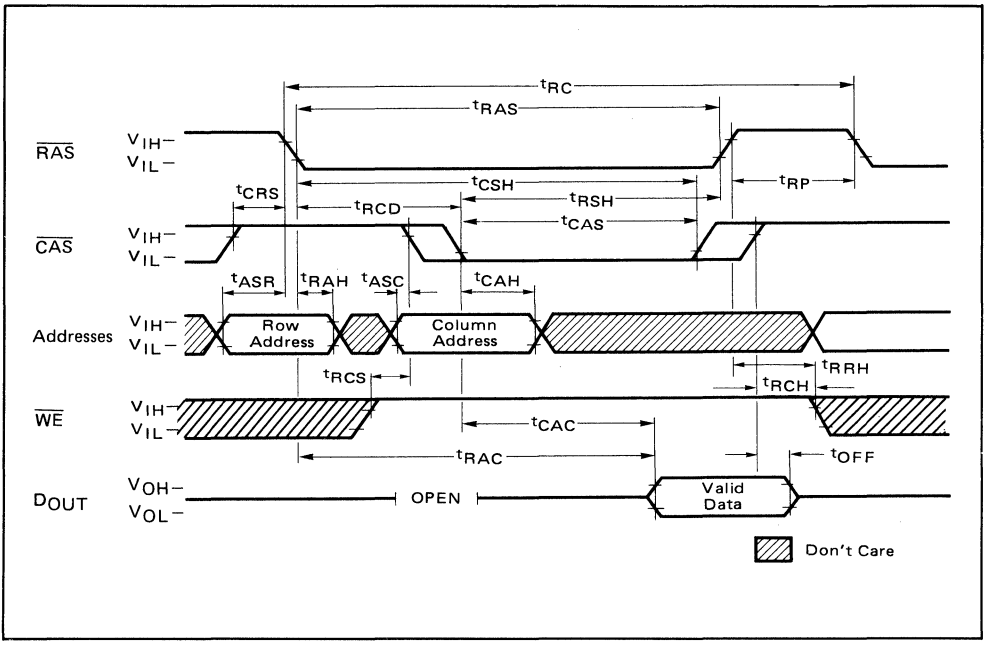
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41256A-10		MSM41256A-12		MSM41256A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	15		20		25		
Write command hold time	t_{WCH}	ns	15		20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		20		25		
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	ns	15		20		25		8
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		30		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		20		
Page mode cycle time	t_{PC}	ns	100		120		145		9
Page mode read write cycle time	t_{PRWC}	ns	105		125		145		9
Page mode $\overline{CAS}$ precharge time	t_{CP}	ns	40		50		60		9
Refresh counter test cycle time	t_{RTC}	ns	315		355		415		10
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	ns	215	10μs	255	10μs	305	10μs	10
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	ns	50		60		70		10

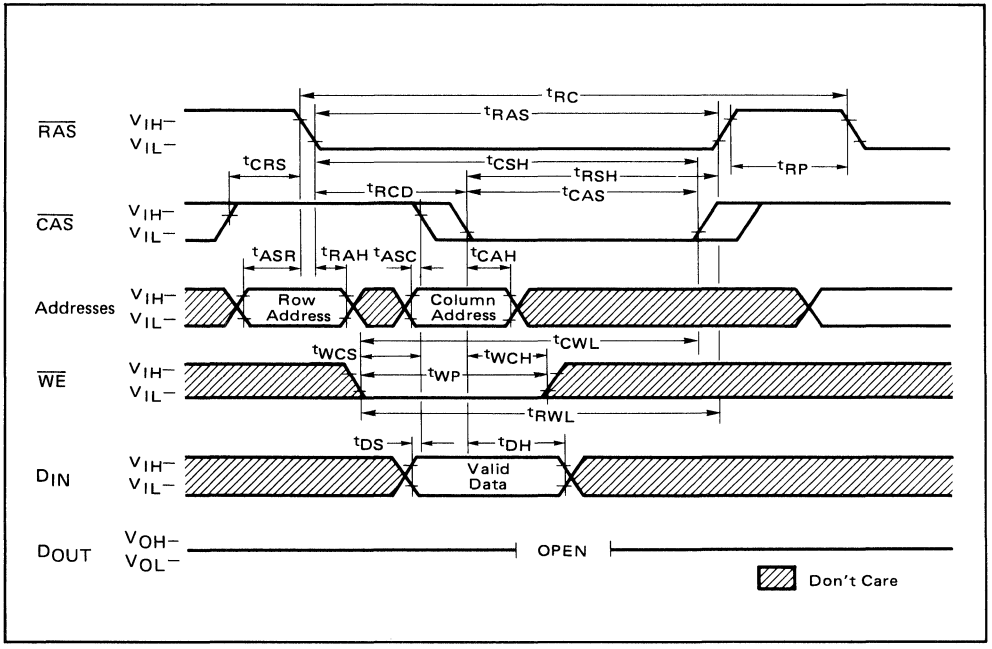
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 RAS cycles (Example: RAS only) before proper device operation is achieved.
2. The AC measurements assume $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. Page mode cycle.
10. $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle only.

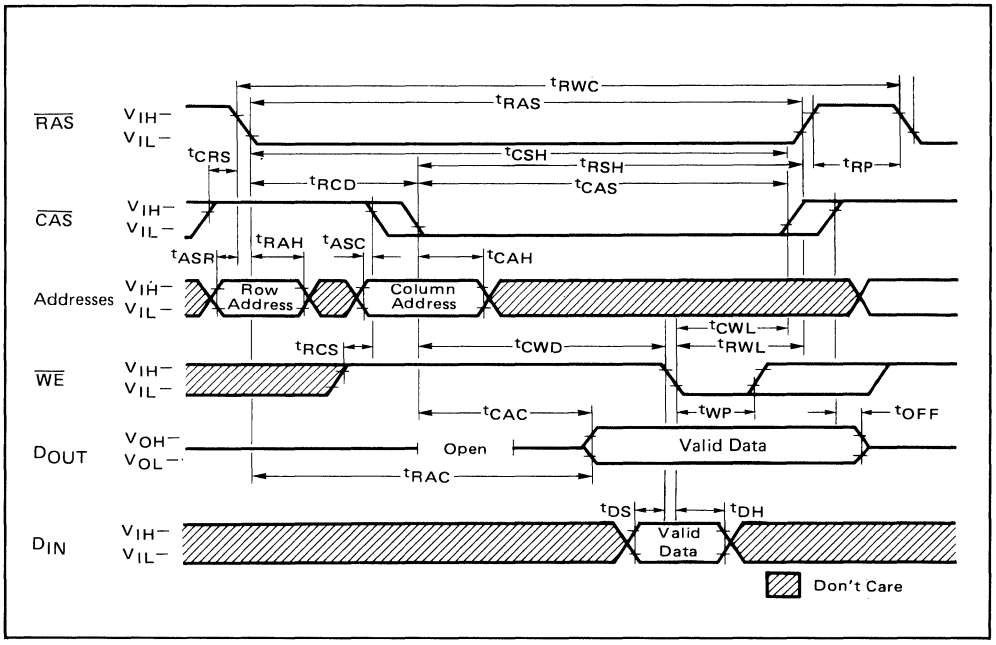
READ CYCLE



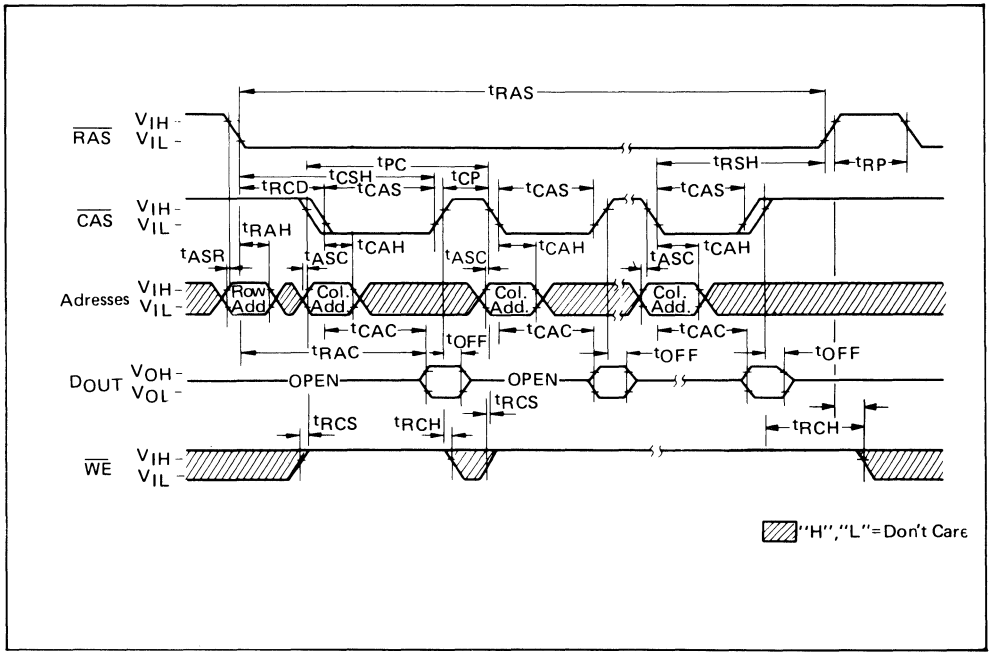
WRITE CYCLE (EARLY WRITE)



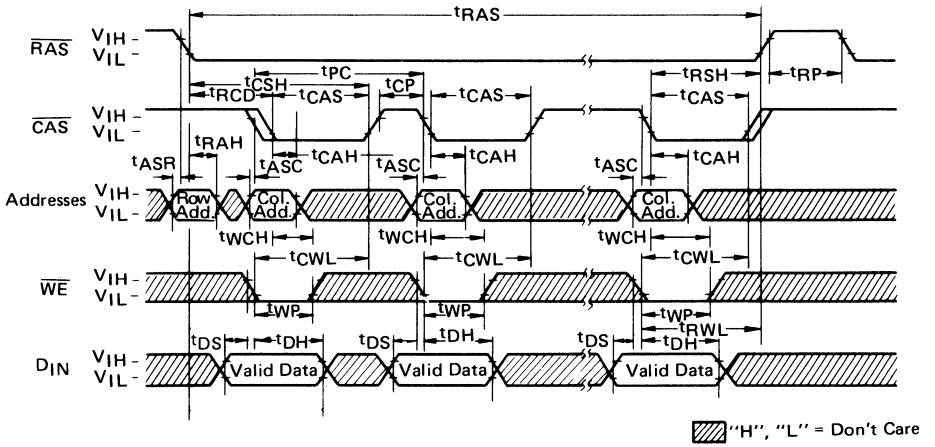
READ-WRITE/READ-MODIFY-WRITE CYCLE



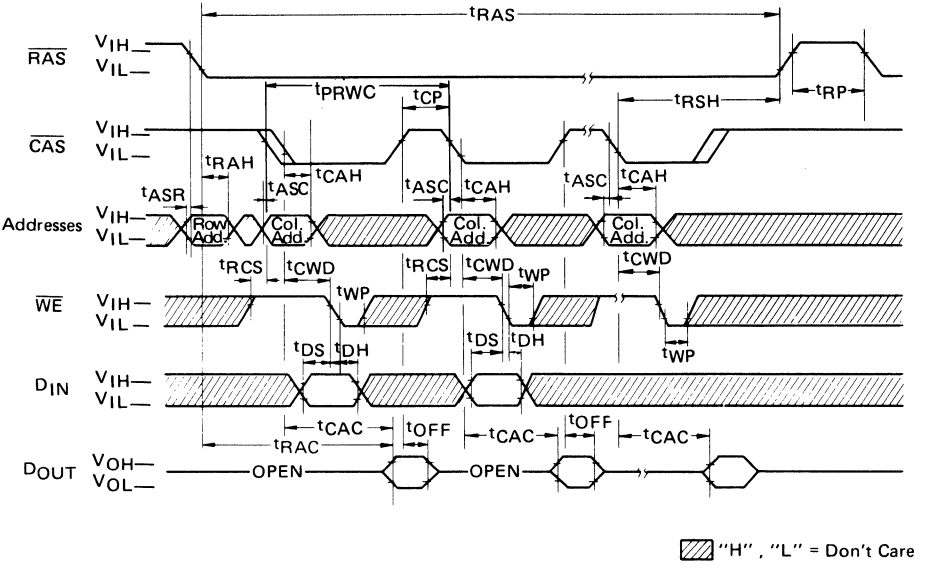
PAGE MODE READ CYCLE



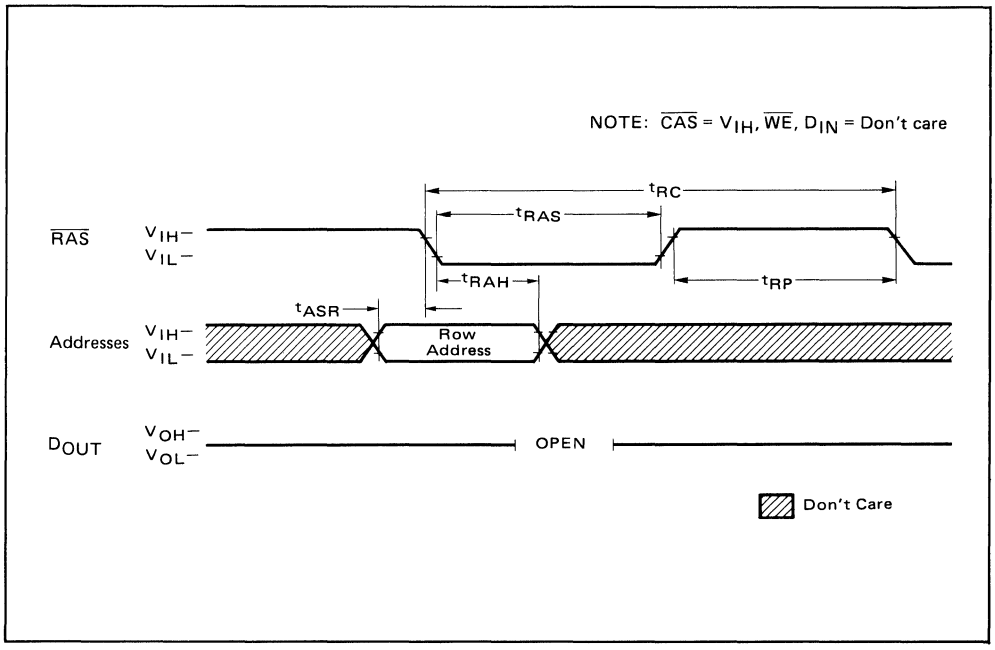
PAGE MODE WRITE CYCLE



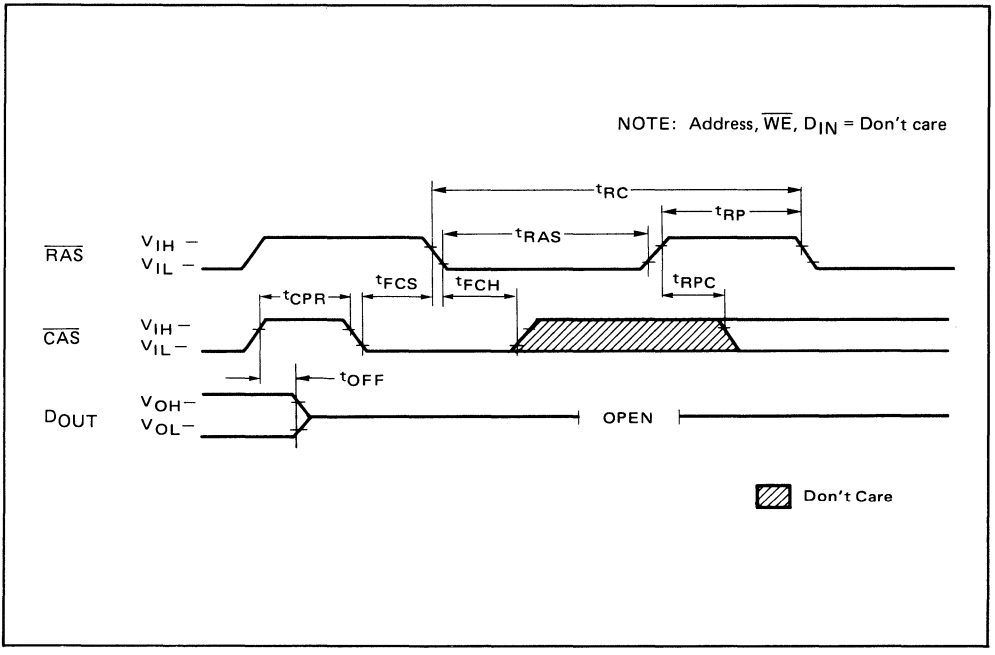
PAGE MODE, READ-MODIFY-WRITE CYCLE



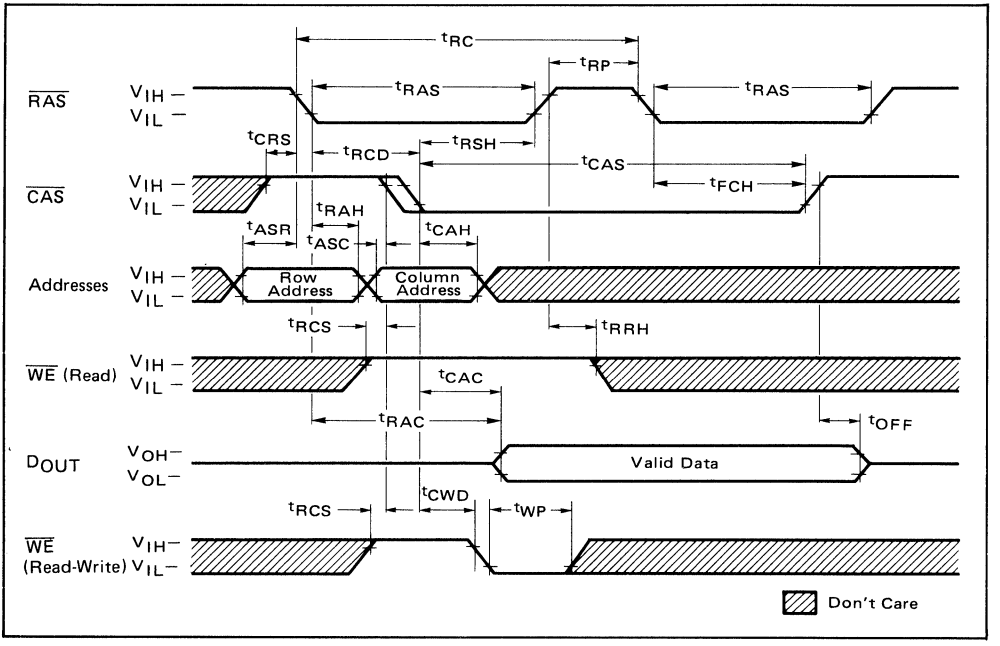
$\overline{RAS}$ ONLY REFRESH CYCLE



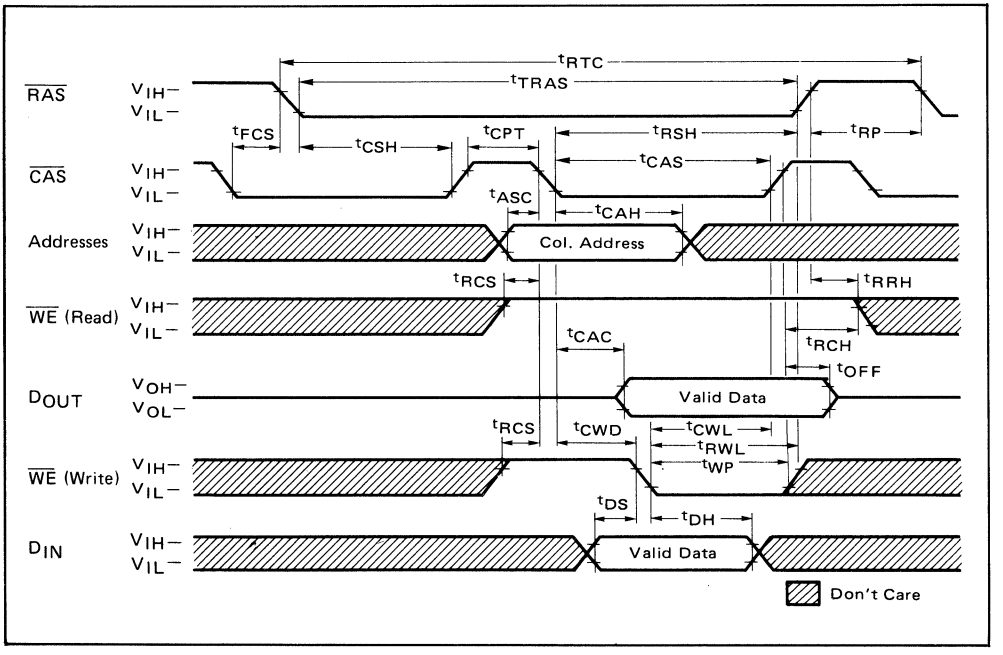
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Simple Timing Requirements:

The MSM41256A has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSM41256A can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSM41256A has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). And the MSM41256A can commit better memory system through-put during operations in an interleaved system. Furthermore, Oki has made timing requirements referenced to $\overline{RAS}$ non-restrictive and deleted from the data sheet, which includes t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. Therefore, the hold times of the Column Address D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not restricted by t_{RCD}.

Fast Read- While-Write Cycle:

The MSM41256A has the fast read while write cycle which is achieved by excellent control of the three-state output buffer in addition to the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MSM41256A goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MSM41256A goes to delayed write mode where the output contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, very fast read write cycle becomes available.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSM41256A. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM41256A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSM41256A offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSM41256A hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.
* A COLUMN ADDRESS
  - All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of CAS.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

MSM41256A Bit Map (Physical-Decimal)

□ Pin 16

252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
128	128	128	128		128	128	128	128		128	128	128	128		128	128	128	128
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
384	384	384	384		384	384	384	384		384	384	384	384		384	384	384	384
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
129	129	129	129		129	129	129	129		129	129	129	129		129	129	129	129
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
385	385	385	385		385	385	385	385		385	385	385	385		385	385	385	385
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
254	254	254	254		254	254	254	254		254	254	254	254		254	254	254	254
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
510	510	510	510		510	510	510	510		510	510	510	510		510	510	510	510
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
255	255	255	255		255	255	255	255		255	255	255	255		255	255	255	255
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
511	511	511	511		511	511	511	511		511	511	511	511		511	511	511	511

COLUMN DECODER

ROW DECODER

ROW DECODER

252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
383	383	383	383		383	383	383	383		383	383	383	383		383	383	383	383
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
127	127	127	127		127	127	127	127		127	127	127	127		127	127	127	127
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
382	382	382	382		382	382	382	382		382	382	382	382		382	382	382	382
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
126	126	126	126		126	126	126	126		126	126	126	126		126	126	126	126
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
257	257	257	257		257	257	257	257		257	257	257	257		257	257	257	257
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
1	1	1	1		1	1	1	1		1	1	1	1		1	1	1	1
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
256	256	256	256		256	256	256	256		256	256	256	256		256	256	256	256
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
0	0	0	0		0	0	0	0		0	0	0	0		0	0	0	0

COLUMN DECODER

A8 ROW = "L"
REFRESH ADDRESS
(0 – 255)

A8 ROW = "H"
REFRESH ADDRESS
(0 – 255)

□
Pin 8

A
B

: CELL

A = ROW ADDRESS (DECIMAL)
B = COLUMN ADDRESS (DECIMAL)

ROW ADDRESS
8N+6, 8N+7, 8N, 8N+1
8N+2, 8N+3, 8N+4, 8N+5
8N+6, 8N+7, 8N, 8N+1
8N+2, 8N+3, 8N+4, 8N+5
N=0, 1, 2, ·····63

COLUMN ADDRESS
2N : POSITIVE
2N : NEGATIVE
2N+1 : NEGATIVE
2N+1 : POSITIVE
N=0, 1, 2, ·····255

MSM41257A

262,144-BIT DYNAMIC RANDOM ACCESS MEMORY <Nibble Mode Type>

GENERAL DESCRIPTION

The Oki MSM41257A is a fully decoded, dynamic NMOS random access memory organized as 262144 one-bit words. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM41257A to be housed in a standard 16 pin DIP or 18 pin PLCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41257A offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability.
high speed serial access to up to 4 bits of data.

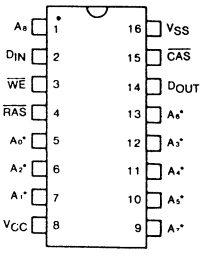
The MSM41257A is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

FEATURES

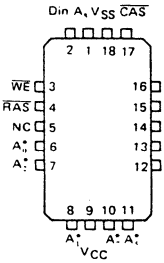
- 262,144 × 1 RAM, 16 or 18 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  - 100 ns max (MSM41257A-10)
  - 120 ns max (MSM41257A-12)
  - 150 ns max (MSM41257A-15)
- Cycle time:
  - 200 ns min (MSM41257A-10)
  - 220 ns min (MSM41257A-12)
  - 260 ns min (MSM41257A-15)
- Low power:
  - 330 mW active (MSM41257A-10)
  - 303 mW active (MSM41257A-12)
  - 275 mW active (MSM41257A-15)
  - 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" CAS
- 256 refresh cycles/4 ms
- Common I/O capability using "Early Write" operation
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Nibble Mode" capability

PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)

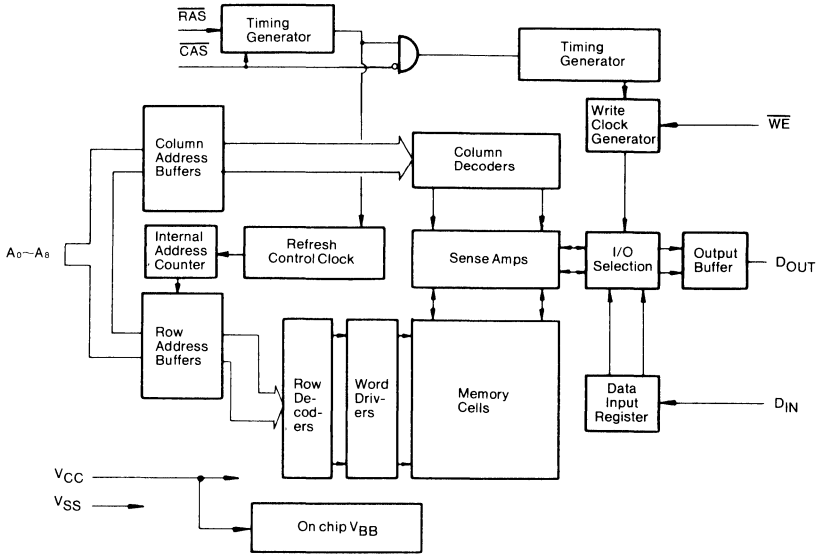
* Refresh Address



Pin Names	Function
$A_0 \sim A_8$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
Din	Data Input
Dout	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground (0V)
NC	No Connection

* Refresh Address

FUNCTIONAL BLOCK DIAGRAM



4

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Parmanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

4

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	MSM41257A-10	I_{CC1}		60	mA	
	MSM41257A-12			55		
	MSM41257A-15			50		
STANDBY CURRENT Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		5.0	mA	
REFRESH CURRENT 1 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MSM41257A-10	I_{CC3}		55	mA	
	MSM41257A-12			50		
	MSM41257A-15			45		
NIBBLE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{NC} = min.)	MSM41257A-10	I_{CC4}		30	mA	
	MSM41257A-12			27		
	MSM41257A-15			25		
REFRESH CURRENT 2 Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	MSM41257A-10	I_{CC5}		55	mA	
	MSM41257A-12			50		
	MSM41257A-15			45		
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)		I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = −5 mA)		V_{OH}	2.4		V	
Output low voltage (I_{OL} = 4.2 mA)		V_{OL}		0.4	V	

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE
(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input capacitance ($A_0 \sim A_8$, D_{IN})	C_{IN1}	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	7	pF
Output capacitance (D_{OUT})	C_{OUT}	–	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSM41257A-10		MSM41257A-12		MSM41257A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Read-write cycle time	t_{RWC}	ns	205		225		260		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	30	0	30	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		0		
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	ns	20		20		20		
Write command set-up time	t_{WCS}	ns	0		0		0		8

AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41257A-10		MSM41257A-12		MSM41257A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	15		20		25		
Write command hold time	t_{WCH}	ns	15		20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		20		25		
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	ns	15		20		25		8
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		30		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		20		
Nibble mode read/write cycle time	t_{NC}	ns	60		70		80		9
Nibble mode read-write cycle time	t_{NRWC}	ns	60		70		80		9
Nibble mode access time	t_{NCAC}	ns		25		30		35	9
Nibble mode $\overline{CAS}$ pulse width	t_{NCAS}	ns	25		30		35		9
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	ns	25		30		35		9
Nibble mode read $\overline{RAS}$ hold time	t_{NRRSH}	ns	25		30		35		9
Nibble mode write $\overline{RAS}$ hold time	t_{NWRSH}	ns	45		50		60		9
Nibble mode $\overline{CAS}$ hold time referenced to $\overline{RAS}$	t_{RNH}	ns	25		30		35		9

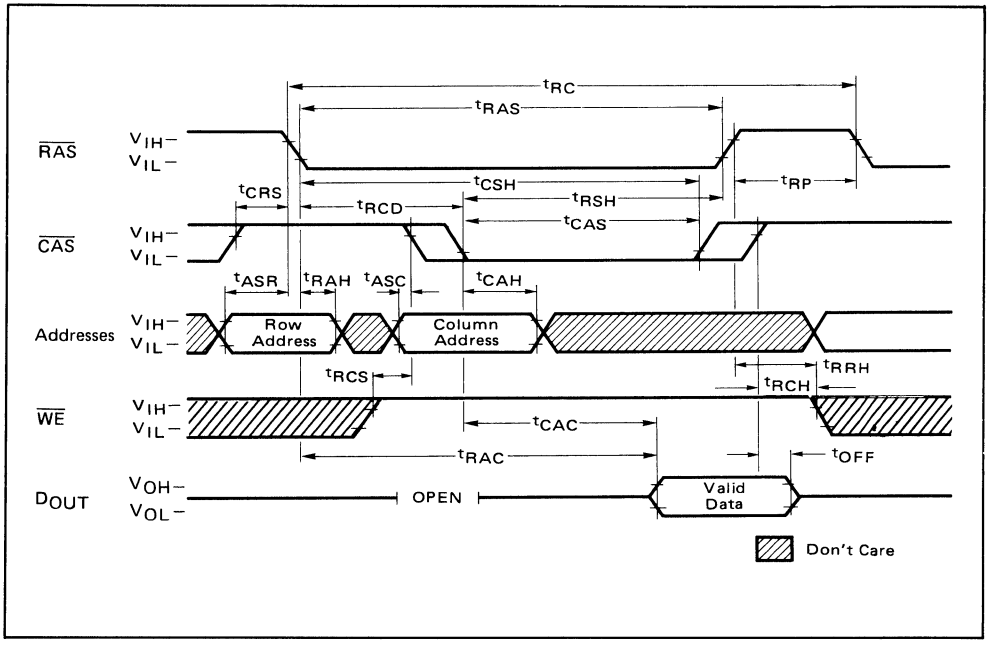
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41257A-10		MSM41257A-12		MSM41257A-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh counter test cycle time	t_{RTC}	ns	315		355		415		10
Refresh counter test $\overline{RAS}$ pulse width	t_{TRAS}	ns	215	10μs	255	10μs	305	10μs	10
Refresh counter test $\overline{CAS}$ precharge time	t_{CPT}	ns	50		60		70		10

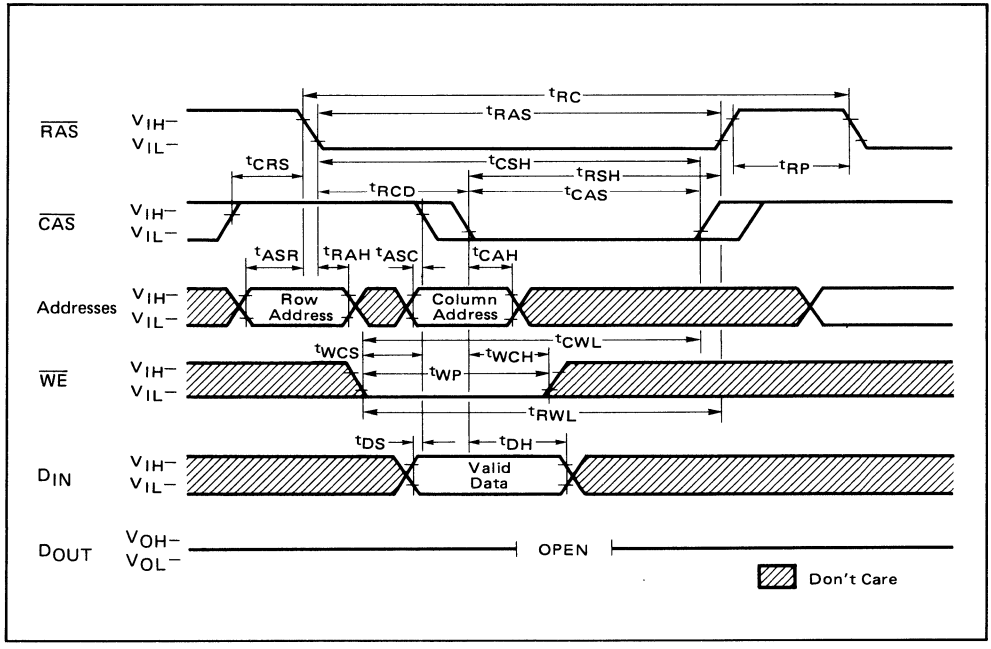
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min.), the cycle is read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. Nibble mode cycle.
10. $\overline{CAS}$ before $\overline{RAS}$ Refresh Counter Test Cycle only.

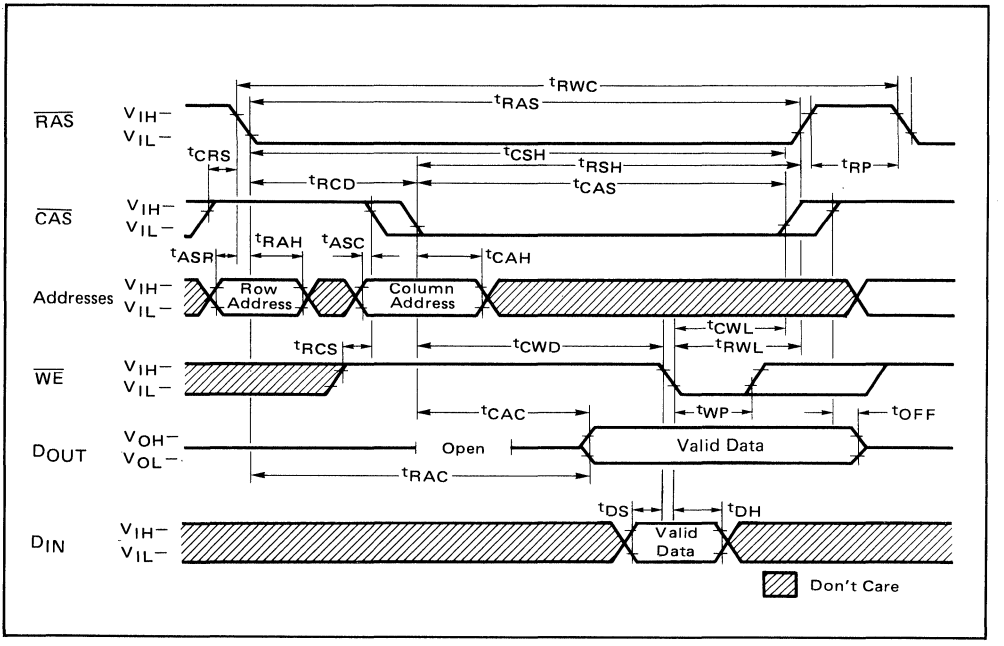
READ CYCLE



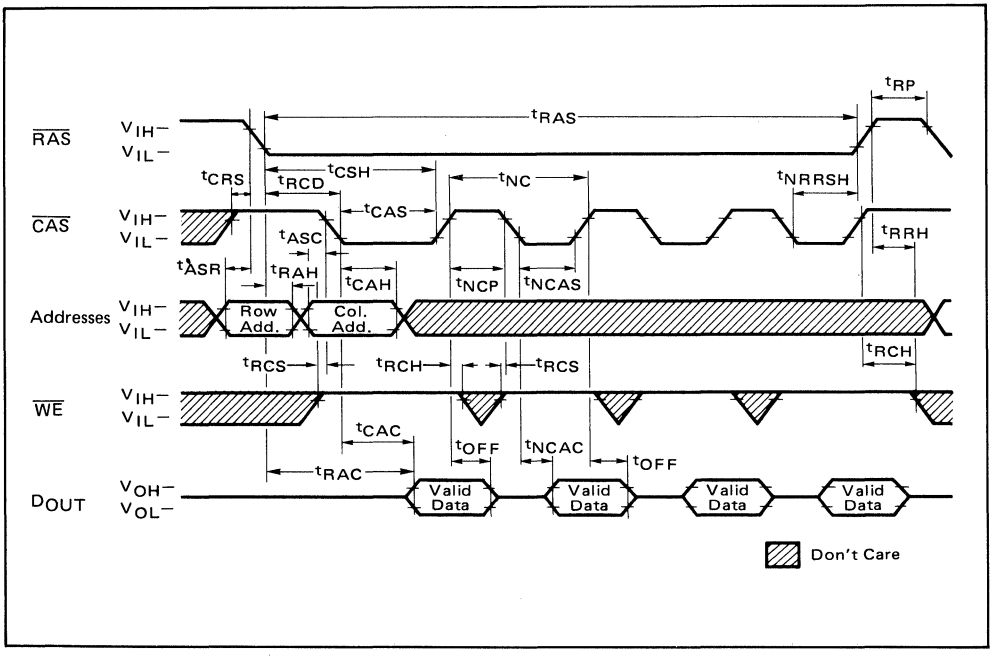
WRITE CYCLE (EARLY WRITE)



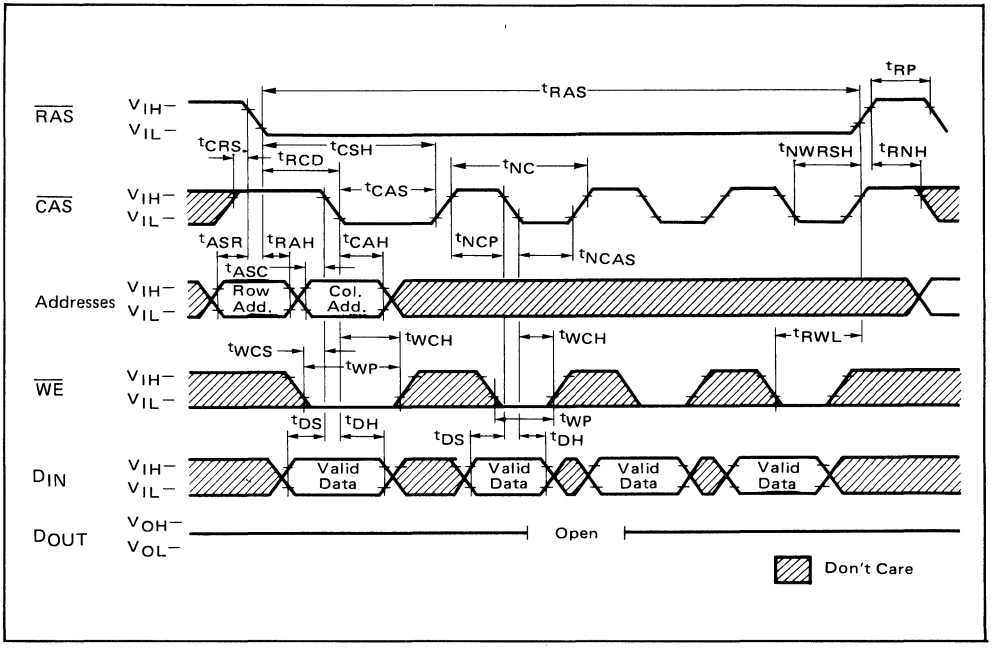
READ-WRITE/READ-MODIFY-WRITE CYCLE



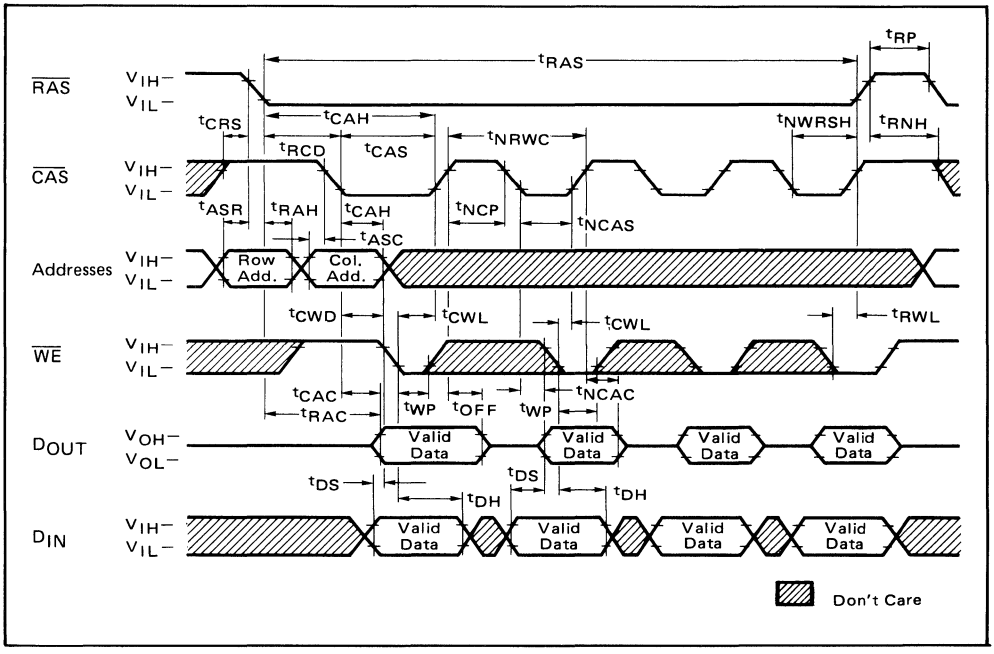
NIBBLE MODE READ CYCLE



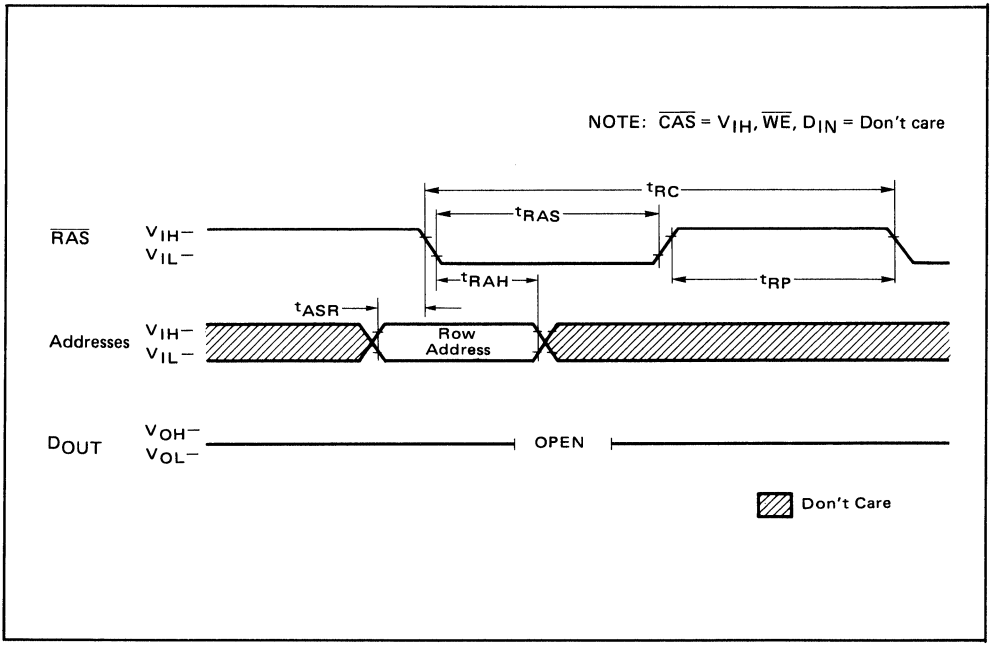
NIBBLE MODE WRITE CYCLE



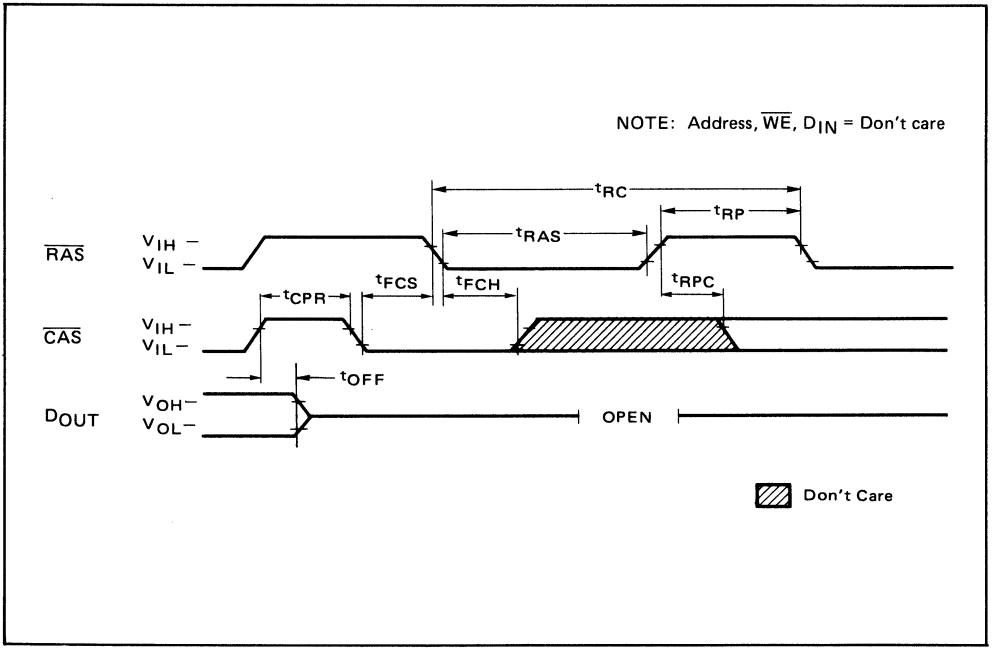
NIBBLE MODE READ-WRITE CYCLE



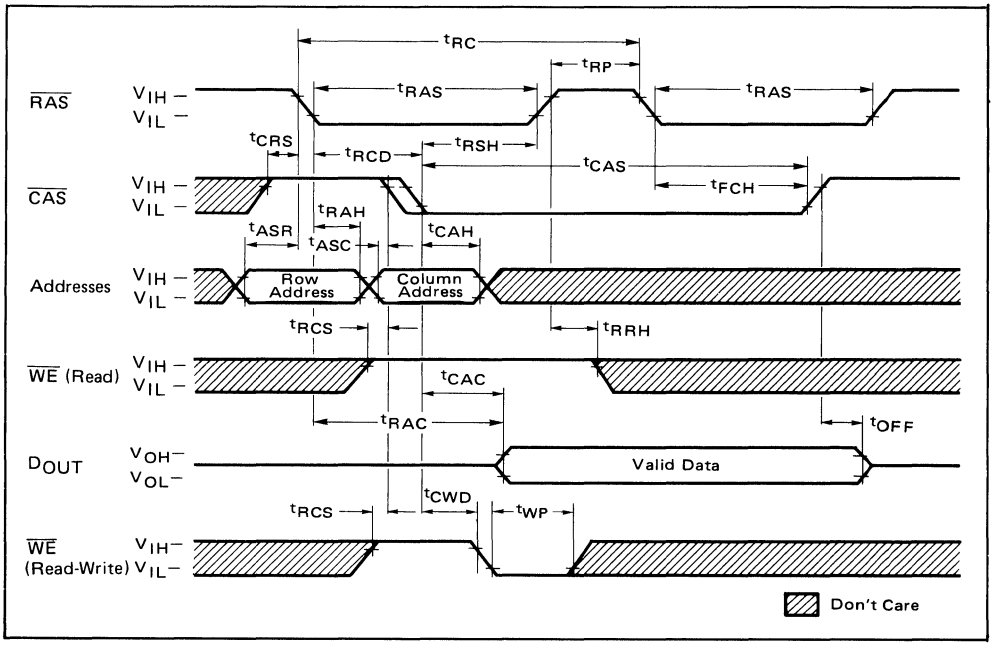
$\overline{RAS}$ ONLY REFRESH CYCLE



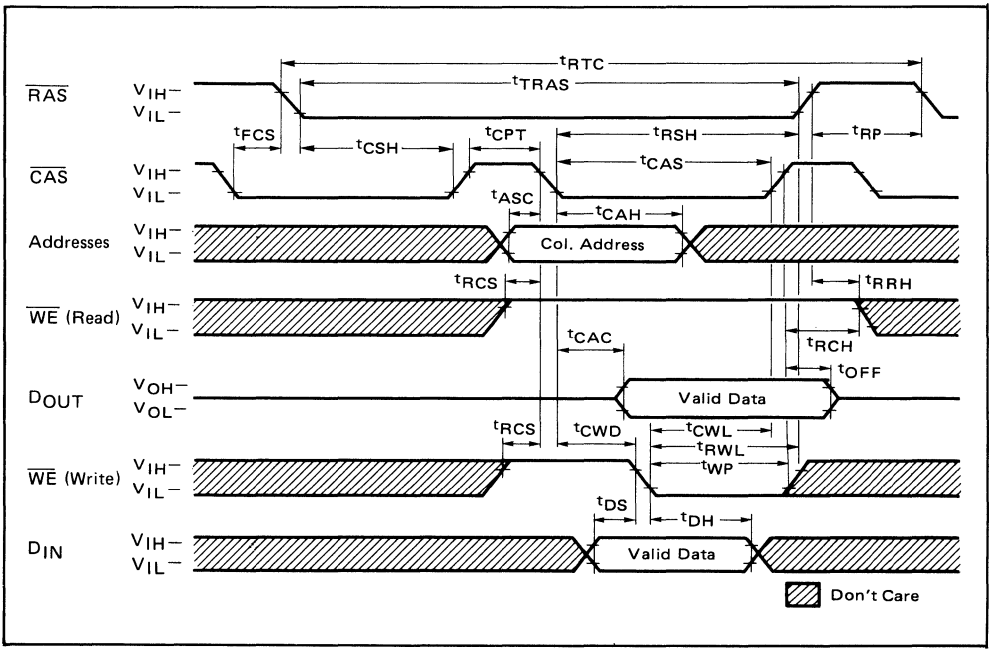
$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Simple Timing Requirements:

The MSM41257A has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSM41257A can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSM41257A has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). And the MSM41257A can commit better memory system through-put during operations in an interleaved system. Furthermore, Oki has made timing requirements referenced to $\overline{RAS}$ non-restrictive and deleted from the data sheet, which includes t_{AR}, t_{WCR}, t_{DHR} and t_{RWD}. Therefore, the hold times of the Column Address D_{IN} and $\overline{WE}$ as well as t_{CWD} ($\overline{CAS}$ to $\overline{WE}$ Delay) are not restricted by t_{RCD}.

Fast Read- While-Write Cycle:

The MSM41257A has the fast read while write cycle which is achieved by excellent control of the three-state output buffer in addition to the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MSM41257A goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MSM41257A goes to delayed write mode where the output contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, very fast read write cycle becomes available.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSM41257A. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM41257A during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is strobed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Nibble Mode:

Nibble mode allows high speed serial read, write or read-modify-write access of 2, 3 or 4 bits of data. The bits of data that may be accessed during nibble mode are determined by the 8 row addresses and the 8 column addresses. The 2 bits of addresses (CA_8 RA_8) are used to select 1 of the 4 nibble bits for initial access. After the first bit is accessed by normal mode, the remaining nibble bits may be accessed by $\overline{CAS}$ "high" then "low" while $\overline{RAS}$ remains "low". Toggling $\overline{CAS}$ causes RA_8 and CA_8 to be incremented internally while all other address bits are held constant and makes the next nibble bit available for access. (See Table 1)

If more than 4 bits are accessed during nibble mode, the address sequence will begin to repeat. If any bit is written during nibble mode, the new data will be read on any subsequent access. If the write operation may be executed again on subsequent access, the new data will be written into the selected cell location.

In nibble mode, the three-state control of D_{OUT} Pin is determined by the first normal access cycle.

The data output is controlled by only $\overline{WE}$ state referenced at $\overline{CAS}$ negative transition of the normal cycle (first Nibble bit). That is, when $t_{WCS} > t_{WCS}$ (min) is met, the data output will remain open circuit throughout the succeeding Nibble cycle regardless of $\overline{WE}$ state. Whereas, when $t_{CWD} > t_{CWD}$ (min) is met, the data output will contain data from the cell selected during the succeeding nibble cycle regardless of $\overline{WE}$ state. The write operation is done during the period where $\overline{WE}$ and $\overline{CAS}$ clocks are low. Therefore, write operation can be done bit by bit during each nibble operation at any timing conditions of $\overline{WE}$ (t_{WCS} and t_{CWD}) at the normal cycle (first Nibble bit).

Table 1 NIBBLE MODE ADDRESS SEQUENCE EXAMPLE

SEQUENCE	NIBBLE BIT	RA_8	ROW ADDRESS	CA_8	COLUMN ADDRESS	
$\overline{RAS}/\overline{CAS}$ (normal mode)	1	0	10101010	0	10101010	... input addresses
toggle $\overline{CAS}$ (nibble mode)	2	1	10101010	0	10101010	generated internally sequence repeats
toggle $\overline{CAS}$ (nibble mode)	3	0	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	4	1	10101010	1	10101010	
toggle $\overline{CAS}$ (nibble mode)	1	0	10101010	0	10101010	

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSM41257A offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSM41257A hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. A memory cell address, consisting of a row address (9 bits) and a column address (9 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_7 are defined by the refresh counter. The other bit A_8 is set "high" internally.
* A COLUMN ADDRESS
  - All the bits A_0 through A_8 are defined by latching levels on A_0 through A_8 at the second falling edge of CAS.

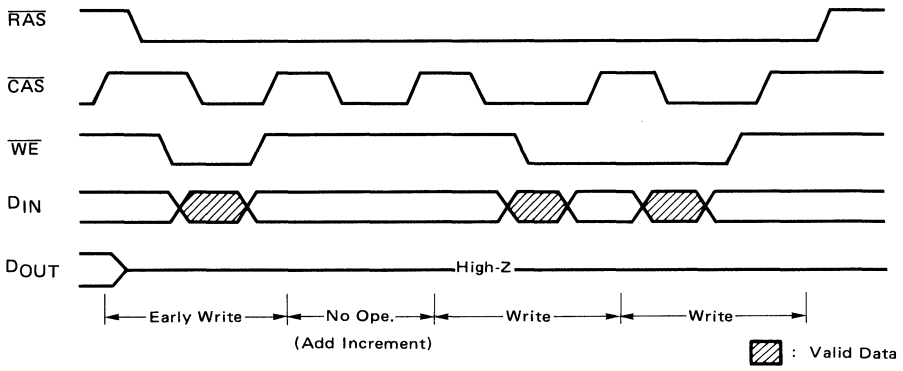
Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

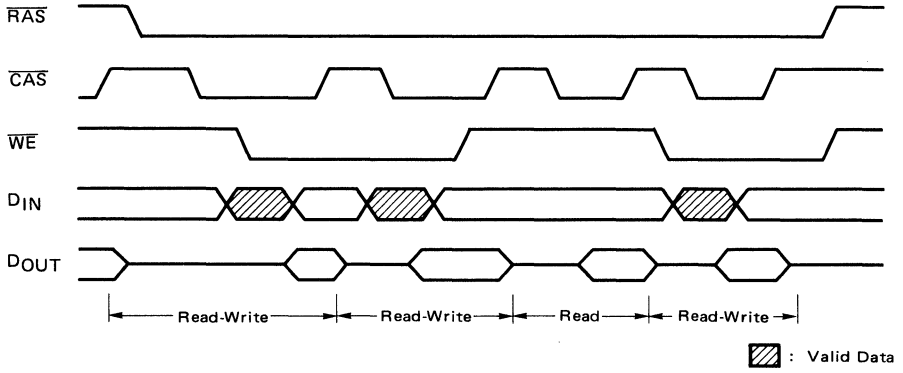
(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

NIBBLE MODE

1) The case of first nibble cycle is Early write



2) The case of first nibble cycle is delyed write (Read-Write)



MSM41257A Bit Map (Physical-Decimal)

□ Pin 16

252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
128	128	128	128		128	128	128	128		128	128	128	128		128	128	128	128
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
384	384	384	384		384	384	384	384		384	384	384	384		384	384	384	384
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
129	129	129	129		129	129	129	129		129	129	129	129		129	129	129	129
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
385	385	385	385		385	385	385	385		385	385	385	385		385	385	385	385
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
254	254	254	254		254	254	254	254		254	254	254	254		254	254	254	254
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
510	510	510	510		510	510	510	510		510	510	510	510		510	510	510	510
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
255	255	255	255		255	255	255	255		255	255	255	255		255	255	255	255
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
511	511	511	511		511	511	511	511		511	511	511	511		511	511	511	511

COLUMN DECODER

ROW DECODER

ROW DECODER

252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
383	383	383	383		383	383	383	383		383	383	383	383		383	383	383	383
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
127	127	127	127		127	127	127	127		127	127	127	127		127	127	127	127
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
382	382	382	382		382	382	382	382		382	382	382	382		382	382	382	382
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
126	126	126	126		126	126	126	126		126	126	126	126		126	126	126	126
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
257	257	257	257		257	257	257	257		257	257	257	257		257	257	257	257
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
1	1	1	1		1	1	1	1		1	1	1	1		1	1	1	1
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
256	256	256	256		256	256	256	256		256	256	256	256		256	256	256	256
252	253	254	255		3	2	1	0		256	257	258	259		511	510	509	508
0	0	0	0		0	0	0	0		0	0	0	0		0	0	0	0

COLUMN DECODER

A8 ROW = "L"
REFRESH ADDRESS
(0 – 255)

A8 ROW = "H"
REFRESH ADDRESS
(0 – 255)

□ Pin 8

A
B

: CELL

A = ROW ADDRESS (DECIMAL)
B = COLUMN ADDRESS (DECIMAL)

ROW ADDRESS
8N+6, 8N+7, 8N, 8N+1
8N+2, 8N+3, 8N+4, 8N+5
8N+6, 8N+7, 8N, 8N+1
8N+2, 8N+3, 8N+4, 8N+5
N=0, 1, 2, ·····63

COLUMN ADDRESS
2N : POSITIVE
2N : NEGATIVE
2N+1 : NEGATIVE
2N+1 : POSITIVE
N=0, 1, 2, ·····255

OKI semiconductor

MSM41464

65,536-WORD × 4-BITS DYNAMIC RANDOM ACCESS MEMORY

GENERAL DESCRIPTION

The Oki MSM41464 is a fully decoded, dynamic NMOS random access memory organized as 65,536 words by 4 bits. The design is optimized for high-speed, high performance applications such as mainframe memory, buffer memory, peripheral storage and environments where low power dissipation and compact layout is required.

Multiplexed row and column address inputs permit the MSM41464 to be housed in a standard 18 pin DIP or PLCC. Pin-outs conform to the JEDEC approved pin out. Additionally, the MSM41464 offers new functional enhancements that make it more versatile than previous dynamic RAMs. "$\overline{CAS}$-before-$\overline{RAS}$" refresh provides an on-chip refresh capability.

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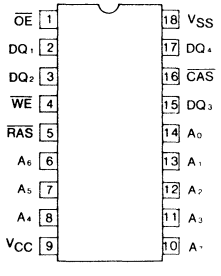
The MSM41464 is fabricated using silicon gate NMOS and Oki's advanced VLSI Polysilicon process. This process, coupled with single-transistor memory storage cells, permits maximum circuit density and minimum chip size. Dynamic circuitry is employed in the design, including the sense amplifiers.

Clock timing requirements are noncritical, and power supply tolerance is very wide. All inputs and output are TTL compatible.

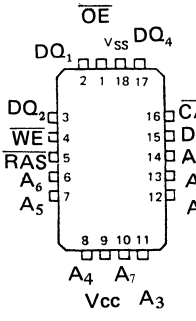
FEATURES

- 65,536 × 4 RAM, 18 pin package
- Silicon-gate, Double Poly NMOS, single transistor cell
- Row access time:
  - 100 ns max (MSM41464-10)
  - 120 ns max (MSM41464-12)
  - 150 ns max (MSM41464-15)
- Cycle time:
  - 200 ns min (MSM41464-10)
  - 220 ns min (MSM41464-12)
  - 260 ns min (MSM41464-15)
- Low power:
  - 385 mW active (MSM41464-10)
  - 360 mW active (MSM41464-12)
  - 330 mW active (MSM41464-15)
  - 28 mW max standby
- Single +5V Supply, ±10% tolerance
- All inputs TTL compatible, low capacitive load
- Three-state TTL compatible output
- "Gated" $\overline{CAS}$
- 256 refresh cycles/4 ms
- Output impedance controllable through early write and $\overline{OE}$ operations
- Output unlatched at cycle end allows extended page boundary and two-dimensional chip select
- Read-Modify-Write, $\overline{RAS}$-only refresh, capability
- On-chip latches for Addresses and Data-in
- On-chip substrate bias generator for high performance
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Page Mode" capability

PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
$A_0 \sim A_7$	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$DQ_1 \sim DQ_4$	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)



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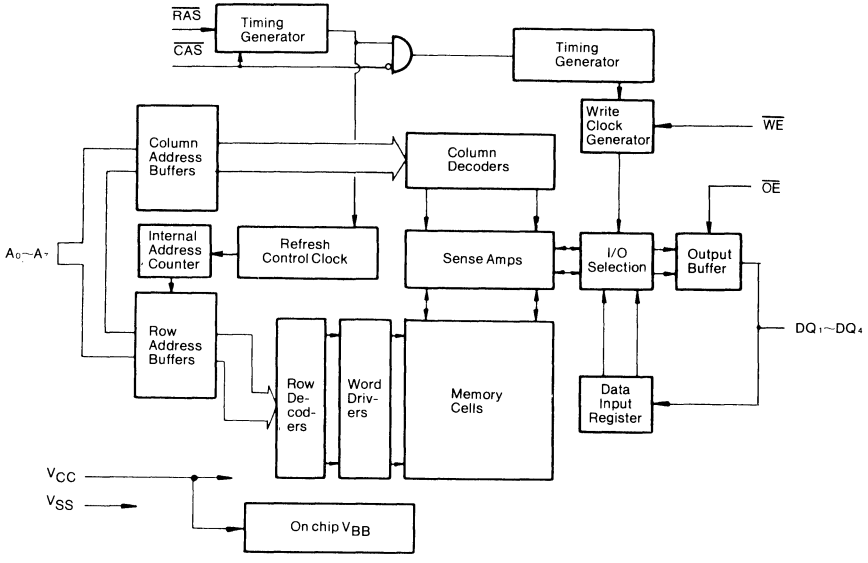
FUNCTIONAL BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	Topr	0 to 70	°C
Storage temperature	Tstg	−55 to +150	°C
Power dissipation	P_D	1.0	W
Short circuit output current		50	mA

Note: Parmanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating Temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Min.	Max.	Unit	Notes
OPERATING CURRENT* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	MSM41464-10	I_{CC1}		70	mA	
	MSM41464-12			65		
	MSM41464-15			60		
STANDBY CURRENT* Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		I_{CC2}		5.0	mA	
REFRESH CURRENT 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	MSM41464-10	I_{CC3}		60	mA	
	MSM41464-12			55		
	MSM41464-15			50		
PAGE MODE CURRENT* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	MSM41464-10	I_{CC4}		45	mA	
	MSM41464-12			40		
	MSM41464-15			35		
REFRESH CURRENT 2* Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	MSM41464-10	I_{CC5}		65	mA	
	MSM41464-12			60		
	MSM41464-15			55		
INPUT LEAKAGE CURRENT Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)		I_{LI}	−10	10	μA	
OUTPUT LEAKAGE CURRENT (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)		I_{LO}	−10	10	μA	
OUTPUT LEVELS Output high voltage (I_{OH} = −5 mA)		V_{OH}	2.4		V	
Output low voltage (I_{OL} = 4.2 mA)		V_{OL}		0.4	V	

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input capacitance ($A_0 \sim A_7$)	C_{IN1}	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	–	7	pF
Data I/O capacitance ($DQ_1 \sim DQ_4$)	C_D	–	7	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSM41464-10		MSM41464-12		MSM41464-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Read-write cycle time	t_{RWC}	ns	270		300		355		
Page mode cycle time	t_{PC}	ns	100		120		145		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	25	0	30	0	40	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ precharge time (Page mode cycle only)	t_{CP}	ns	40		50		60		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7, 8
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time	t_{RCH}	ns	0		0		0		10
Write command set-up time	t_{WCS}	ns	0		0		0		9

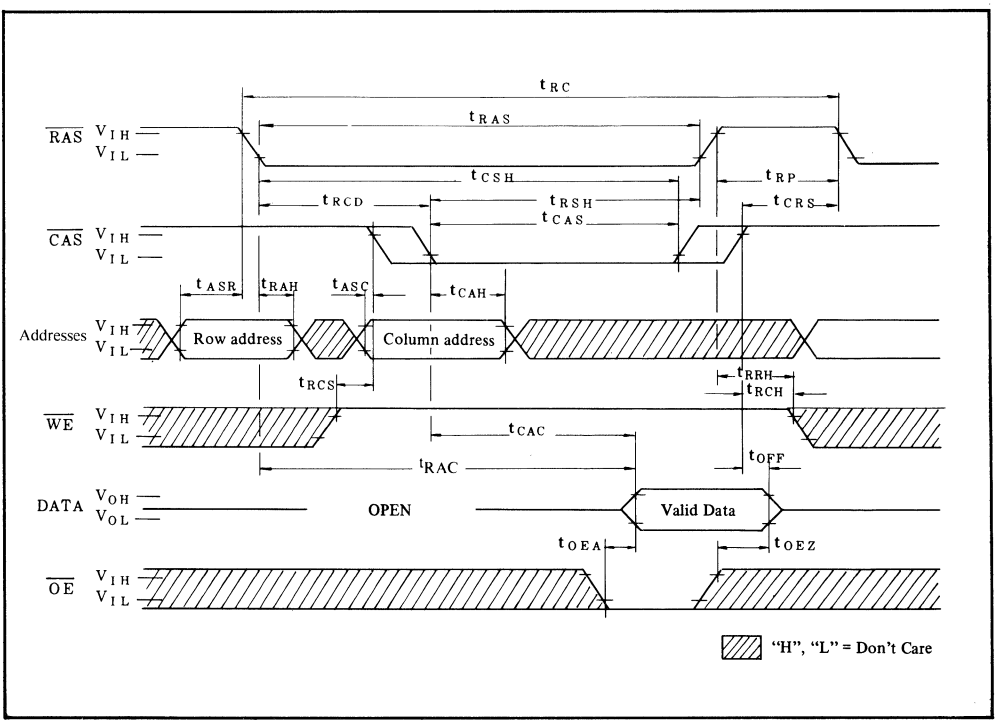
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSM41464-10		MSM41464-12		MSM41464-15		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	25		30		35		
Write command hold time	t_{WCH}	ns	25		30		35		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	25		30		35		
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	ns	80		95		120		9
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	ns	130		155		195		9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	ns	20		20		20		10
Access time from $\overline{OE}$	t_{OEA}	ns		25		30		40	
$\overline{OE}$ data delay time	t_{OED}	ns	25		30		40		
$\overline{OE}$ hold time	t_{OEH}	ns	0		0		0		
Turn-off delay time from $\overline{OE}$	t_{OEZ}	ns	0	25	0	30	0	40	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCS}	ns	20		25		30		
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	ns	20		20		20		
$\overline{CAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CPR}	ns	20		25		30		
Read/write cycle (Refresh counter test)	t_{RTC}	ns	380		430		510		11
$\overline{RAS}$ pulse width (Refresh counter test)	t_{TRAS}	ns	280	10μs	330	10μs	400	10μs	11
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	ns	50		60		70		11
Read/write cycle time (Page mode)	t_{PRWC}	ns	170		200		240		

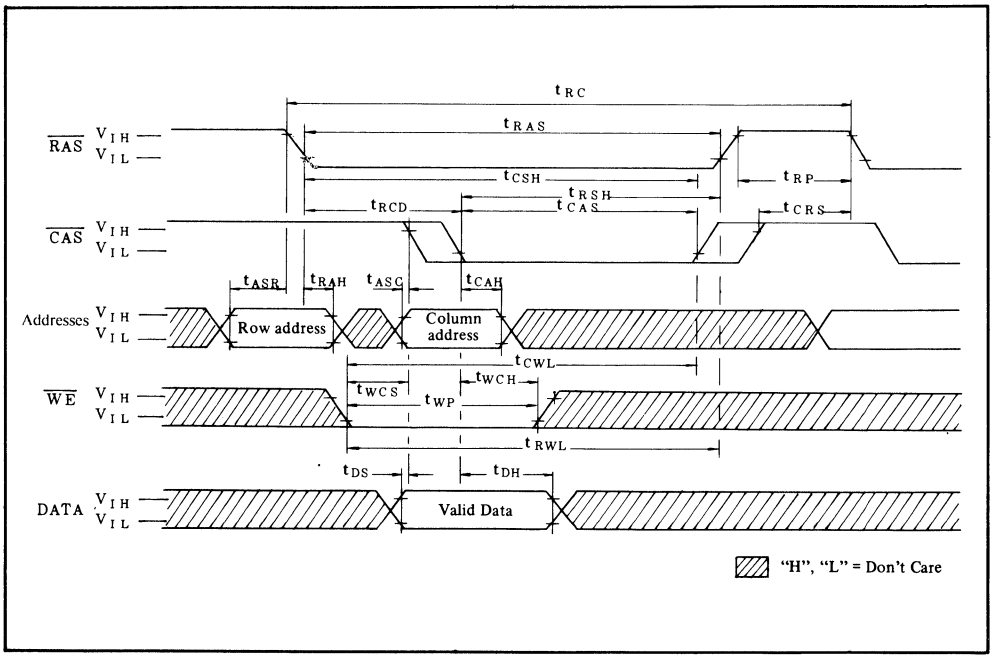
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.) If $t_{RCD} > t_{RCD}$ (Max.), t_{RAC} will increase by $\{t_{RCD} - t_{RCD}$ (Max.)$\}$.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Assumes that t_{RCD} (Min.) $= t_{RAH}$ (Min.) $+ 2t_T + t_{ASC}$ (Min.)
9. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical charcteristics only; if $t_{WCS} > t_{WCS}$ (Min.), the cycle is an early write cycle and the data in/data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (Min.) and $t_{RWD} \geqq t_{RWD}$ (Min.) the cycle is read-write cycle and the data in/data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
11. $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle only.

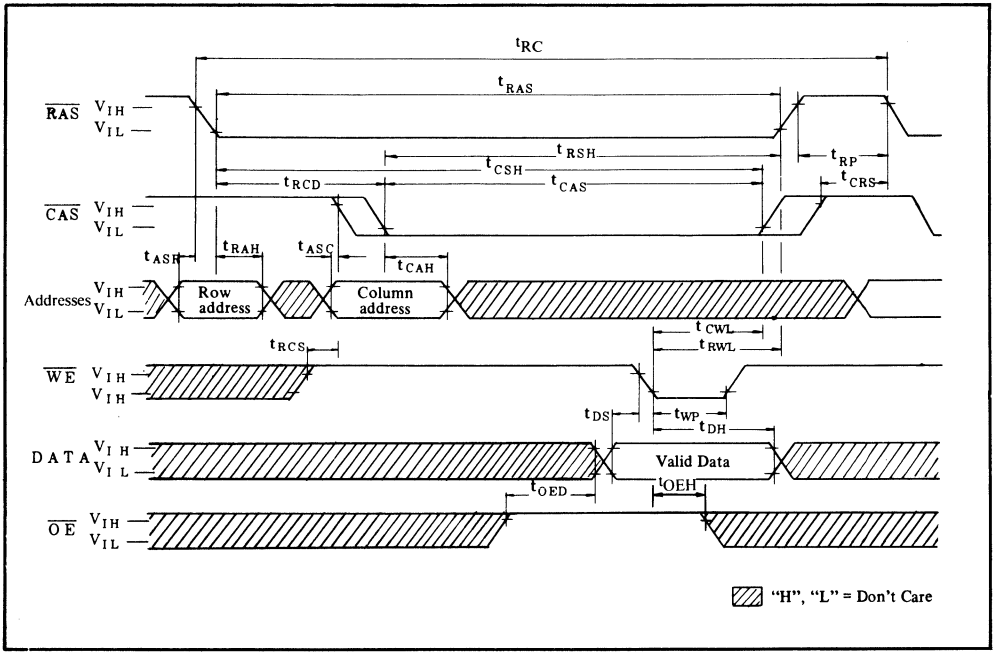
READ CYCLE



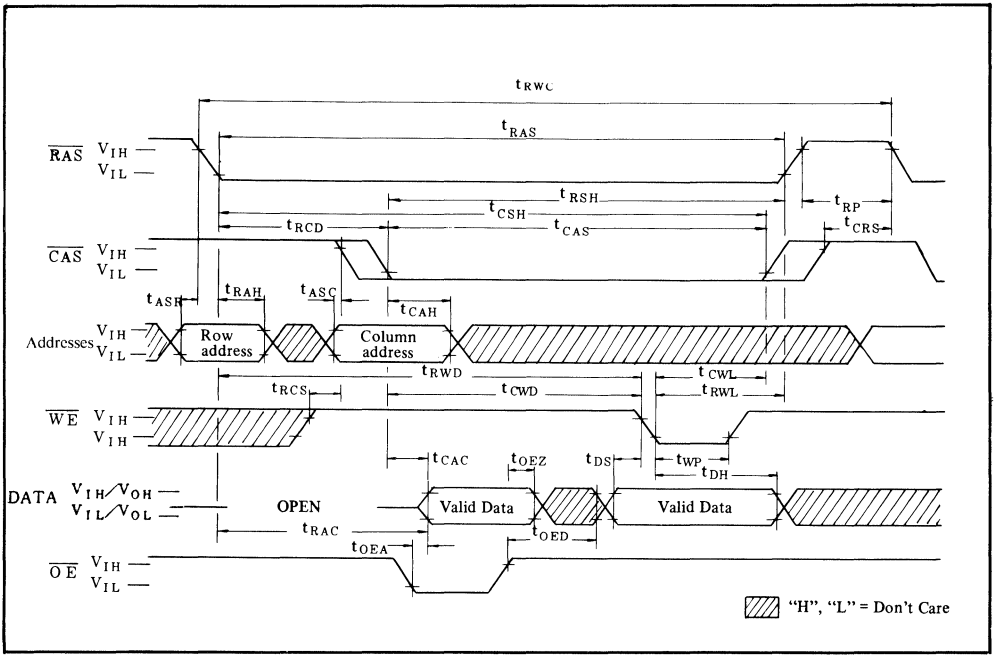
WRITE CYCLE (EARLY WRITE)



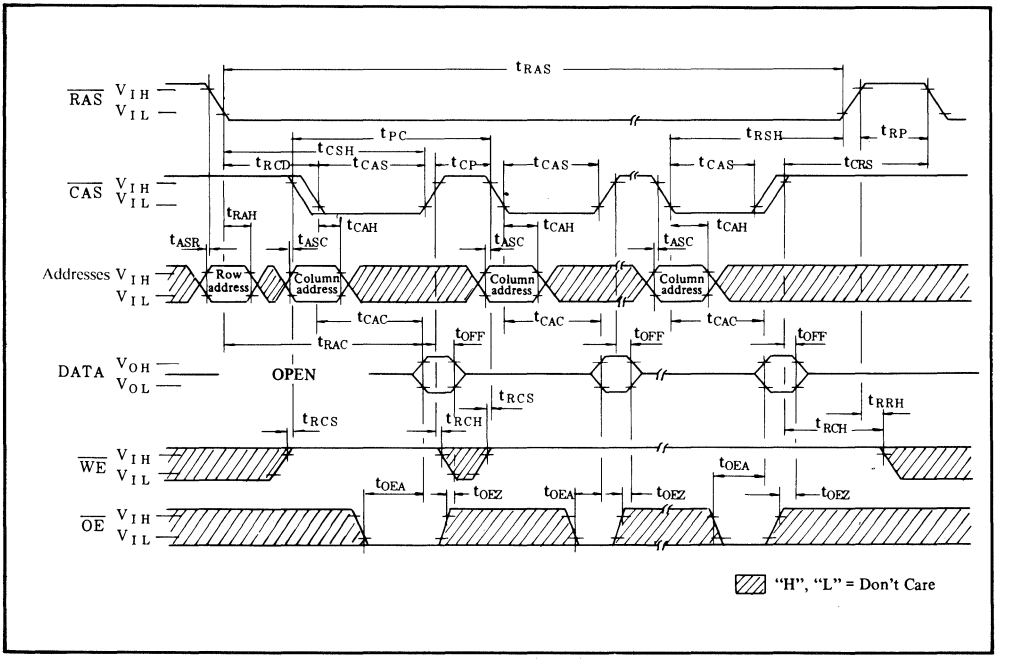
$\overline{OE}$ WRITE CYCLE



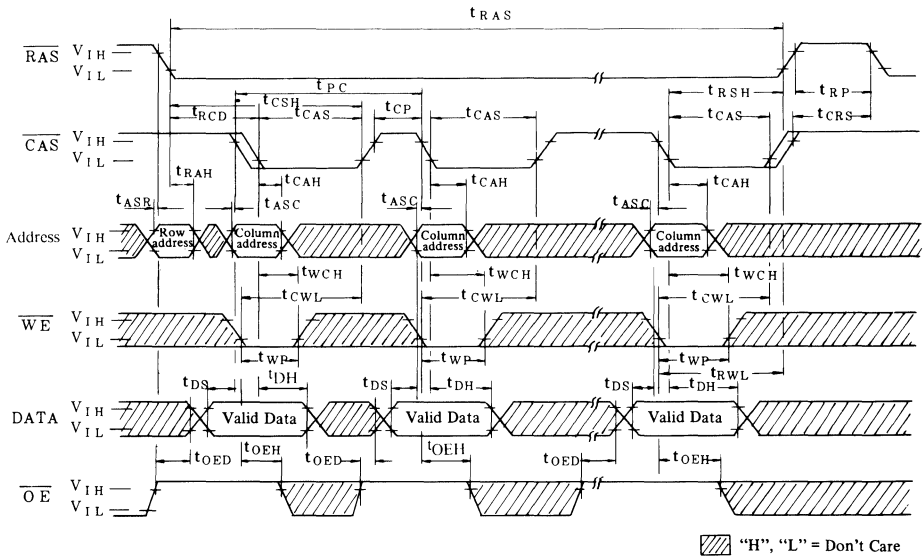
READ/WRITE AND READ MODIFY WRITE CYCLE



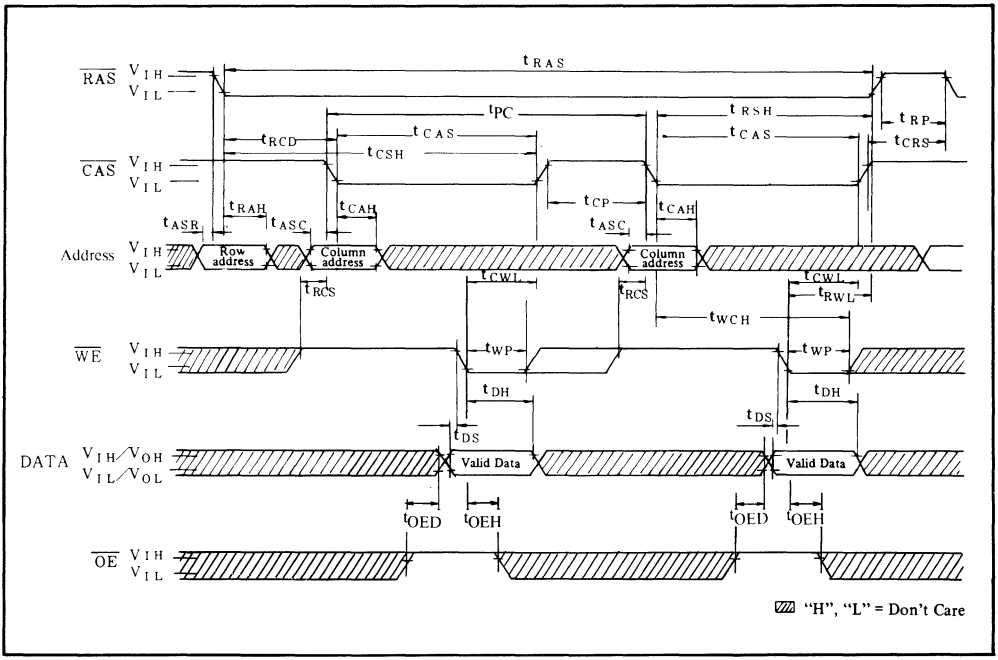
PAGE MODE READ CYCLE



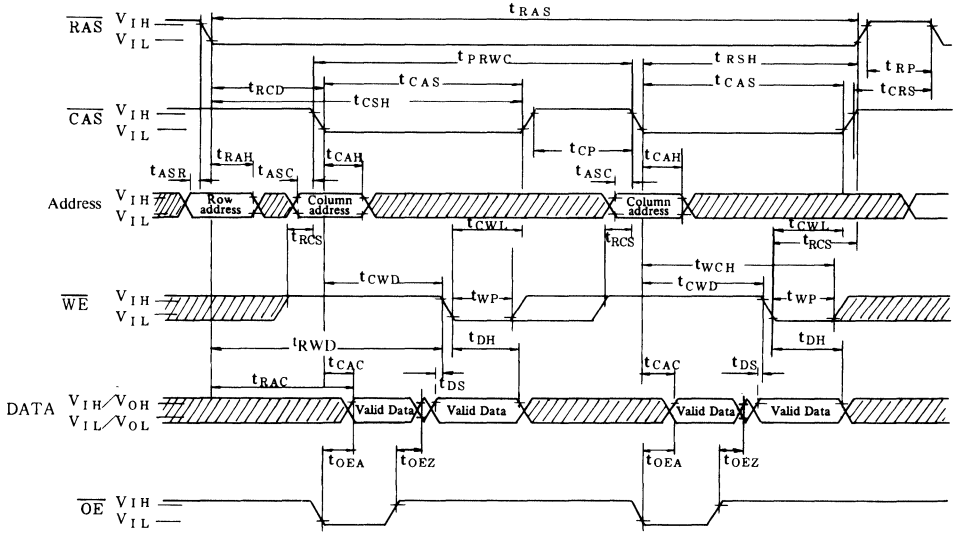
PAGE MODE WRITE CYCLE



PAGE MODE $\overline{OE}$ WRITE CYCLE

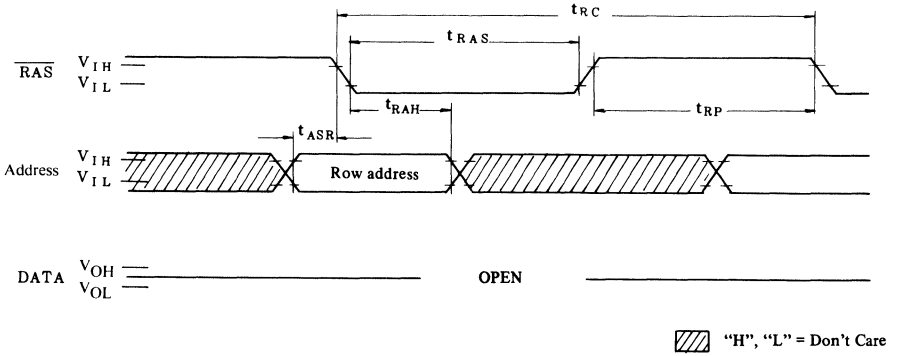


PAGE MODE READ/WRITE CYCLE



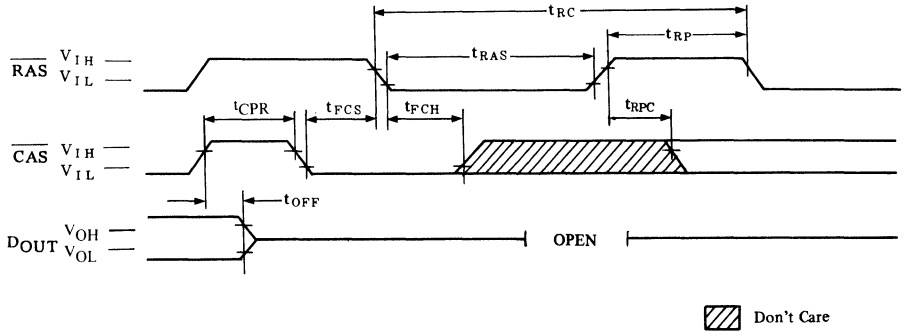
RAS ONLY REFRESH CYCLE

Note: CAS = VIH, WE and OE not dependent on the high or low level.

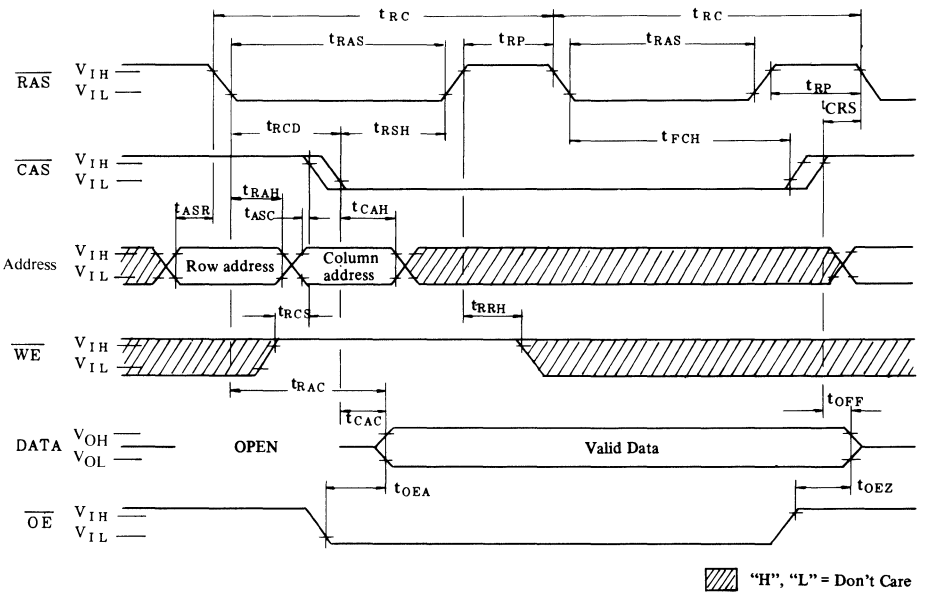


$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

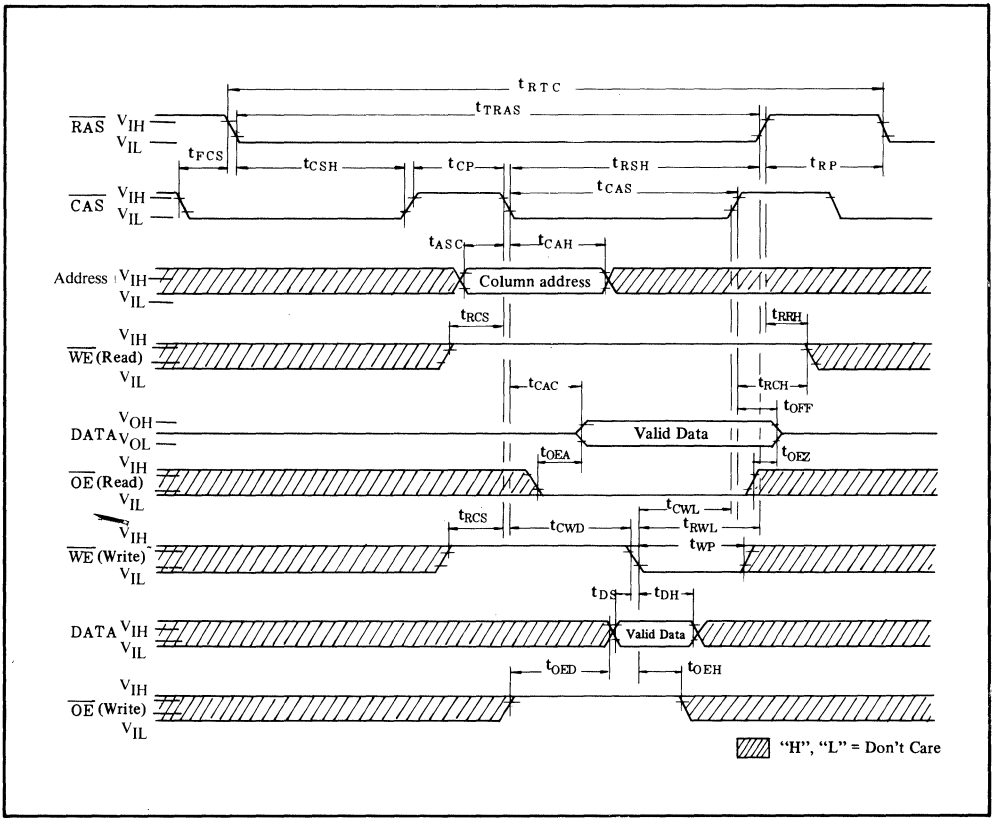
Note: $\overline{WE}$ and $\overline{OE}$ not dependent on the high or low level.



HIDDEN REFRESH CYCLE



CAS BEFORE RAS REFRESH COUNTER TEST CYCLE



FUNCTIONAL DESCRIPTION

Address Inputs:

16 bits of binary address input are required to decode any one of the 65,536 words by 4 bit storage cell locations.

8 row-address bits are set up on address input pins A_0 through A_7 and latched onto the chip by the row address strobe (RAS). Then 8 column-address bits are set up on pins A_0 through A_7 and latched onto the chip by the column address strobe (CAS).

All addresses must be stable on or before the falling edges of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (gated) by the $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Therefore specifications permit column addresses to be input immediately after the row address hold time (t_{RAH}).

Write Enable:

The read mode or write mode is selected with the $\overline{WE}$ input. The logic high of the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The data input is disabled when the read mode is selected. Data-out will remain in the high-impedance state allowing a write cycle with $\overline{WE}$ grounded.

Data Input:

Data is written during a write or read-modify write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{WE}$ strobes data into the on-chip data latches. In an early-write cycle, $\overline{WE}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{WE}$ with setup and hold times referenced to this signal. In delayed or read-modify-write, $\overline{OE}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

Data Output:

The three-state output buffer provides direct TTL compatibility with a fan-out of two standard TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval t_{CAC} that begins with the negative transition of $\overline{CAS}$ as long as t_{RAC} and t_{OEA} are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ or $\overline{OE}$ are low. $\overline{CAS}$ or $\overline{OE}$ going high returns it to a high impedance state. In an early-write cycle, the output is always in the high impedance state. In a delayed-write or read-modify-write cycle, the output must be put in the high impedance state prior to applying data to the DQ input. This is accomplished by bringing $\overline{OE}$ high prior to applying data, thus satisfy t_{OED}.

Output Enable:

The $\overline{OE}$ controls the impedance of the output buffers. When $\overline{OE}$ is high, the buffers will remain in the high impedance state. Bringing $\overline{OE}$ low during a normal cycle will activate the output buffers putting them in the low impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low impedance state. Once in the low impedance state, they will remain in the low impedance state until $\overline{OE}$ or $\overline{CAS}$ is brought high.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every four milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of 256 (A_0 to A_7) row-addresses with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$-only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time. Hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Cycle:

A special timing sequence using $\overline{CAS}$ before $\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of $\overline{CAS}$ before $\overline{RAS}$ refresh activated circuitry. As shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, if $\overline{CAS}$ goes to high and goes to low again while $\overline{RAS}$ is held low, the read and write operation are enabled. This is shown in the $\overline{CAS}$ before $\overline{RAS}$ counter test cycle. A memory cell address, consisting of a row address (8 bits) and a column address (8 bits), to be acceded can be defined as follows:

* A ROW ADDRESS
  - Bits A_0 through A_7 are defined by the refresh counter.
* A COLUMN ADDRESS
  - All the bits A_0 through A_7 are defined by latching levels on A_0 through A_7 at the second falling edge of $\overline{CAS}$.

Suggested $\overline{CAS}$ before $\overline{RAS}$ Counter Test Procedure:

The timing, as shown in $\overline{CAS}$ before $\overline{RAS}$ Counter Test Cycle, is used for all the operations described as follows:

(1) Initialize the internal refresh counter. For this operaton, 8 cycles are required.
(2) Write a test pattern of lows into memory cells at a single column address and 256 row addresses.
(3) By using read-modify-write cycle, read the low written at the last operation (Step (2)) and write a new high in the same cycle. This cycle is repeated 256 times, and highs are written into the 256 memory cells.
(4) Read the high written at the last operation (Step (3)).
(5) Complement the test pattern and repeat the steps (2), (3) and (4).

MSM41464 Bit Map (Physical-Decimal)

DQ1 DQ2 DQ4 DQ3

□ Pin 18

252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
128	128	128	128	128	128	128	128	128	128	128	128	128	128	128	128
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
128	128	128	128	128	128	128	128	128	128	128	128	128	128	128	128
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
129	129	129	129	129	129	129	129	129	129	129	129	129	129	129	129
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
129	129	129	129	129	129	129	129	129	129	129	129	129	129	129	129
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
130	130	130	130	130	130	130	130	130	130	130	130	130	130	130	130
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
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253	253	253	253	253	253	253	253	253	253	253	253	253	253	253	253
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
254	254	254	254	254	254	254	254	254	254	254	254	254	254	254	254
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
254	254	254	254	254	254	254	254	254	254	254	254	254	254	254	254
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
255	255	255	255	255	255	255	255	255	255	255	255	255	255	255	255
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
255	255	255	255	255	255	255	255	255	255	255	255	255	255	255	255

COLUMN DECODER

ROW DECODER

ROW DECODER

252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
127	127	127	127	127	127	127	127	127	127	127	127	127	127	127	127
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
127	127	127	127	127	127	127	127	127	127	127	127	127	127	127	127
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
126	126	126	126	126	126	126	126	126	126	126	126	126	126	126	126
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
126	126	126	126	126	126	126	126	126	126	126	126	126	126	126	126
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
125	125	125	125	125	125	125	125	125	125	125	125	125	125	125	125
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
125	125	125	125	125	125	125	125	125	125	125	125	125	125	125	125
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2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
2	2	2	2	2	2	2	2	2	2	2	2	2	2	2	2
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
252	253	254	255	3	2	1	0	0	1	2	3	255	254	253	252
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

COLUMN DECODER

REFRESH ADDRESS

(0 – 255)

REFRESH ADDRESS

(0 – 255)

□
Pin 9

A
B

: CELL

A = ROW ADDRESS (DECIMAL)

B = COLUMN ADDRESS (DECIMAL)

OKI semiconductor
MSM51C256

262,144 WORD X 1-BITS DYNAMIC RAM

GENERAL DESCRIPTION

The MSM51C256 is a new generation dynamic RAM organized as 262,144 words by 1 bit. The technology used to fabricate the MSM51C256 is OKI's CMOS silicon gate process technology. The device operates at a single + 5V power supply. Its I/O pins are TTL compatible.

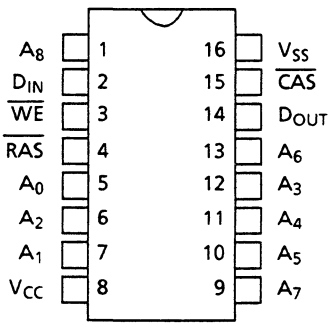
FEATURES

- Silicon gate, double polysilicon CMOS, 1-transistor memory cell
- 262,144 words by 1 bit
- Standard 16 lead plastic DIP/18 lead PLCC
- Family organization

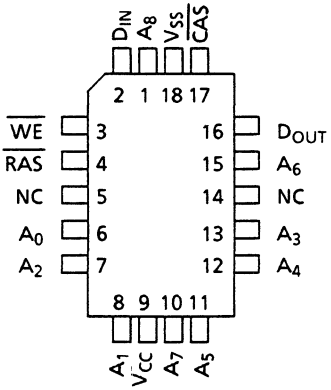
Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM51C256-80	80 ns	160 ns	330 mW	20 mW
MSM51C256-10	100 ns	190 ns	275 mW	

- Single + 5V supply, ± 10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 256 cycles/4 ms
- Common I/O capability using "Early Write" operation
- Fast page mode, read/write capability
- $\overline{CAS}$ before $\overline{RAS}$ refersh, Hidden refresh, RAS only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit

MSM51C256RS
16 Lead Plastic DIP PIN CONFIGURATION
Top View

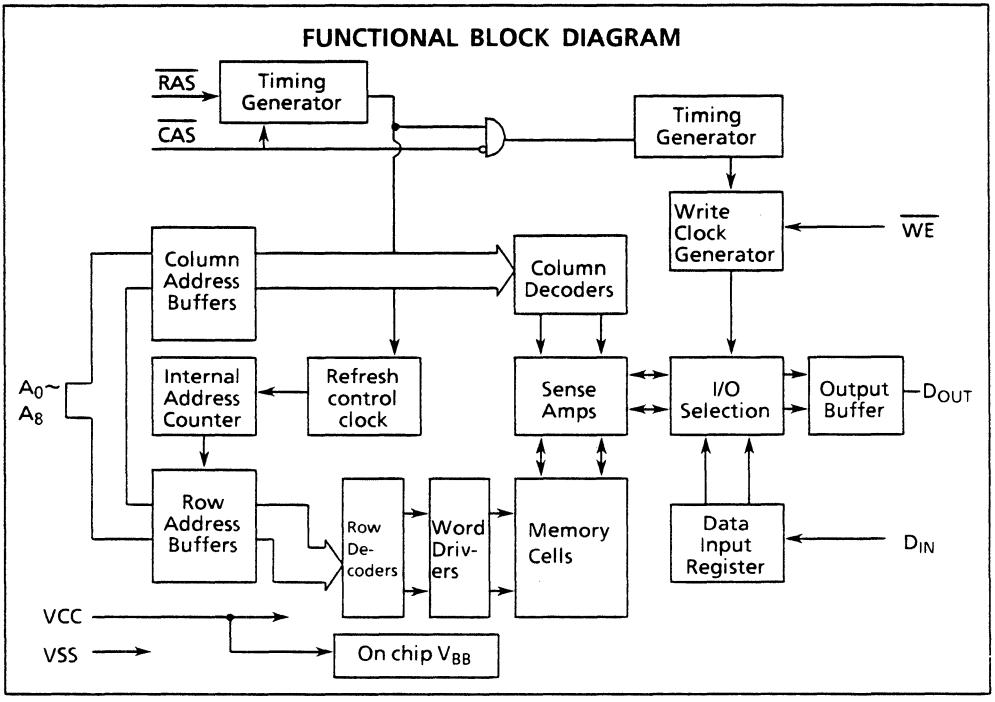


MSM51C256JS
18 Lead PLCC Package PIN CONFIGURATION
Top View



DYNAMIC RAM·MSM51C256RS/JS

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Rating	Symbol	Condition	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	− 1.0 to + 7.0	V
Short circuit output current	I_{OS}	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	−	0 to + 70	°C
Storage temperature	Tstg	−	− 55 to + 125	°C

• Recommended Operating Conditions (Ta = 0 to + 70°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	−	4.5	5.0	5.5	V
	V_{SS}	−	0	0	0	V
Input high voltage	V_{IH}	−	2.4	−	V_{CC} + 1.0	V
Input low voltage	V_{IL}	−	− 1.0	−	0.8	V

• DC Characteristics

(V_{CC} = 5V ± 10%, Ta = 0 to + 70°C)

Parameter	Symbol	Conditions		MSM51C256 -80 Min	MSM51C256 -80 Max	MSM51C256 -10 Min	MSM51C256 -10 Max	Unit	Note
Output high voltage	V_{OH}	I_{OH} = − 5.0mA		2.4	−	2.4	−	V	
Output low voltage	V_{OL}	I_{OL} = 4.2mA		−	0.4	−	0.4	V	
Input leakage current	I_{LI}	$V_{SS} \leqq VI \leqq V_{CC}$ all other pins not under test = 0V		− 10	10	− 10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable $V_{SS} \leqq VO \leqq V_{CC}$		− 10	10	− 10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min		−	60	−	50	mA	
Power supply current" (Standby)	I_{CC2}	$\overline{RAS} = V_{IH}$ $\overline{CAS} = V_{IH}$ D_{OUT} = Hz	TTL	−	3.5	−	3.5	mA	
			MOS	−	2.5	−	2.5	mA	
Average power supply current* (RAS only refresh)	I_{CC3}	$\overline{RAS}$ = cycling, $\overline{CAS} = V_{IH}$ t_{RC} = min		−	60	−	50	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ = cycling, $\overline{CAS}$ before $\overline{RAS}$		−	60	−	50	mA	
Average power supply current* (Fast page mode)	I_{CC7}	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ = cycling t_{PC} = min		−	40	−	35	mA	

*Note: I_{CC} is dependent on output loading and cycle. Specified values are obtained with the output open.

• Capacitance

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A8, D_{IN})	C_{IN1}	−	−	4	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	−	−	5	pF
Output capacitance (D_{OUT})	C_{OUT}	−	−	6	pF

● AC Characteristics

(V_{CC} = 5V ± 10%, Ta = 0 to + 70°C) Note 1, 2, 3

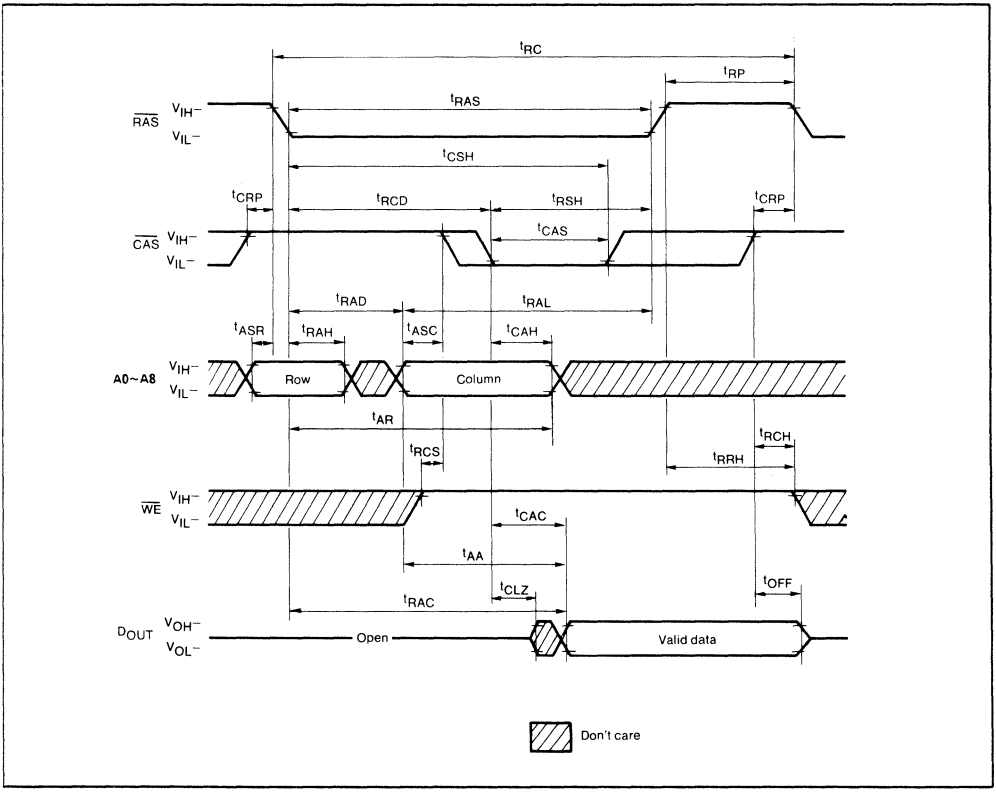
Parameter	Symbol	MSM51C256 -80		MSM51C256 -10		Unit	Note
		Min	Max	Min	Max		
Refresh period	t_{REF}	–	4	–	4	ms	
Random read or write cycle time	t_{RC}	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	185	–	220	–	ns	
Fast page mode cycle time	t_{PC}	55	–	55	–	ns	
Fast page mode read/write cycle time	t_{PRWC}	80	–	90	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	ns	4.5
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	ns	4.5
Access time from column address	t_{AA}	–	40	–	50	ns	4.6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	50	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	30	ns	
Transition time	t_T	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10K	100	10K	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10K	25	10K	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	ns	

• AC Characteristics (Cont.)

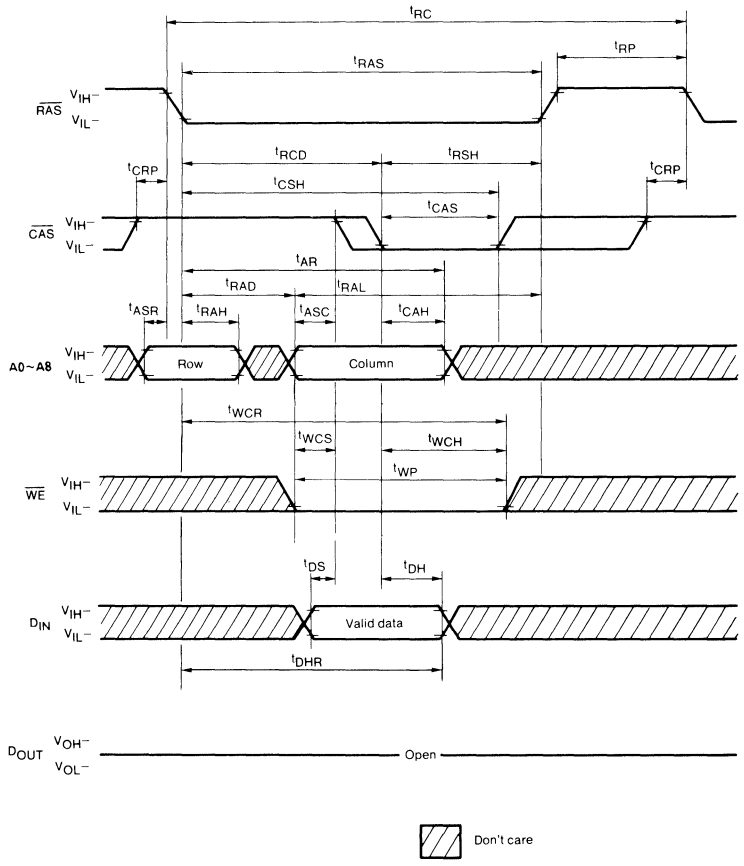
Parameter	Symbol	MSM51C256 -80		MSM51C256 -10		Unit	Note
		Min	Max	Min	Max		
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	ns	8
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	ns	7
Write command hold time	t_{WCH}	15	–	20	–	ns	
Write command pulse width	t_{WP}	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20	–	25	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80	–	100	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	40	–	50	–	ns	7
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	15	–	ns	

Notes:
1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if t_{CWD} (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{RWD}$ (min.) the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

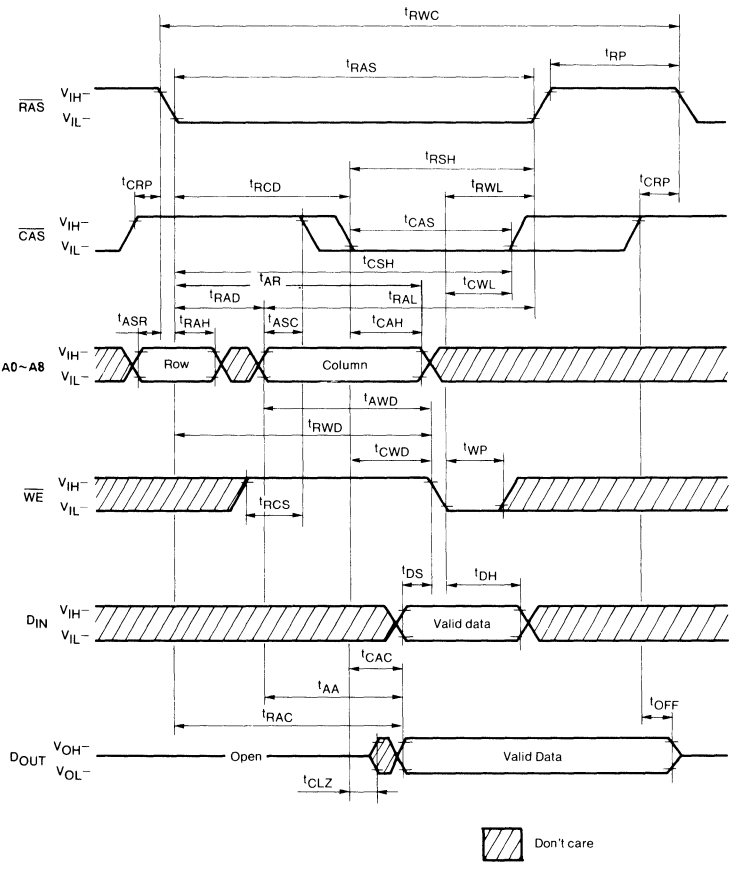
READ CYCLE



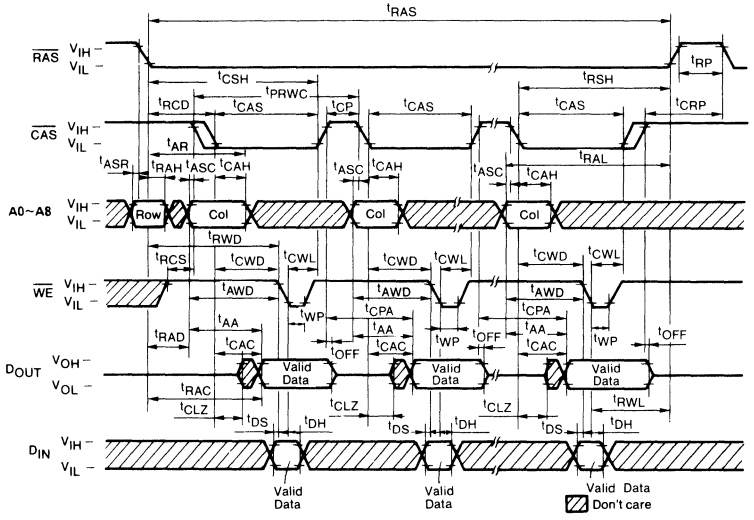
WRITE CYCLE (EARLY WRITE)



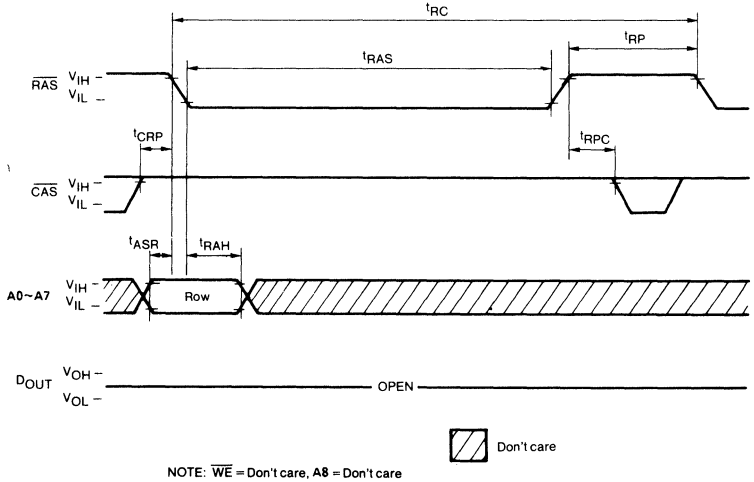
READ/WRITE CYCLE



FAST PAGE MODE READ/WRITE CYCLE

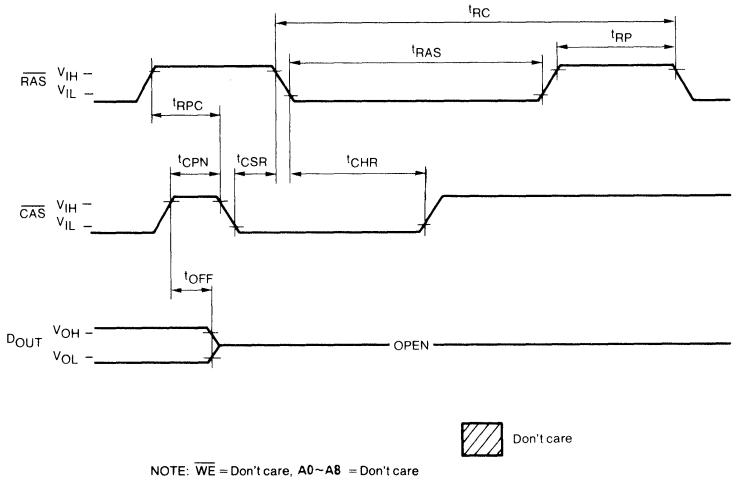


RAS ONLY REFRESH CYCLE



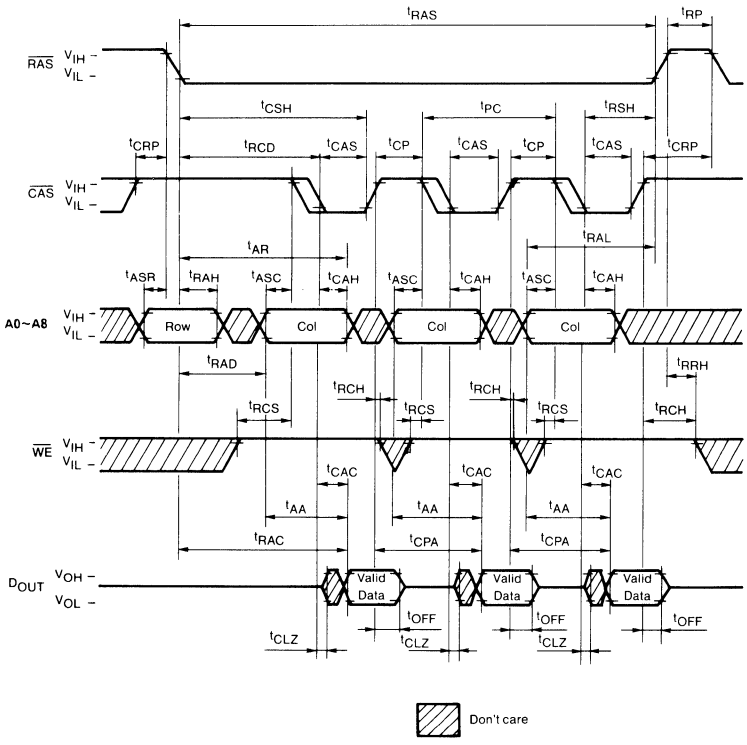
NOTE: $\overline{WE}$ = Don't care, A8 = Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

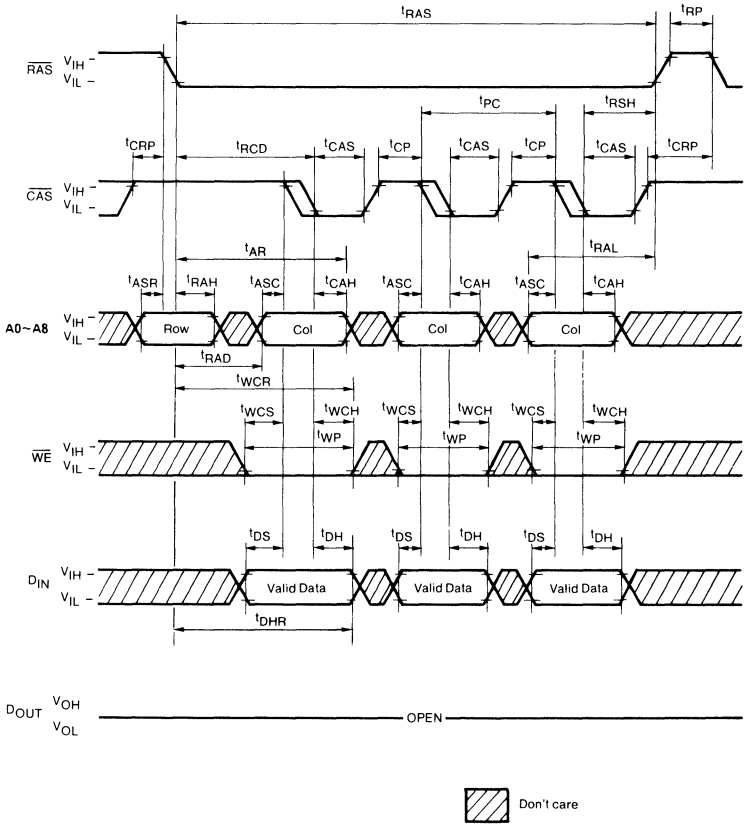


NOTE: $\overline{WE}$ = Don't care, A0~A8 = Don't care

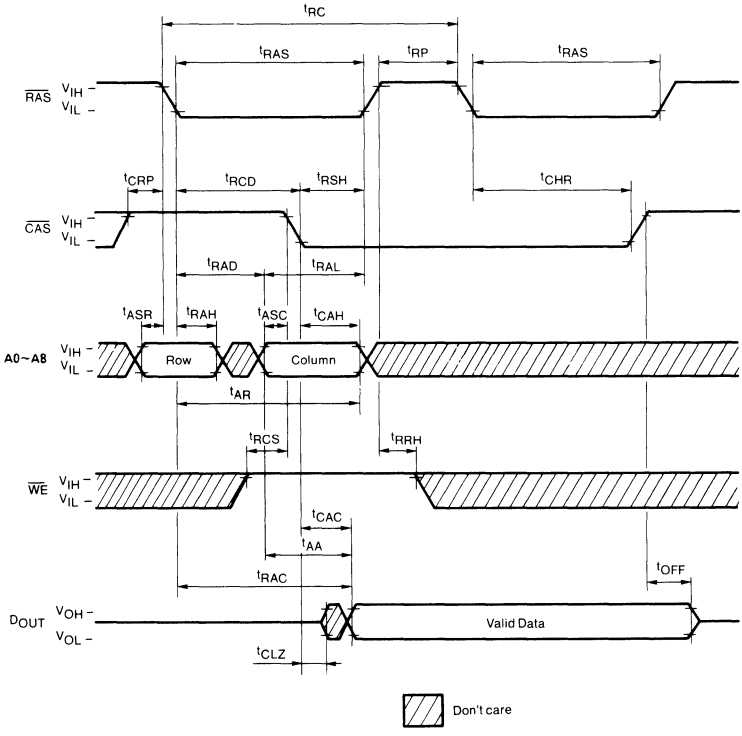
FAST PAGE MODE READ CYCLE



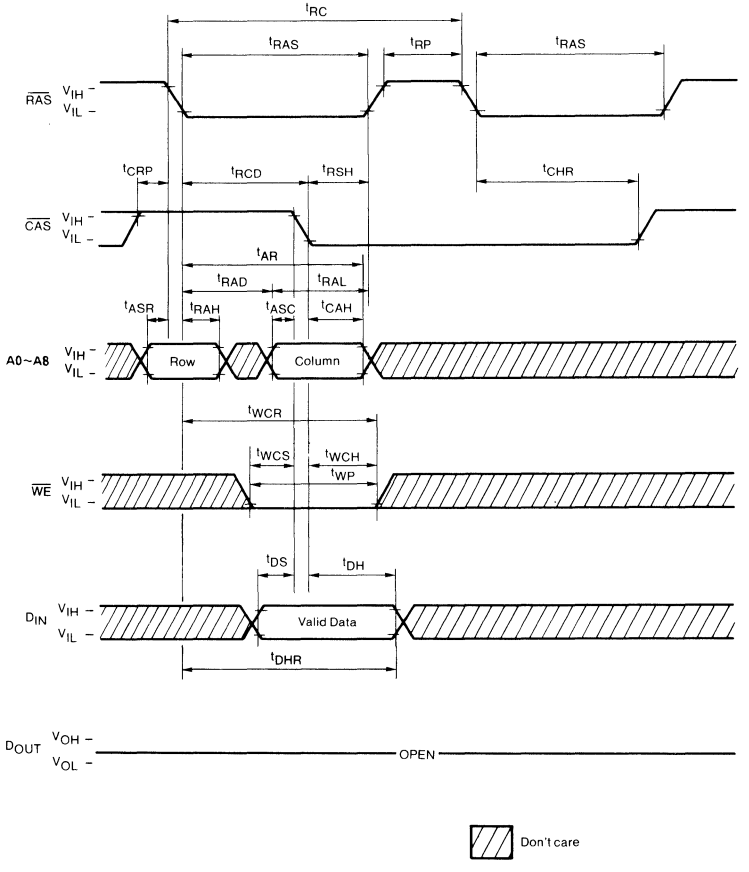
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



FUNCTIONAL DESCRIPTION

Simple timing Requirements:

The MSM51C256 is a CMOS dynamic RAM optimized for high speed access time operations, low power applications. It is functionally similar to a traditional dynamic RAM. The MSM51C256 reads and writes data by multiplexing 18-bit address into 9-bit row and 9-bit column address. Because access time is primarily dependent on a valid column address rather than the precise time that $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ (t_{RCD}) has little effect on the access time. And the MSM51C256 can commit better memory system through-put during operations in an interleared system.

Fast-Read-While-Write Cycle:

The MSM51C256 has the fast read while write cycle which is achieved by excellent control of the three-state output buffer in adition to the simplified timings described in the previous section. The output buffer is controlled by the state of $\overline{WE}$ when $\overline{CAS}$ goes low. When $\overline{WE}$ is low during $\overline{CAS}$ transition to low, the MSM51C256 goes to early write mode where the output becomes floating and common I/O bus can be used on the system level. Whereas, when $\overline{WE}$ goes low after t_{CWD} following $\overline{CAS}$ transition to low, the MSM51C256 goes to delayed write mode where the output contains the data from the cell selected and the data from D_{IN} is written into the cell selected. Therefore, very fast read write cycle becomes available.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSM51C256. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column adress bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$, $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Addres Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed form row-addresses to column-addreses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSM51C256 during a write or read-write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. In a read-write cycle, $\overline{WE}$ will be delayed until $\overline{CAS}$ has made its negative transition. Thus D_{IN} is storbed by $\overline{WE}$, and set-up and hold times are referenced to $\overline{WE}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max.). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSM51C256 offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{CSR}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSM51C256 hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresha ddresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

MSM511000A

1,048,576-WORD × 1-BITS DYNAMIC RAM

GENERAL DESCRIPTION

The MSM511000A is a new generation dynamic RAM organized as 1,048,576 words by 1 bit. The technology used to fabricate the MSM511000A is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

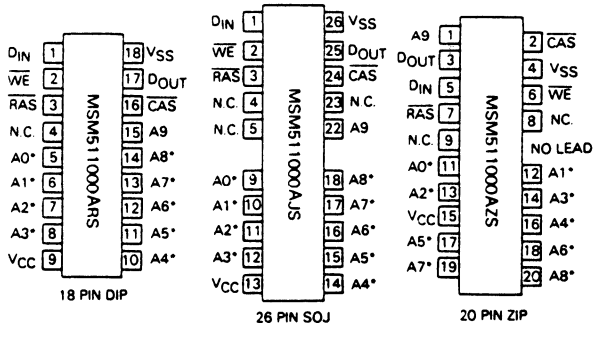
FEATURES

- Silicon gate, tripple polysilicon CMOS, 1-transistor memory cell
- Family organization
- 1,048,576 words by 1 bit

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM511000A-70	70ns	140ns	468mW	5.5mW
MSM511000A-8A/80	80ns	160ns	413mW	
MSM511000A-1A/10	100ns	190ns	358mW	

- Single +5V supply, ± 10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using "Early Write" operation
- Fast page mode, read/write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit

PIN CONFIGURATION (TOP VIEW)

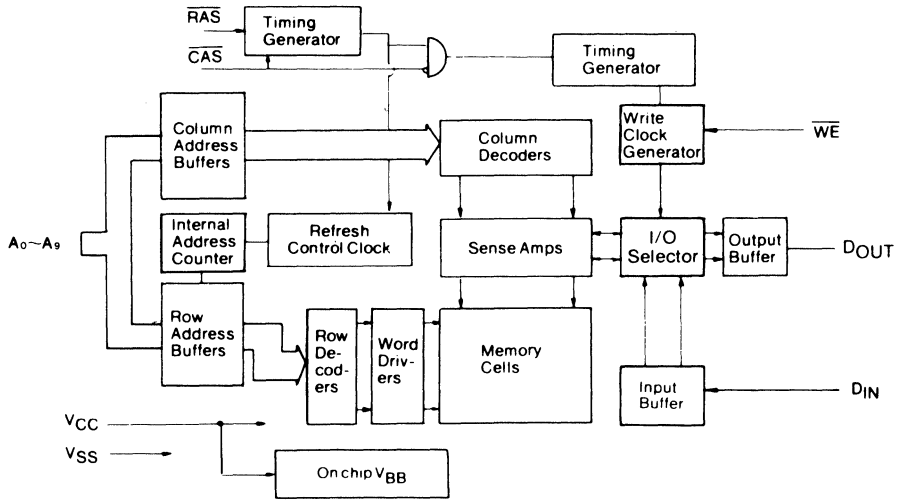


* Refresh Address

Pin Names	Function
A0 to A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
N.C.	No Connection

4

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta=25°C	−1.0 to+7.0	V
Short circuit output current	Ios	Ta=25°C	50	mA
Power dissipation	P_D	Ta=25°C	1	W
Operating temperature	Topr	–	0 to+70	°C
Storage temperature	Tstg	–	−55 to+150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions		MSM511000 A-8A		MSM511000 A-1A		MSM511000 A-70		MSM511000 A-80		MSM511000 A-10		Unit	Noto
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0mA		2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2mA		0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	OV≦VI≦6.5V; all oter pins not under test = OV		−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable OV≦VO≦5.5V		−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, T_{RC} = min		−	75	−	65	−	85	−	75	−	65	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = Hz	TTL	−	2	−	2	−	2	−	2	−	2	mA	
			MOS	−	1	−	1	−	1	−	1	−	1		
Average power supply current* ($\overline{RAS}$only represh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min		−	75	−	65	−	85	−	75	−	65	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$		−	75	−	65	−	85	−	75	−	65	mA	
Average power supply current* (Fast page mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min		−	55	−	55	−	70	−	60	−	55	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A9, D_{IN})	C_{IN1}	−	−	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	−	−	7	pF
Output capacitance (D_{OUT})	C_{OUT}	−	−	7	pF

4

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSM511000 A-8A		MSM511000 A-1A		MSM511000 A-70		MSM511000 A-80		MSM511000 A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REP}	–	8	–	8	–	8	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	160	–	190	–	140	–	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	185	–	220	–	165	–	185	–	220	–	ns	
Fast page mode cycle time	t_{PC}	55	–	55	–	45	–	50	–	55	–	ns	
Fast page mode read/write cycle time	t_{PRWC}	80	–	85	–	70	–	75	–	85	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	70	–	80	–	100	ns	4.5
Access time from $\overline{CAS}$	t_{CAC}	–	25	–	30	–	20	–	20	–	25	ns	4.5
Access time fro columu address	t_{AA}	–	40	–	50	–	35	–	40	–	50	ns	4.6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	50	–	50	–	40	–	45	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	0	–	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ prechrge time	t_{RP}	70	–	80	–	60	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	70	10000	80	10000	100	10000	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100000	100	100000	70	100000	80	100000	100	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25	–	30	–	20	–	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	30	10000	20	10000	20	10000	25	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	70	–	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	55	25	70	22	50	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	17	35	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	10	–	10	–	ns	
Row address set-time	t_{ASR}	0	–	0	–	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	12	–	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	15	–	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	55	–	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	35	–	40	–	50	–	ns	

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM511000 A-8A		MSM511000 A-1A		MSM511000 A-70		MSM511000 A-80		MSM511000 A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	–	0	–	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	0	–	0	–	ns	8
Write connand hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	55	–	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	0	–	0	–	0	–	ns	7
Write command hold time	t_{WCH}	15	–	20	–	15	–	15	–	20	–	ns	
Write command pulse width	t_{WP}	15	–	20	–	15	–	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	20	–	20	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	25	–	20	–	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	15	–	15	–	20	–	ns	
Data-ds hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	55	–	60	–	75	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	25	–	30	–	20	–	20	–	25	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80	–	100	–	70	–	80	–	100	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	40	–	50	–	35	–	40	–	50	–	ns	7
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time (CAS before $\overline{RAS}$)	t_{CHR}	30	–	30	–	30	–	30	–	30	–	ns	
$\overline{CAS}$ active delay fron $\overline{RAS}$ preharge	t_{RPC}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	50	–	40	–	40	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	15	–	10	–	10	–	15	–	ns	

Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

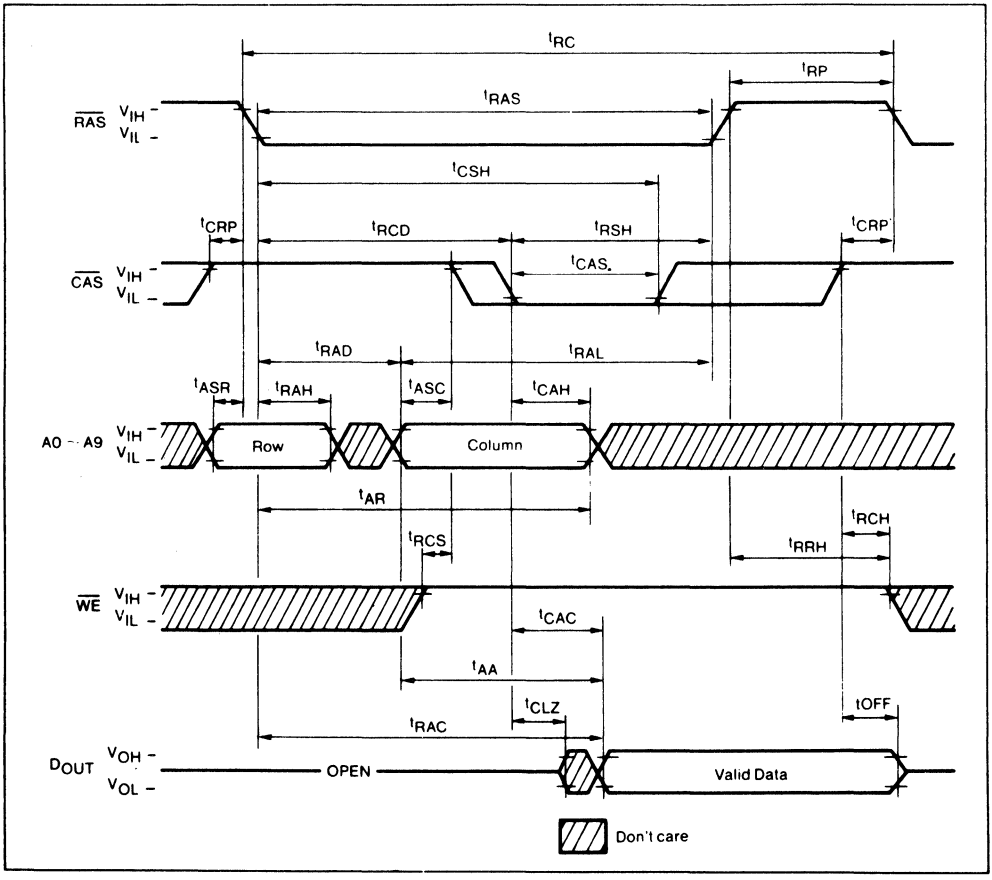
6 Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

7 t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

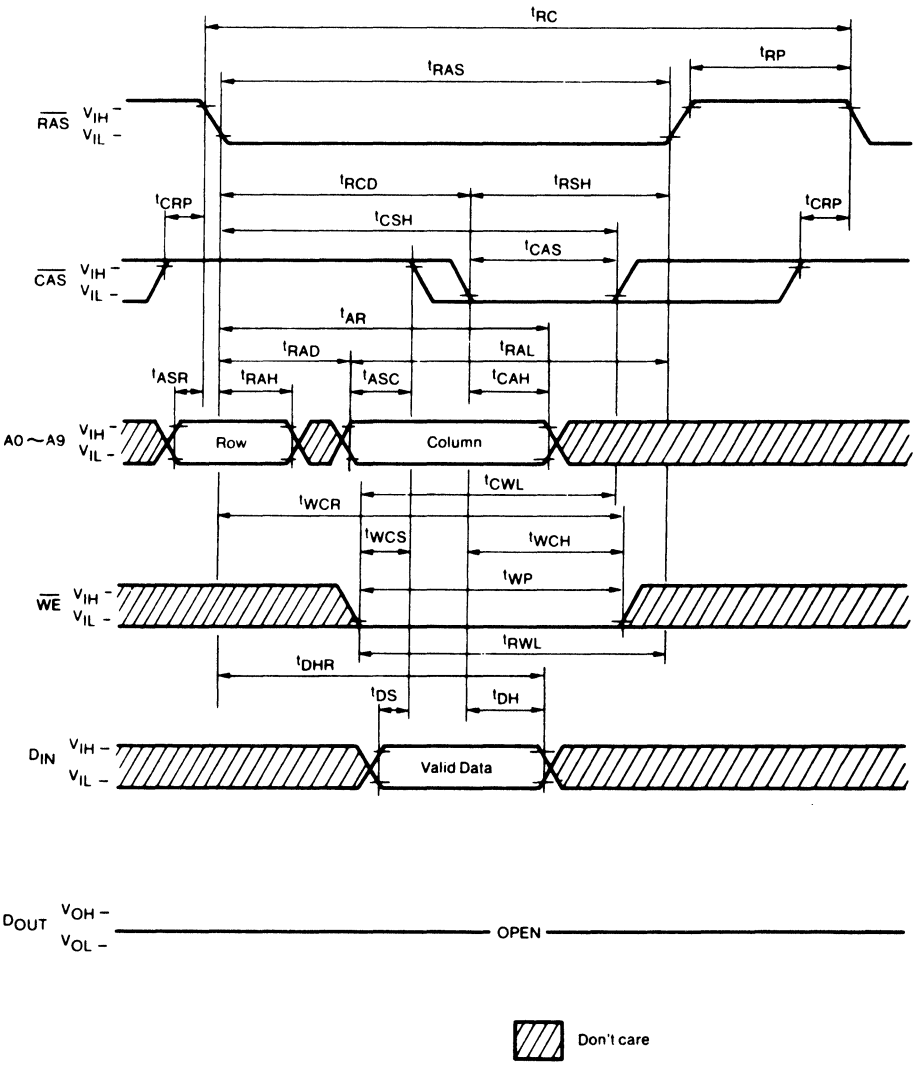
8 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

4

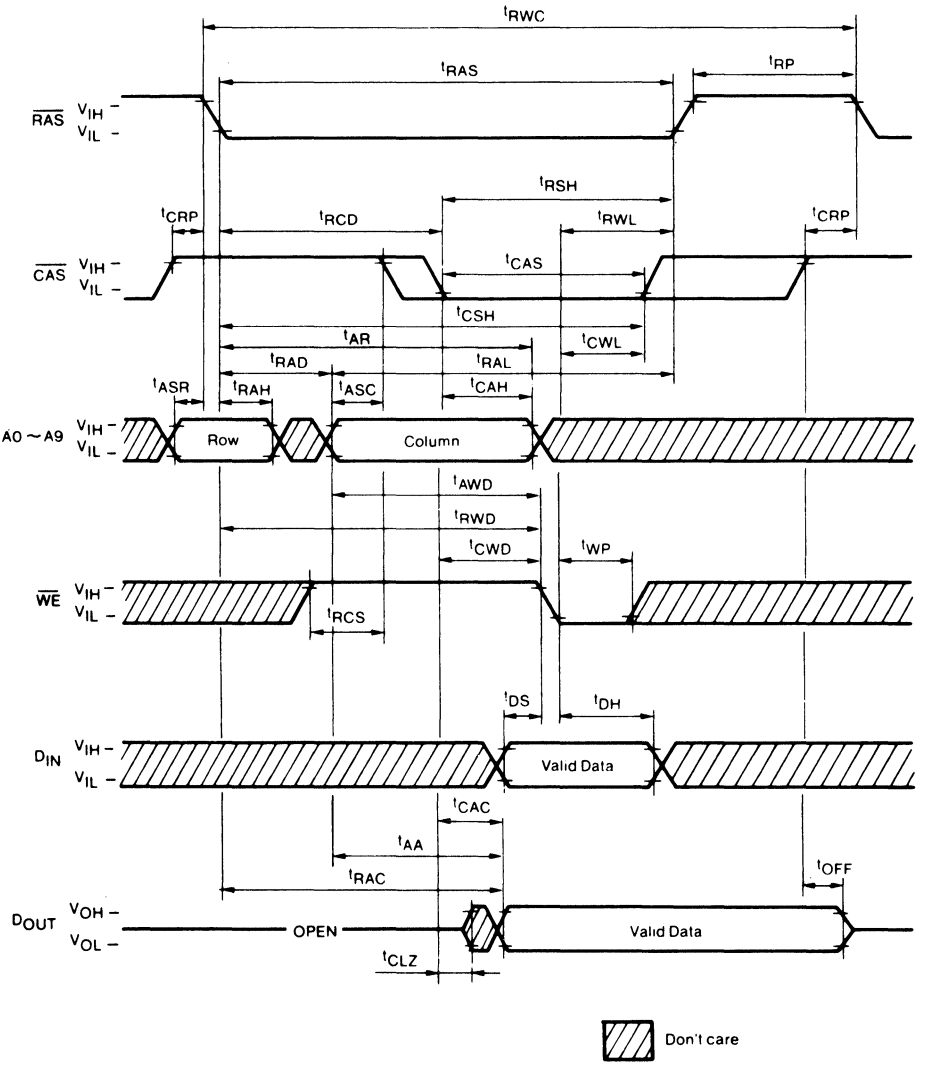
READ CYCLE



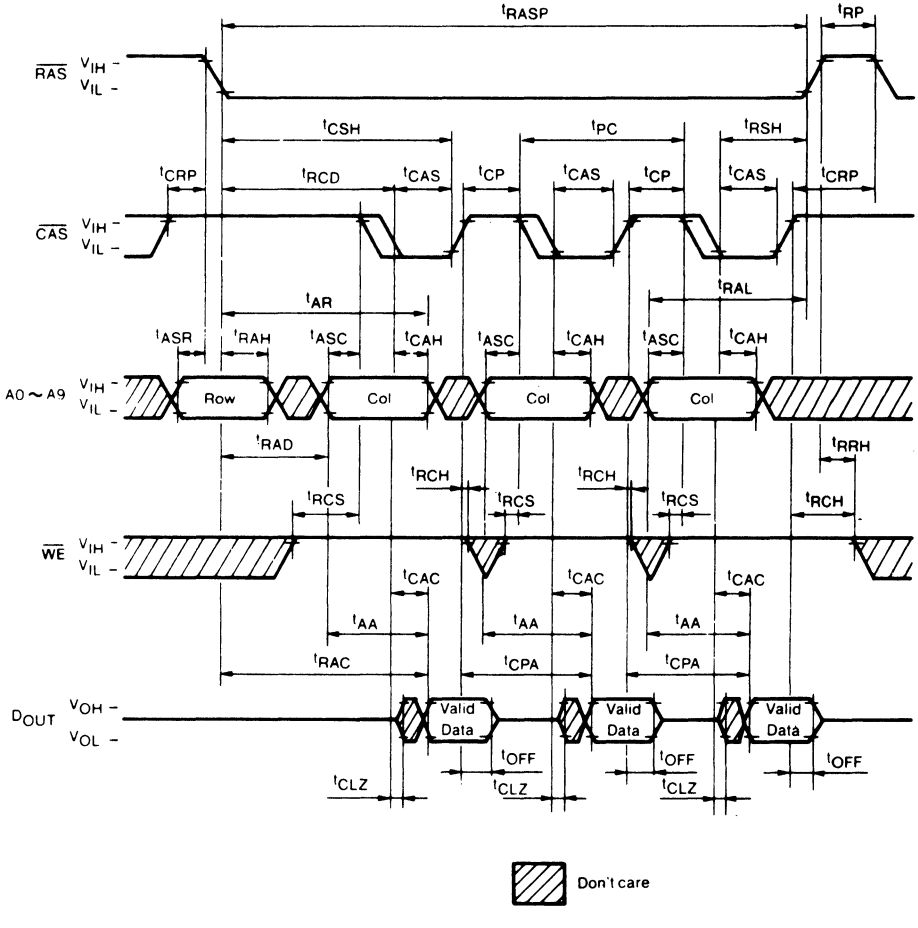
WRITE CYCLE (EARLY WRITE)



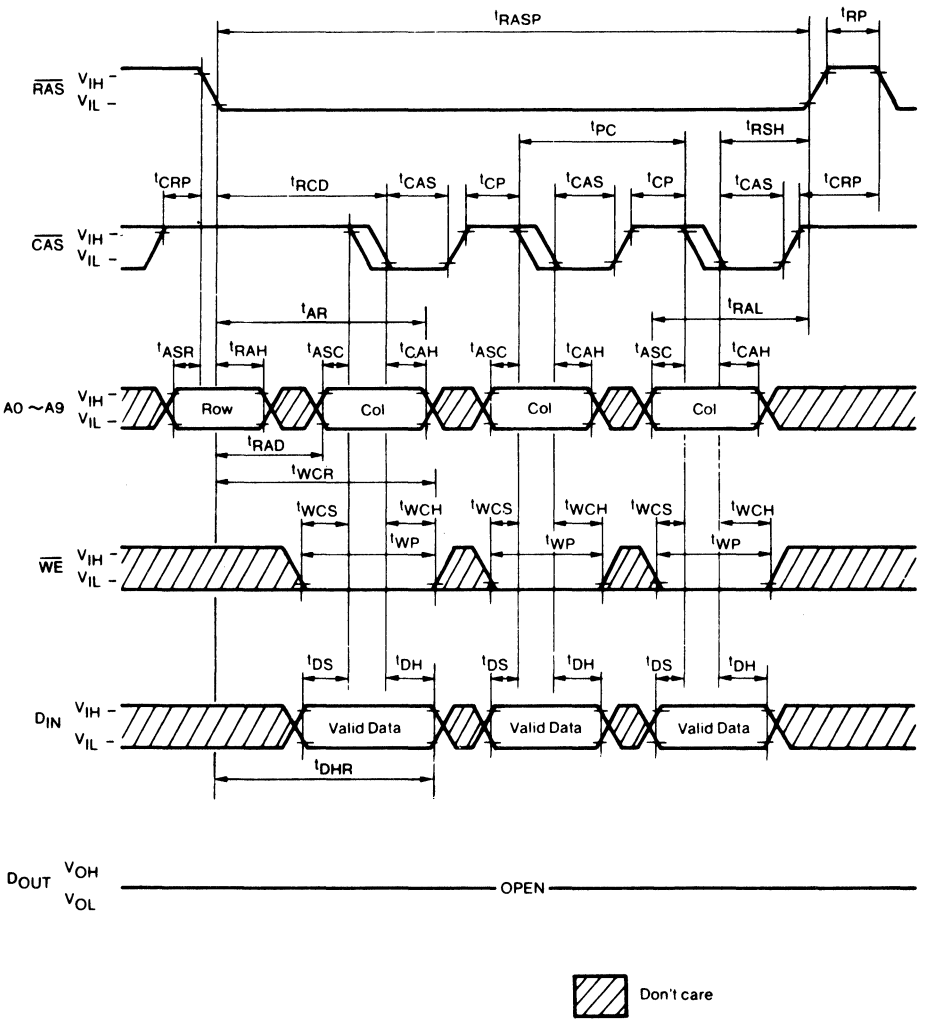
READ/WRITE CYCLE



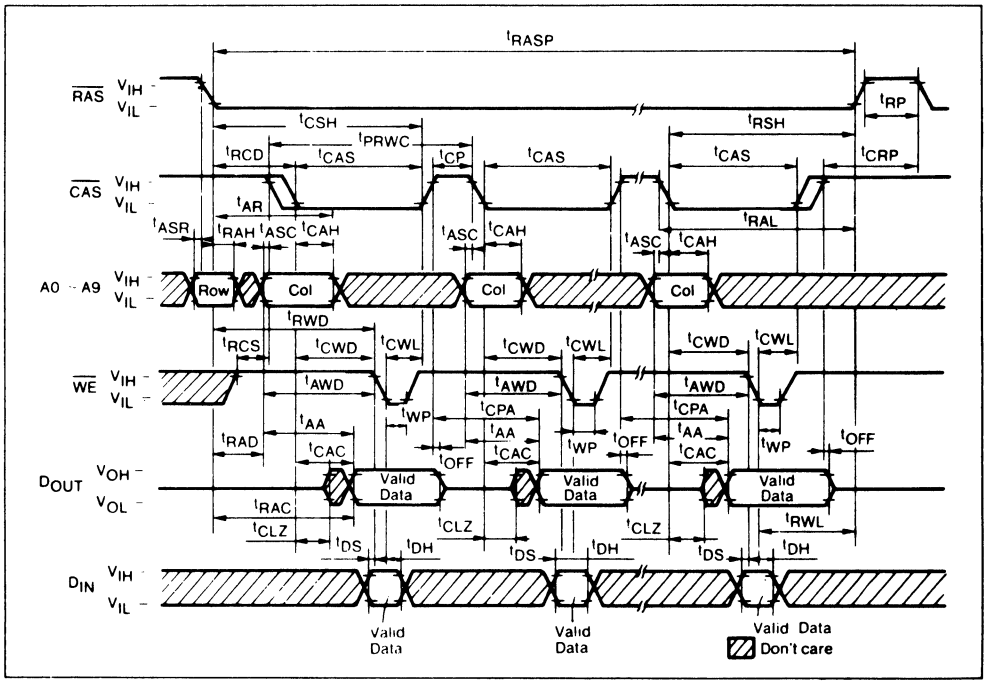
FAST PAGE MODE READ CYCLE



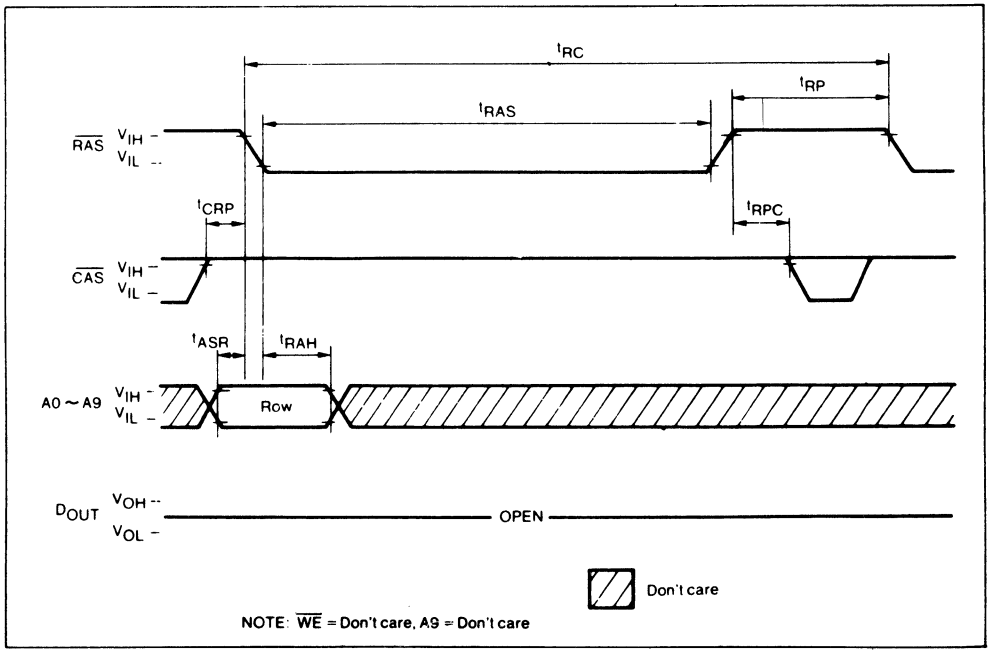
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



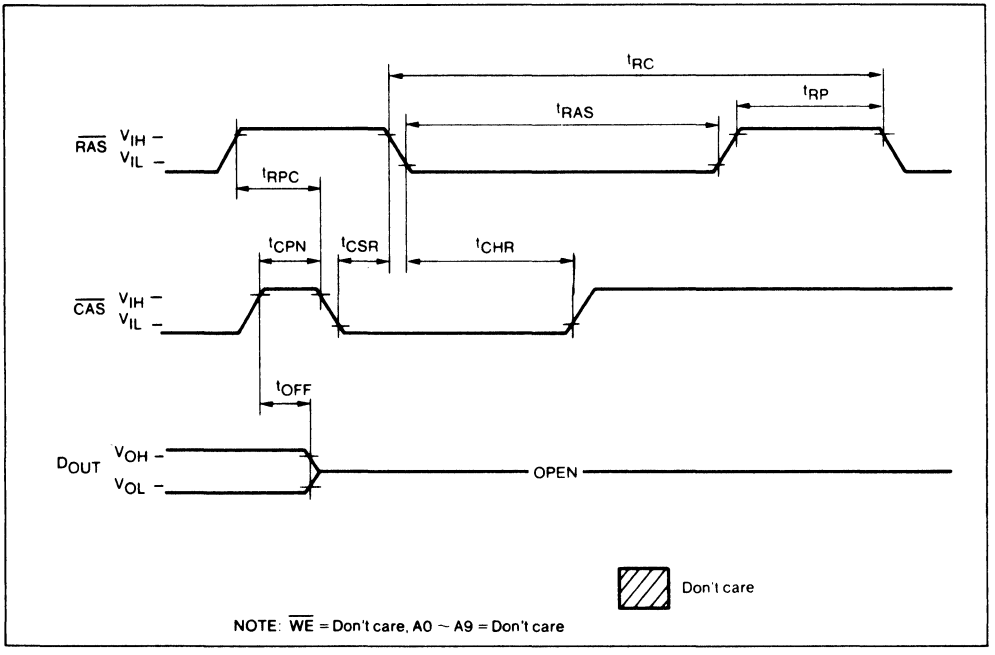
FAST PAGE MODE READ/WRITE CYCLE



RAS ONLY REFRESH CYCLE

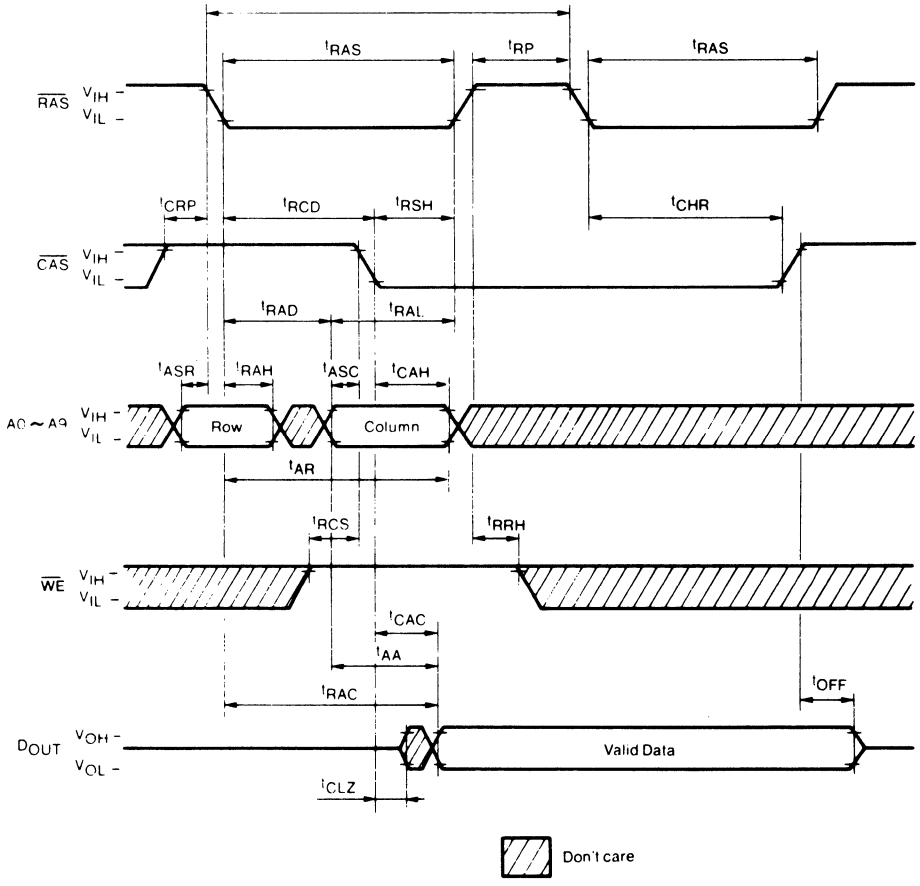


$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE

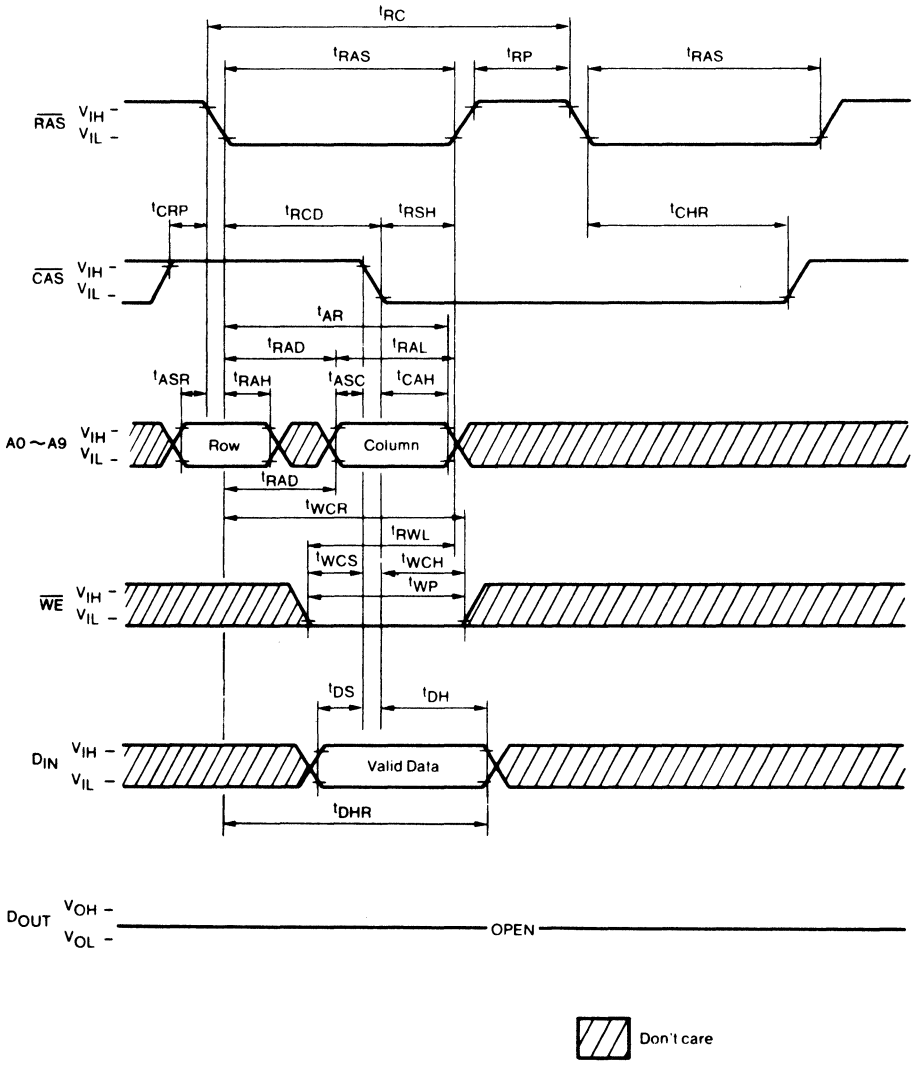


NOTE: $\overline{WE}$ = Don't care, A0 ~ A9 = Don't care

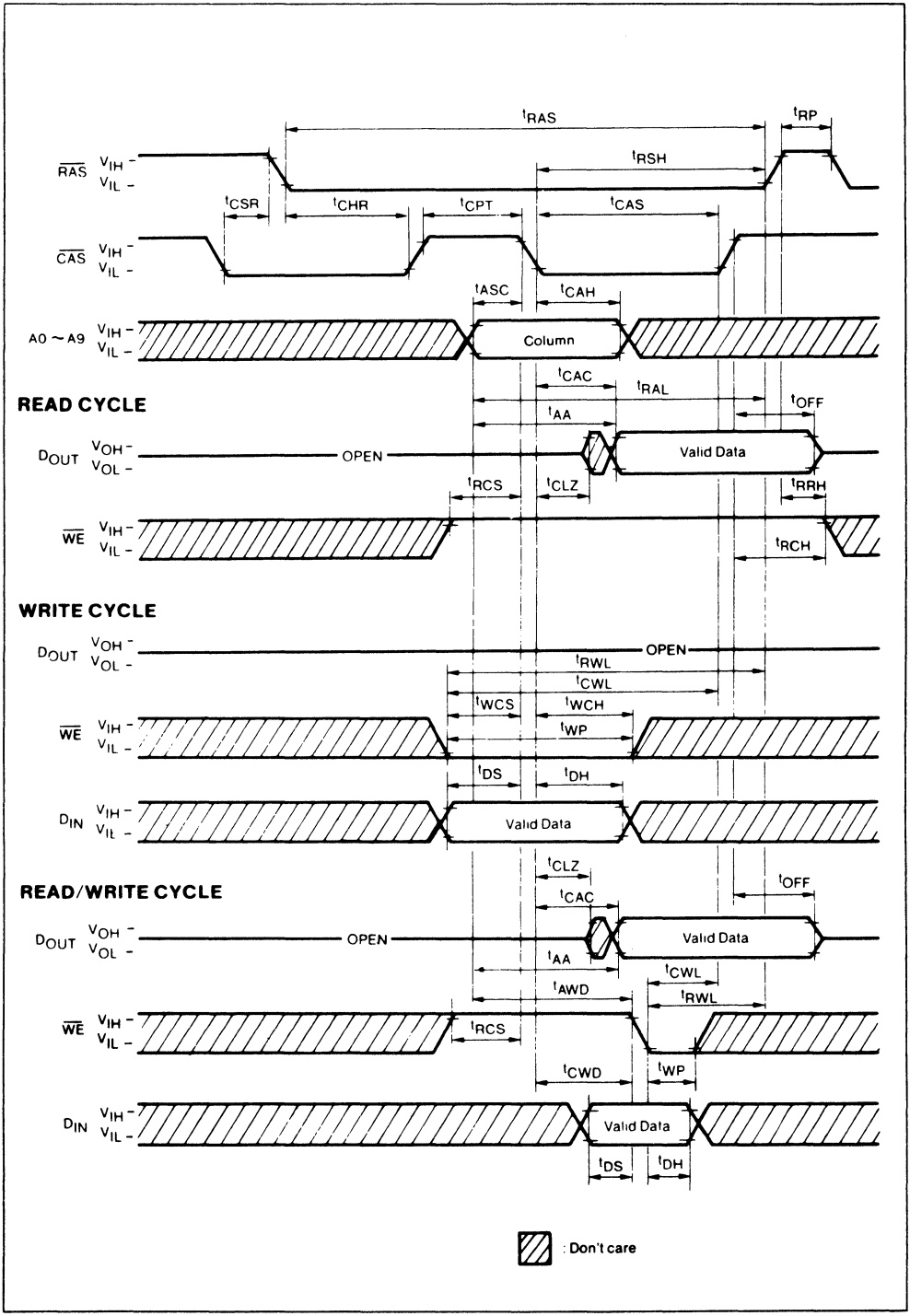
HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



OKI semiconductor

MSM511001A

1,048,576-WORD × 1-BITS DYNAMIC RAM

GENERAL DESCRIPTION

The MSM511001A is a new generation dynamic RAM organized as 1,048,576 words by 1 bit. The technology used to fabricate the MSM511001A is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

FEATURES

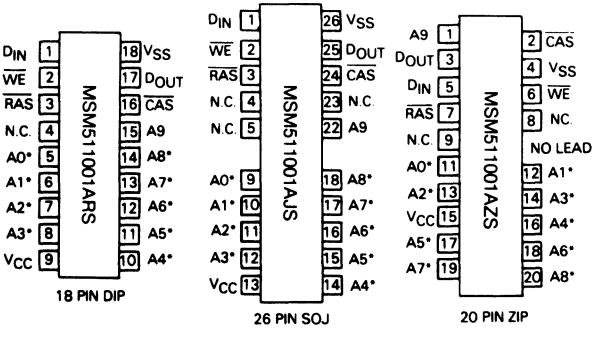
4

- Silicon gate, tripple polysilicon CMOS, 1-transistor memory cell
- Family organization
- 1,048,576 words by 1 bit

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM511001A-70	70ns	140ns	468mW	5.5mW
MSM511001A-8A/80	80ns	160ns	413mW	
MSM511001A-1A/10	100ns	190ns	358mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using "Early Write" operation
- Nibble mode, read/write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit

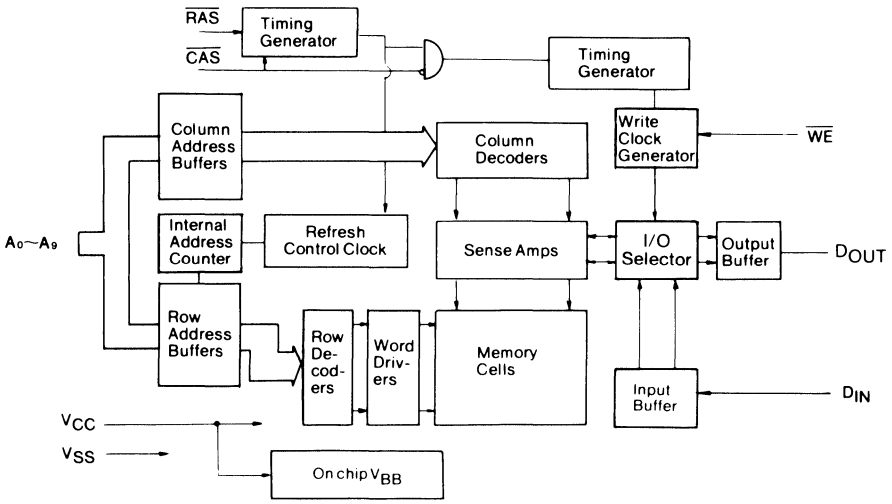
PIN CONFIGURATION (TOP VIEW)



* Refresh Address

Pin Names	Function
A0 to A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions		MSM 511001A-8A		MSM 511001A-1A		MSM 511001A-70		MSM 511001A-80		MSM 511001A-10		Unit	Noto
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0mA		2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2mA		0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	OV≦VI≦6.5V; all oter pins not under test=OV		−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable OV≦VO≦5.5V		−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC}=min		–	75	–	65	–	85	–	75	–	65	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH} $\overline{CAS}$=V_{IH} D_{OUT}=Hz	TTL	–	2	–	2	–	2	–	2	–	2	mA	
			MOS	–	1	–	1	–	1	–	1	–	1		
Average power supply current* ($\overline{RAS}$ only represh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min		–	75	–	65	–	85	–	75	–	65	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$		–	75	–	65	–	85	–	75	–	65	mA	
Average power supply current* (Nibble mode)	I_{CC8}	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{NC}=min		–	55	–	50	–	70	–	60	–	55	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A9, D_{IN})	C_{IN1}	–	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	–	–	7	pF
Output capacitance (D_{OUT})	C_{OUT}	–	–	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSM 511001A-8A		MSM 511001A-1A		MSM 511001A-70		MSM 511001A-80		MSM 511001A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REP}	–	8	–	8	–	8	–	8	–	8	m	
Random read or write cycle time	t_{RC}	160	–	190	–	140	–	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	185	–	220	–	165	–	185	–	220	–	ns	
Nibble mode cycle time	t_{NC}	55	–	60	–	50	–	50	–	55	–	ns	
Nibble mode read/write cycle time	t_{NRMW}	80	–	90	–	75	–	75	–	85	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	70	–	80	–	100	ns	4,5,6
Access time from $\overline{CAS}$	t_{CAC}	–	25	–	30	–	20	–	20	–	25	ns	4, 5
Access time fro column address	t_{AA}	–	40	–	50	–	35	–	40	–	50	ns	4, 6
Nibble mode access time	t_{NCAC}	–	25	–	30	–	20	–	20	–	25	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	0	–	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ prechrge time	t_{RP}	70	–	80	–	60	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	70	10000	80	10000	100	10000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25	–	30	–	20	–	20	–	25	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	30	10000	20	10000	20	10000	25	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	70	–	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	55	25	70	22	50	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	17	35	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	10	–	10	–	ns	
Row address set-time	t_{ASR}	0	–	0	–	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	12	–	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	15	–	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	55	–	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	35	–	40	–	50	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	0	–	0	–	0	–	ns	

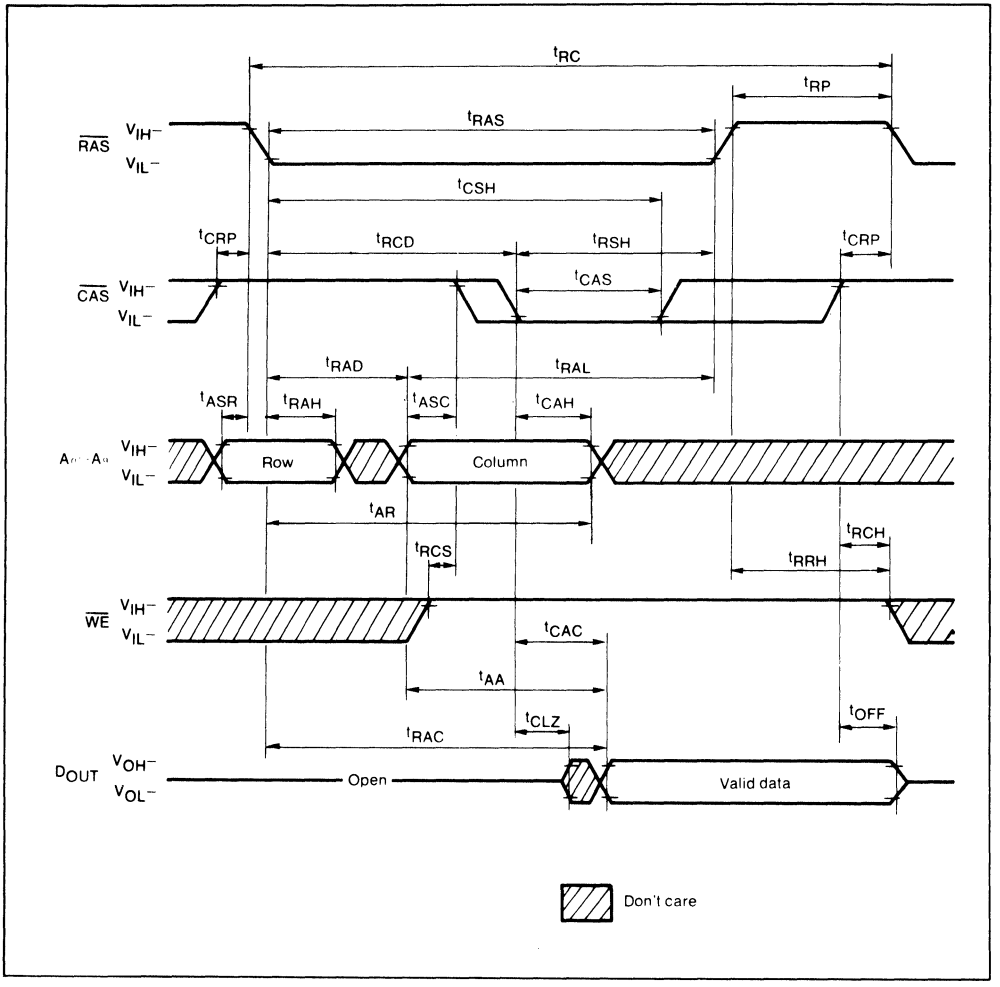
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM 511001A-8A		MSM 511001A-1A		MSM 511001A-70		MSM 511001A-80		MSM 511001A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read command hold time	t_{RCH}	0	–	0	–	0	–	0	–	0	–	ns	8
Write connand hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	55	–	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	0	–	0	–	0	–	ns	7
Write command hold time	t_{WCH}	15	–	20	–	15	–	15	–	20	–	ns	
Write command pulse width	t_{WP}	15	–	20	–	15	–	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	20	–	20	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	25	–	20	–	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	15	–	15	–	20	–	ns	
Data-ds hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	55	–	60	–	75	–	ns	7
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	25	–	30	–	20	–	20	–	25	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80	–	100	–	70	–	80	–	100	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	40	–	50	–	35	–	40	–	50	–	ns	7
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	30	–	30	–	30	–	ns	
$\overline{CAS}$ active delay fron $\overline{RAS}$ preharge	t_{RPC}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	50	–	40	–	40	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	15	–	10	–	10	–	15	–	ns	
Nibble mode pulse width	t_{NCAS}	25	–	30	–	20	–	20	–	25	–	ns	
Nibble mode $\overline{CAS}$ precharge time	t_{NCP}	20	–	20	–	20	–	20	–	20	–	ns	
Nibble mode $\overline{RAS}$ hold time	t_{NRSH}	25	–	25	–	20	–	20	–	25	–	ns	
Nibble mode $\overline{CAS}$ to $\overline{WE}$ delay	t_{NCWD}	25	–	30	–	20	–	20	–	25	–	ns	
Nibble mode write command to $\overline{RAS}$ lead time	t_{NRWL}	20	–	25	–	20	–	20	–	25	–	ns	
Nibble mode write command to $\overline{CAS}$ lead time	t_{NCWL}	20	–	25	–	20	–	20	–	25	–	ns	

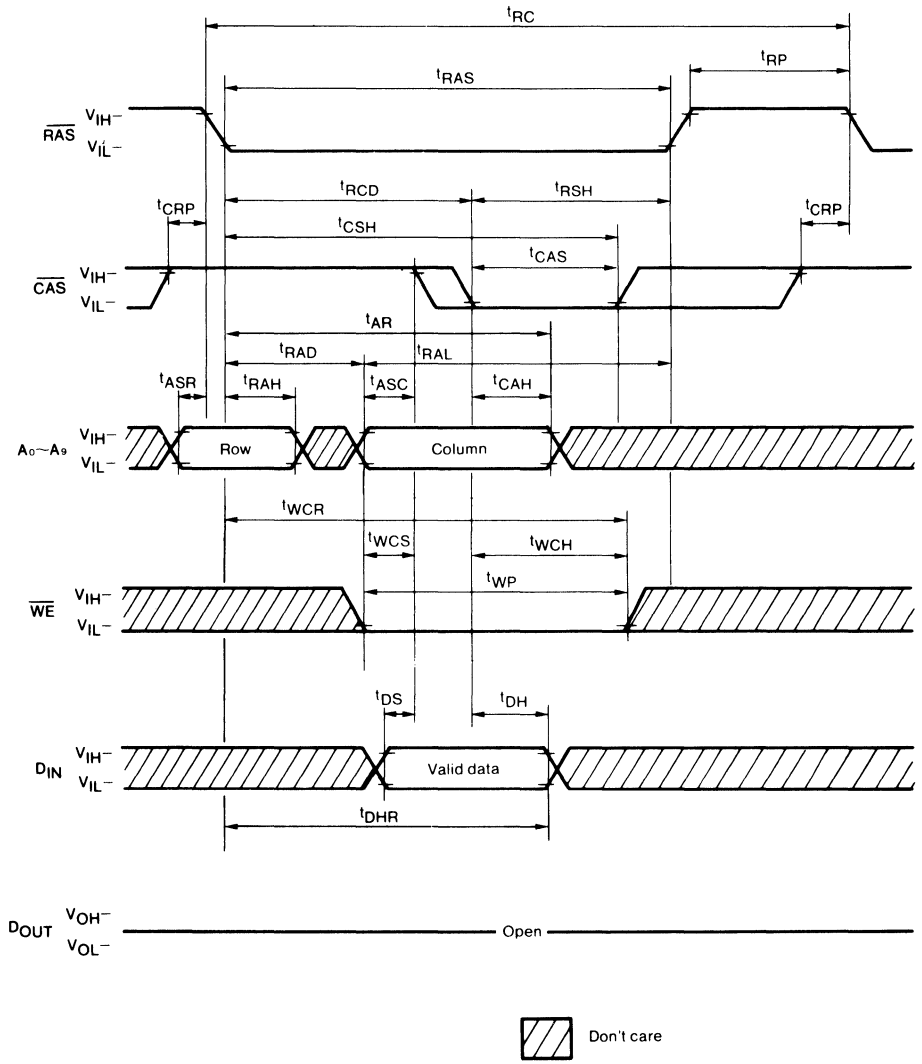
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

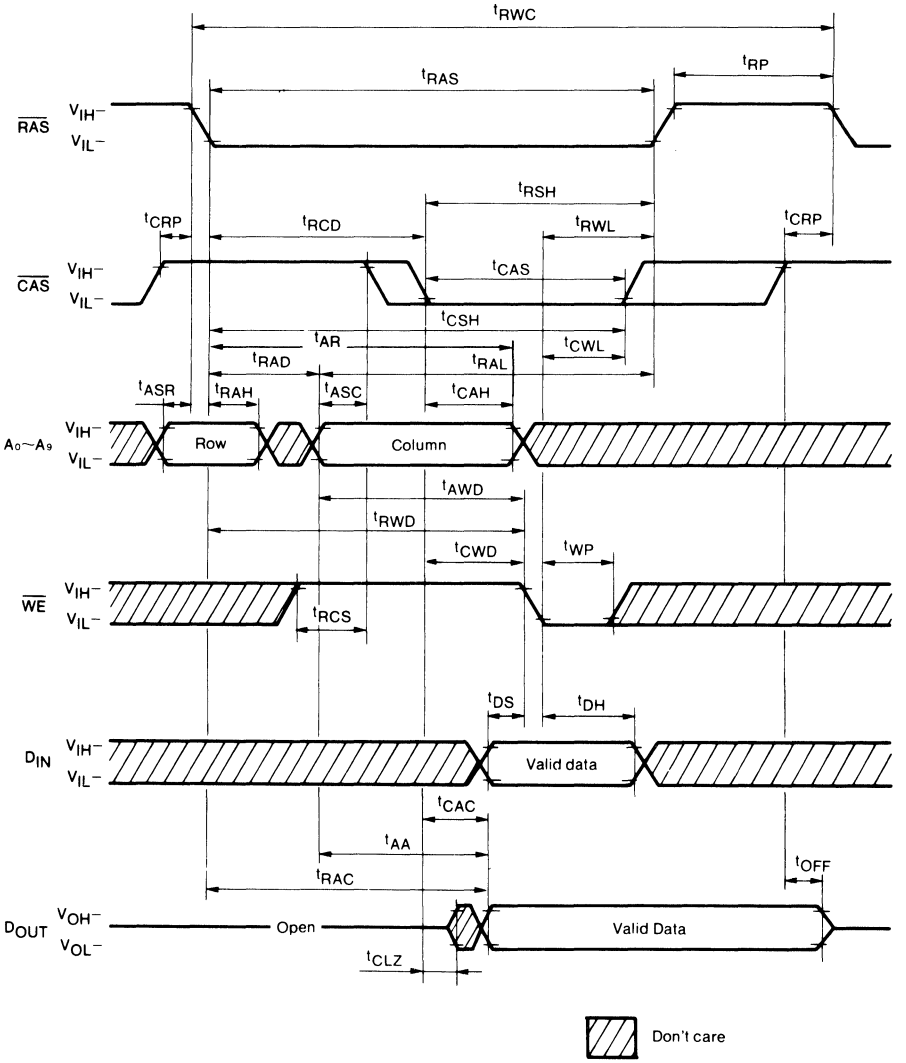
READ CYCLE


tRC
tRP
tRAS
RAS VIH− VIL−
tCSH
tCRP
tRCD
tRSH
tCRP
CAS VIH− VIL−
tCAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
A0−A9 VIH− VIL−
Row
Column
tAR
tRCS
tRCH
tRRH
WE VIH− VIL−
tCAC
tAA
tCLZ
tOFF
tRAC
DOUT VOH− VOL−
Open
Valid data
Don't care

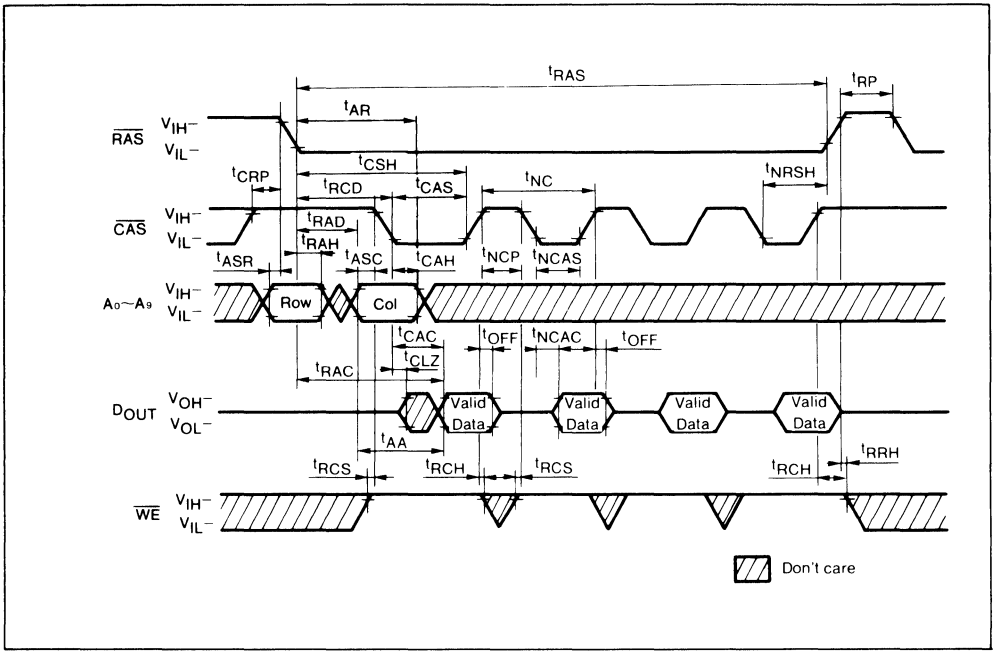
WRITE CYCLE (EARLY WRITE)



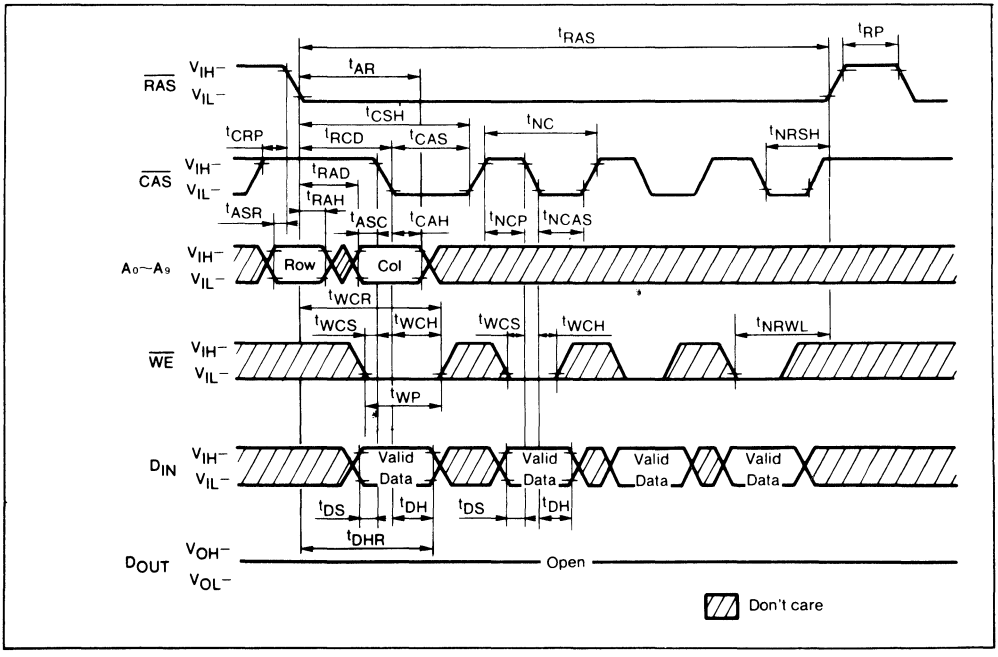
READ/WRITE CYCLE



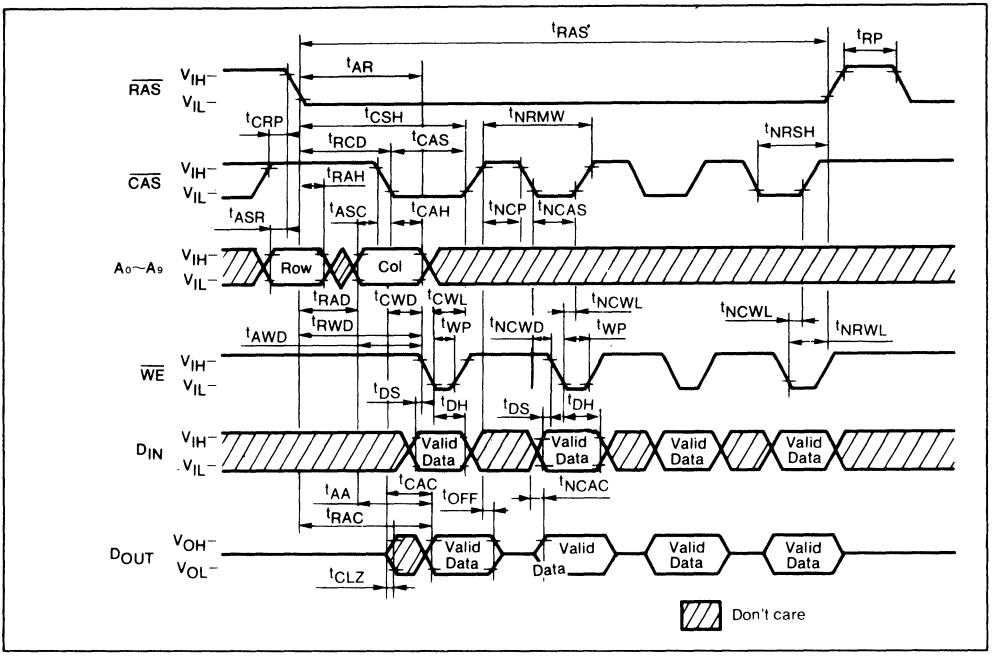
NIBBLE MODE READ CYCLE



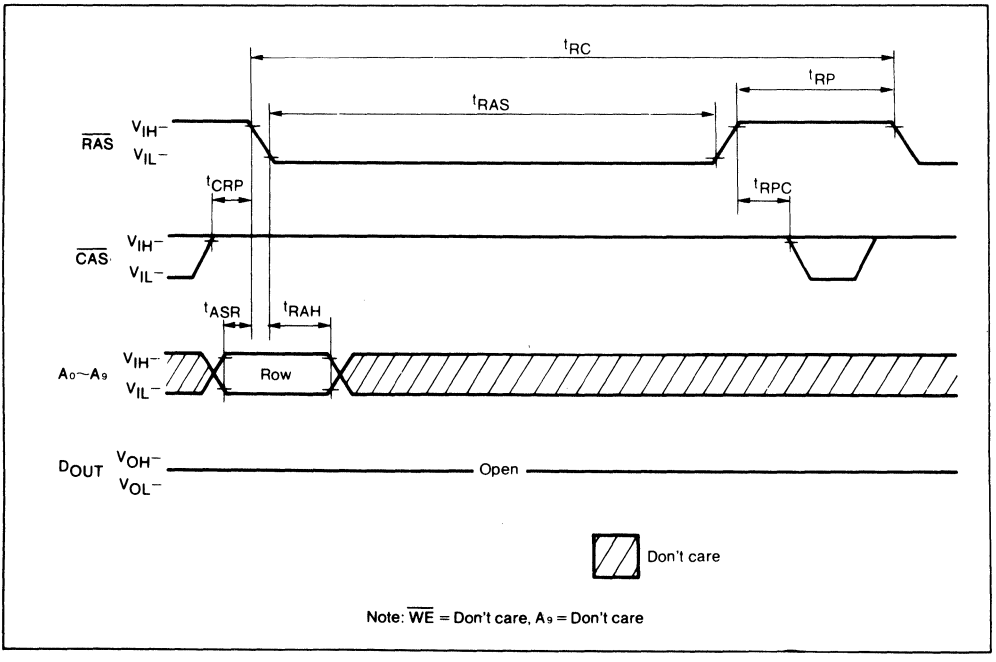
NIBBLE MODE WRITE CYCLE (EARLY WRITE)



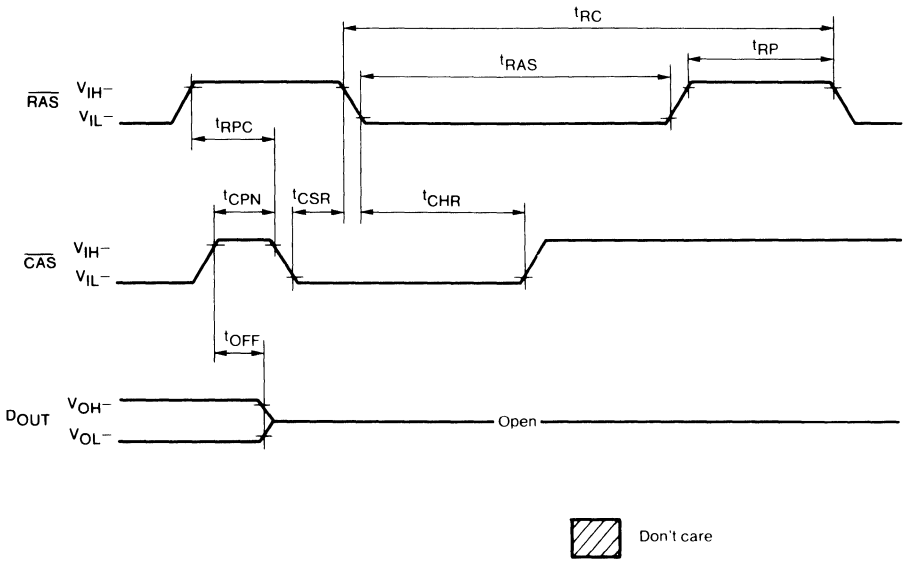
NIBBLE MODE READ/WRITE CYCLE



RAS ONLY REFRESH CYCLE

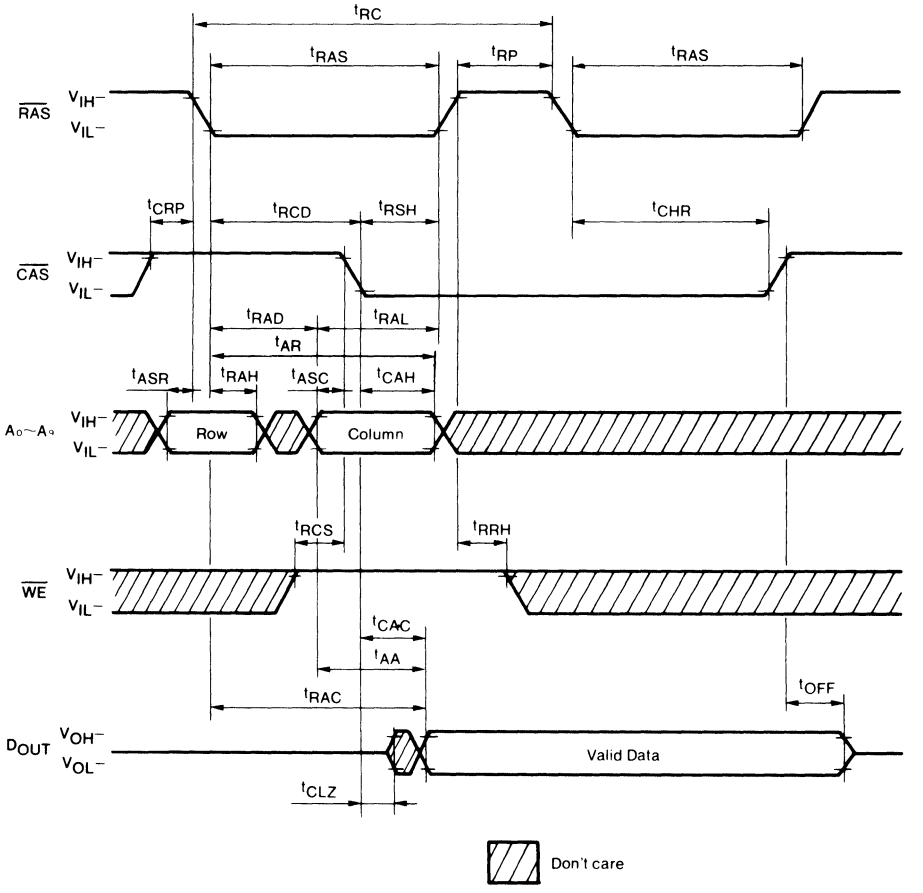


$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE

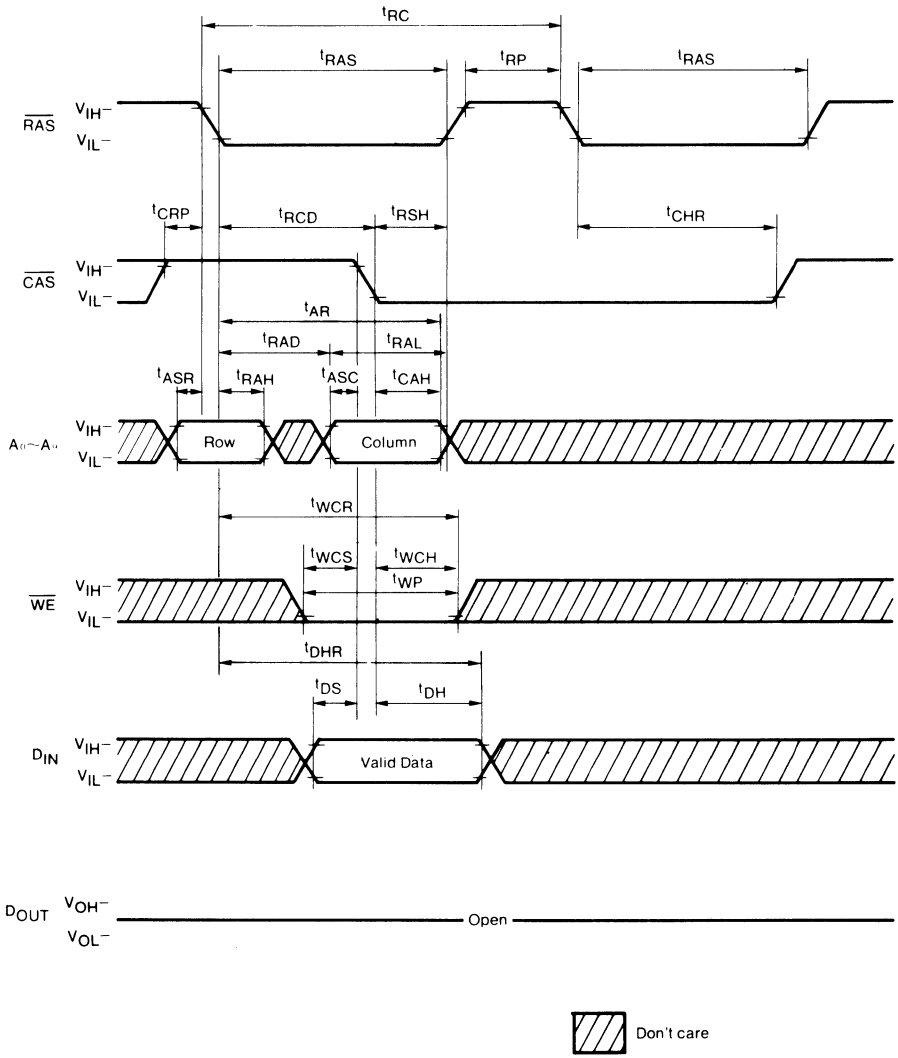


Note: $\overline{WE}$ = Don't care, $A_0 - A_9$ = Don't care

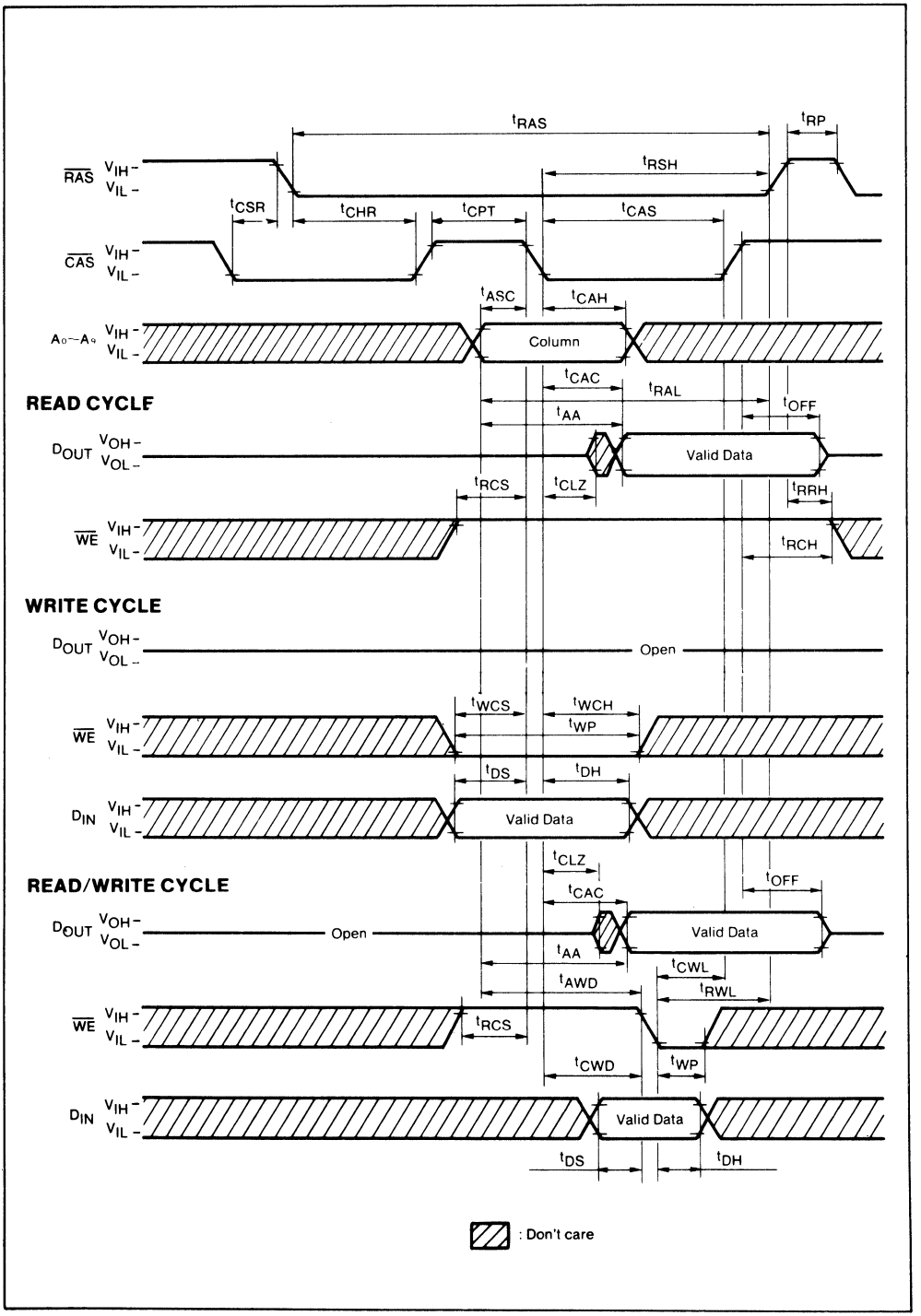
HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



OKI semiconductor

MSM511002A

1,048,576-WORD × 1-BITS DYNAMIC RAM

GENERAL DESCRIPTION

The MSM511002A is a new generation dynamic RAM organized as 1,048,576 words by 1 bit. The technology used to fabricate the MSM511002A is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

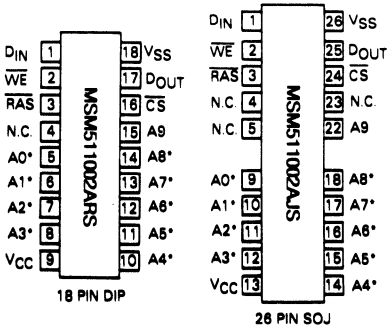
FEATURES

- Silicon gate, tripple polysilicon CMOS, 1-transistor memory cell
- Family organization
- 1,048,576 words by 1 bit

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM511002A-70	70ns	140ns	468mW	5.5mW
MSM511002A-8A/80	80ns	160ns	413mW	
MSM511002A-1A/10	100ns	190ns	358mW	

- Single +5V supply, ± 10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Common I/O capability using "Early Write" operation
- Static column mode, read/write capability
- $\overline{CS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$ only refresh capability
- Built-in V_{BB} generator circuit

PIN CONFIGURATION (TOP VIEW)

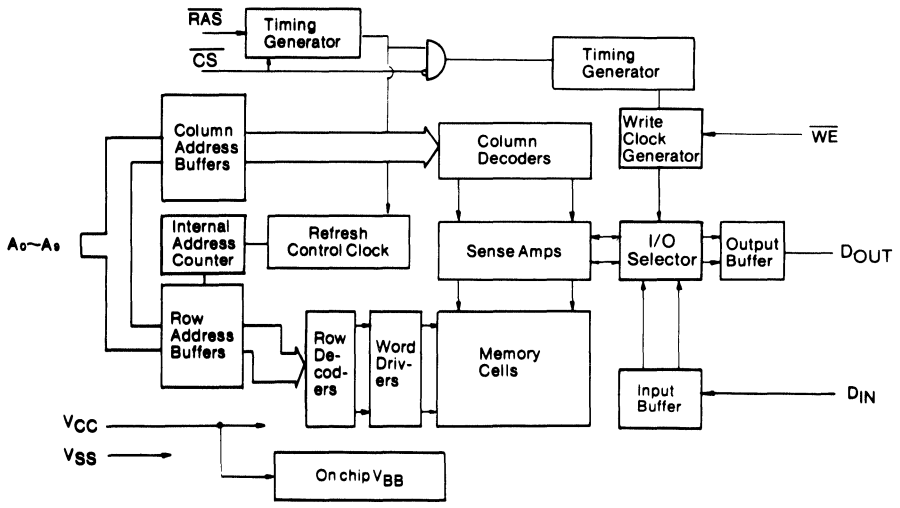


Pin Names	Function
A0 to A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip select Input
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
N.C	No Connection

* Refresh Address

4

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 511002A-8A		MSM 511002A-1A		MSM 511002A-70		MSM 511002A-80		MSM 511002A-10		Unit	Noto
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	OV≦VI≦6.5V; all oter pins not under test=OV	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable OV≦VO≦5.5V	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC}=min	−	75	−	65	−	85	−	75	−	65	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH} $\overline{CS}$=V_{IH} D_{OUT}=Hz TTL	−	2	−	2	−	2	−	2	−	2	mA	
		MOS	−	1	−	1	−	1	−	1	−	1		
Average power supply current* ($\overline{RAS}$ only represh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min	−	75	−	65	−	85	−	75	−	65	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	−	75	−	65	−	85	−	75	−	65	mA	
Average power supply current* (Static column mode)	I_{CC9}	$\overline{RAS}$=V_{IL}, $\overline{CS}$ cycling t_{SC}=min	−	55	−	55	−	70	−	60	−	55	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A9, D_{IN})	C_{IN1}	−	−	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WE}$)	C_{IN2}	−	−	7	pF
Output capacitance (D_{OUT})	C_{OUT}	−	−	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSM 511002A-8A		MSM 511002A-1A		MSM 511002A-70		MSM 511002A-80		MSM 511002A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REP}	–	8	–	8	–	8	–	8	–	8	m	
Random read or write cycle time	t_{RC}	160	–	190	–	140	–	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	185	–	220	–	165	–	185	–	220	–	ns	
Static column mode cycle time	t_{SC}	55	–	55	–	45	–	50	–	55	–	ns	
Static column mode read/write cycle time	t_{SRWC}	80	–	100	–	70	–	80	–	100	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	70	–	80	–	100	ns	4,5,6
Access time from $\overline{CS}$	t_{CAC}	–	25	–	30	–	20	–	20	–	25	ns	4, 5
Access time from column address	t_{AA}	–	40	–	50	–	35	–	40	–	50	ns	4,6,7
Access time from last write	t_{ALW}	–	75	–	95	–	65	–	75	–	95	ns	4, 7
Output low impedance time from $\overline{CS}$	t_{CLZ}	0	–	0	–	0	–	0	–	0	–	ns	4
Data out put hold time reference to column address	t_{AOH}	5	–	5	–	5	–	5	–	5	–	ns	
Data output enable time reference to $\overline{WE}$	t_{OW}	–	30	–	30	–	30	–	30	–	30	ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	–	80	–	60	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	70	10000	80	10000	100	10000	ns	
$\overline{RAS}$ pulse width (static column mode cycle only)	t_{RASC}	80	100000	100	100000	70	100000	80	100000	100	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25	–	30	–	20	–	20	–	25	–	ns	
$\overline{CS}$ precharge time	t_{CP}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{CS}$ pulse width	t_{CS}	25	10000	30	10000	20	10000	20	10000	25	10000	ns	
$\overline{CS}$ pulse width (Static column mode cycle only)	t_{CSC}	25	100000	30	100000	20	100000	20	100000	25	100000	ns	
$\overline{CS}$ hold time	t_{CSH}	80	–	100	–	70	–	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	55	25	70	22	50	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	17	35	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	10	–	10	–	ns	
Row address set-time	t_{ASR}	0	–	0	–	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	12	–	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	15	–	15	–	20	–	ns	

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM 511002A-8A		MSM 511002A-1A		MSM 511002A-70		MSM 511002A-80		MSM 511002A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	35	–	40	–	50	–	ns	
Column adress hold time reference to $\overline{RAS}$ (WRITE CYCLE)	t_{AWR}	60	–	75	–	55	–	60	–	75	–	ns	
Column address hold time reference to $\overline{RAS}$	t_{AR}	95	–	115	–	85	–	95	–	115	–	ns	
Column address hold time reference to $\overline{RAS}$ precharge	t_{AH}	10	–	10	–	10	–	10	–	10	–	ns	
Column address hold time reference to $\overline{WE}$	t_{AHLW}	75	–	95	–	65	–	75	–	95	–	ns	
Last write to column address delay	t_{LWAD}	20	35	25	45	20	30	20	35	25	45	ns	7
Read command se-up time	t_{RCS}	0	–	0	–	0	–	0	–	0	–	ns	
Read command hold time reference to $\overline{CS}$	t_{RCH}	0	–	0	–	0	–	0	–	0	–	ns	9
Write connand hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	55	–	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	0	–	0	–	0	–	ns	8
Write command pulse width	t_{WP}	15	–	20	–	15	–	15	–	20	–	ns	
Write invalid time	t_{WI}	10	–	10	–	10	–	10	–	10	–	ns	
Write command hole time (Dout disable)	t_{WCH}	15	–	20	–	15	–	15	–	20	–	ns	8
Data-in hold time from$\overline{RAS}$	t_{DHR}	60	–	75	–	55	–	60	–	75	–	ns	
Data output hold time reference to $\overline{WE}$	t_{WOH}	0	–	0	–	0	–	0	–	0	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	20	–	20	–	25	–	ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20	–	25	–	20	–	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	15	–	15	–	20	–	ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	25	–	30	–	20	–	20	–	25	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80	–	100	–	70	–	80	–	100	–	ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	40	–	50	–	35	–	40	–	50	–	ns	8
$\overline{RAS}$ to second $\overline{WE}$ delay	t_{RSWD}	95	–	115	–	80	–	95	–	115	–	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	10	–	ns	9
$\overline{RAS}$ to $\overline{CS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	10	–	10	–	ns	

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM 511002A-8A		MSM 511002A-1A		MSM 511002A-70		MSM 511002A-80		MSM 511002A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$\overline{RAS}$ to $\overline{CS}$ hold time ($\overline{CS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	30	–	30	–	30	–	ns	
$\overline{CS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{CS}$ precharge time (Refrech counter test)	t_{CPT}	40	–	50	–	40	–	40	–	50	–	ns	
$\overline{CS}$ precharge time	t_{CPN}	10	–	15	–	10	–	10	–	15	–	ns	

4

Notes: **1** An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.

2 The AC characteristics assume at $t_T = 5$ ns.

3 V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4 Measured with a load circuit equivalent to 2TTL + 100 pF.

5 Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

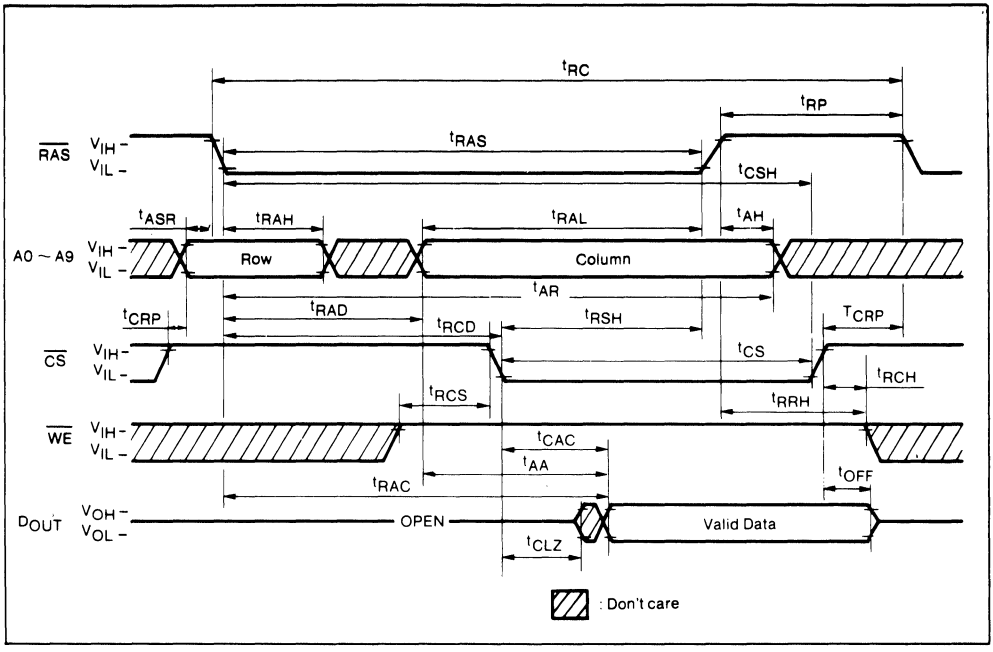
6 Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

7 Operation within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met. t_{LWAD} (max.) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

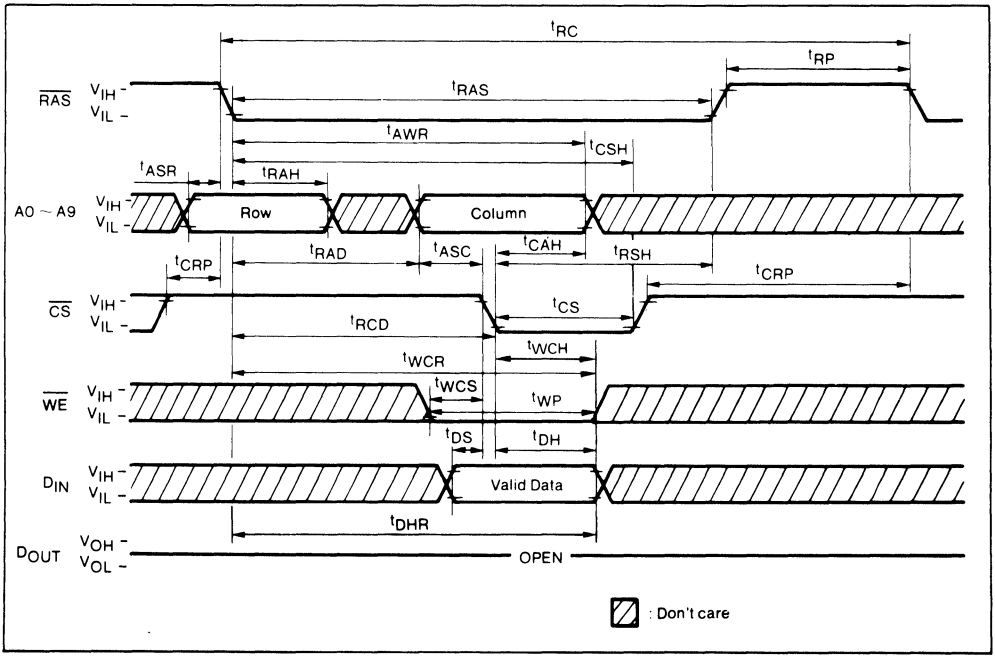
8 t_{WCS}, t_{WH}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) and $t_{WH} \geqq t_{WH}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

9 Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

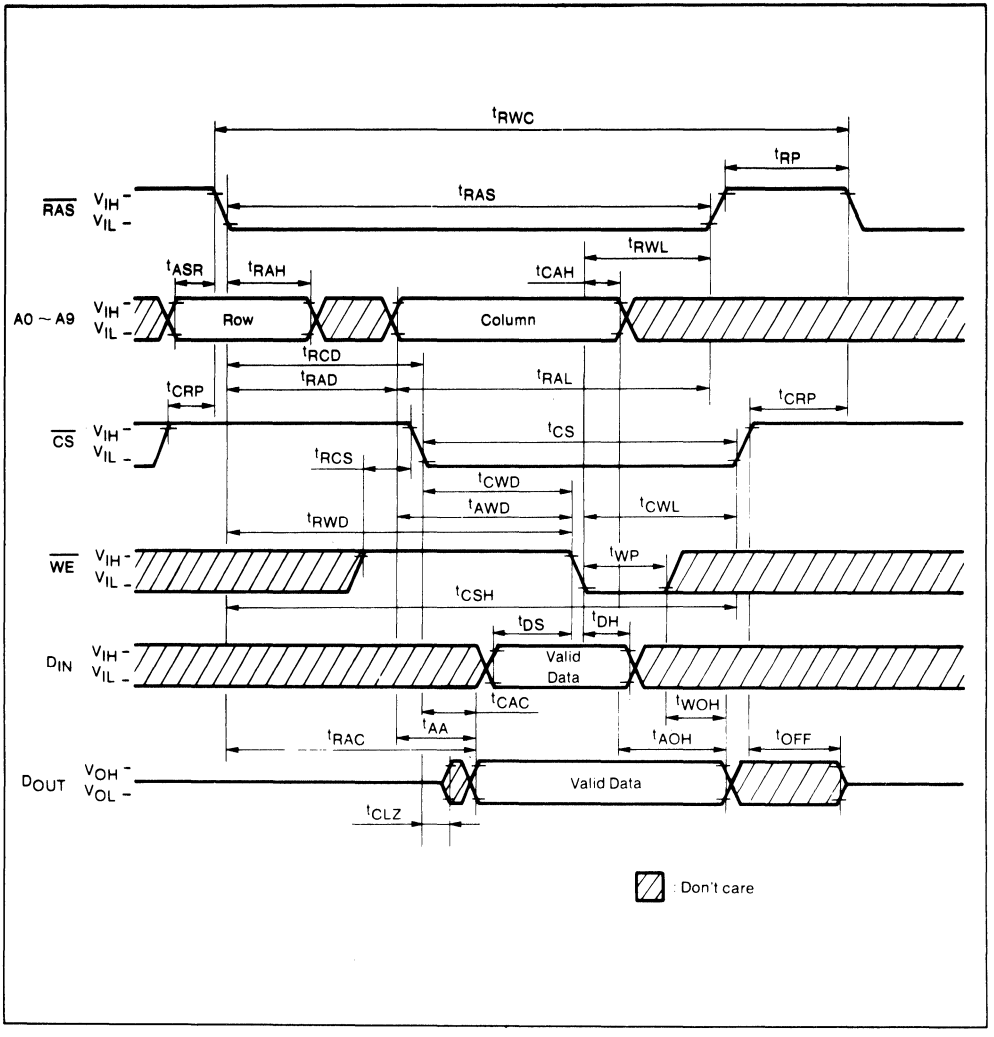
READ CYCLE



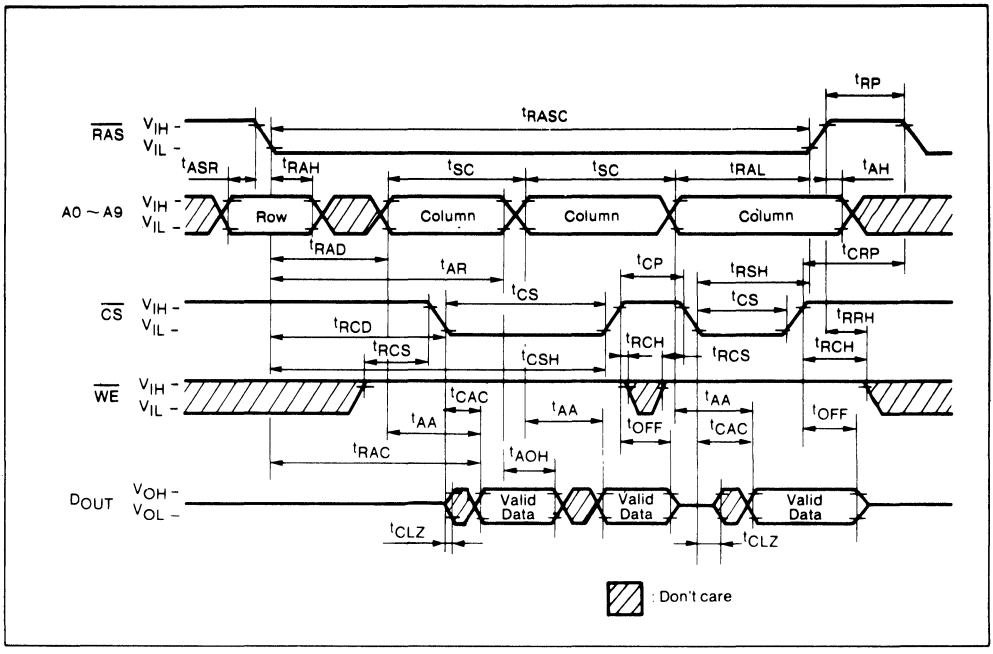
WRITE CYCLE (EARLY WRITE)



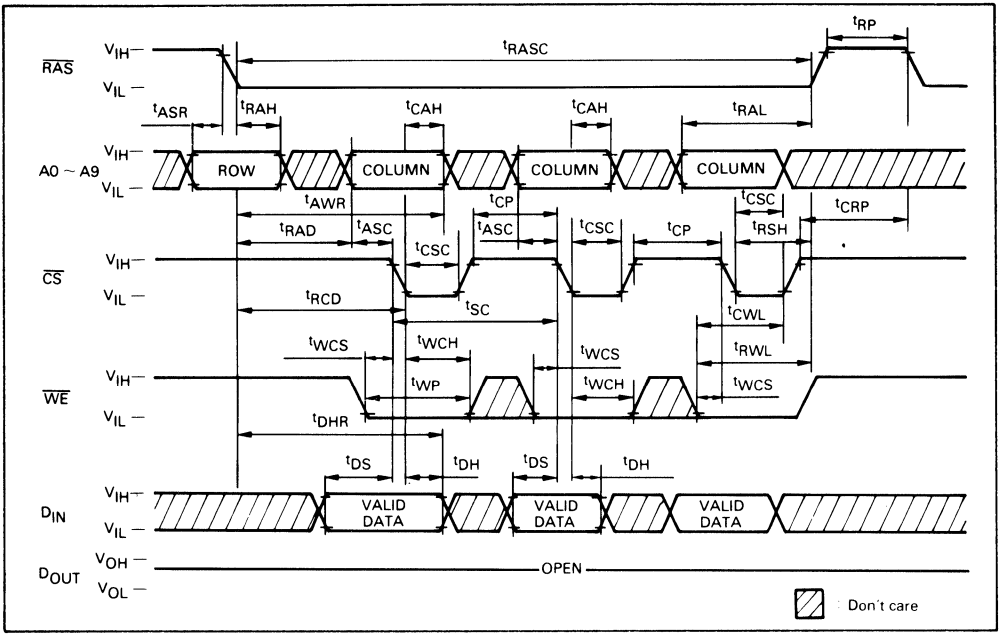
READ/WRITE CYCLE



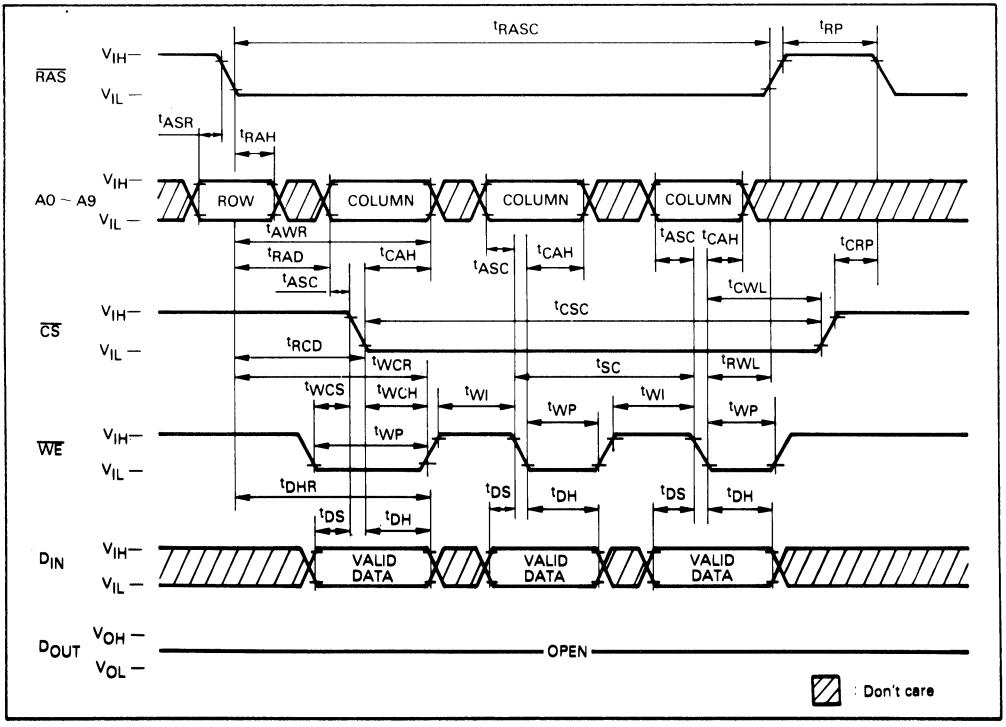
STATIC COLUMN MODE READ CYCLE



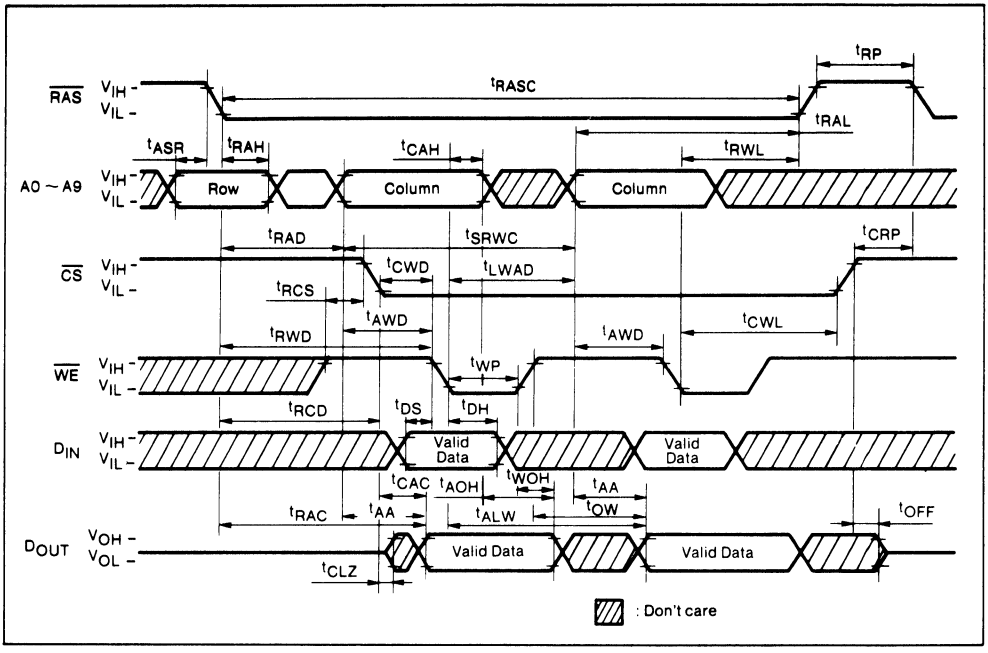
● STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



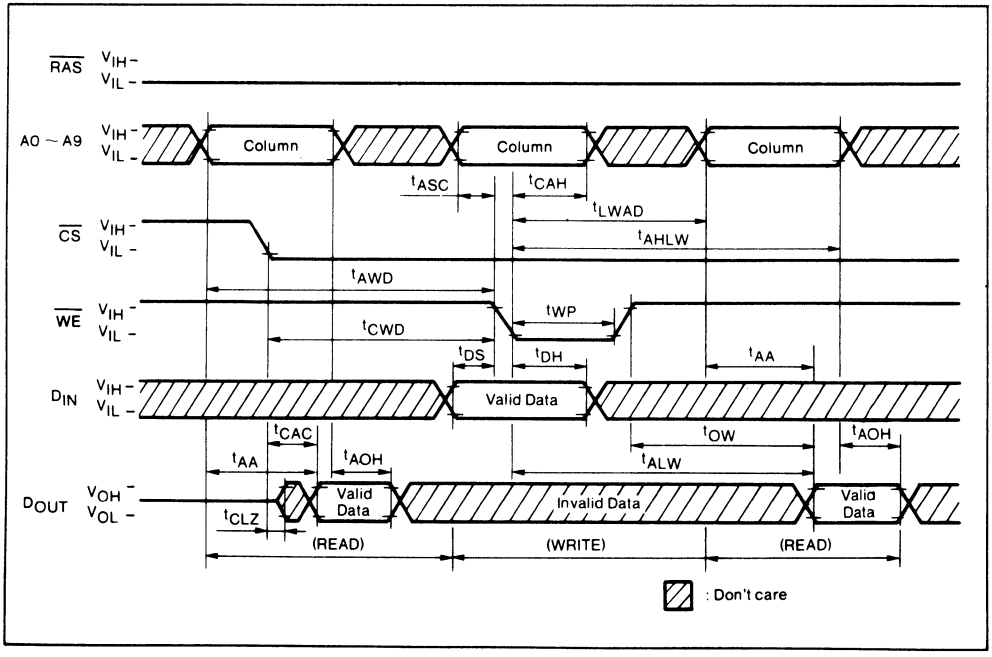
● STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



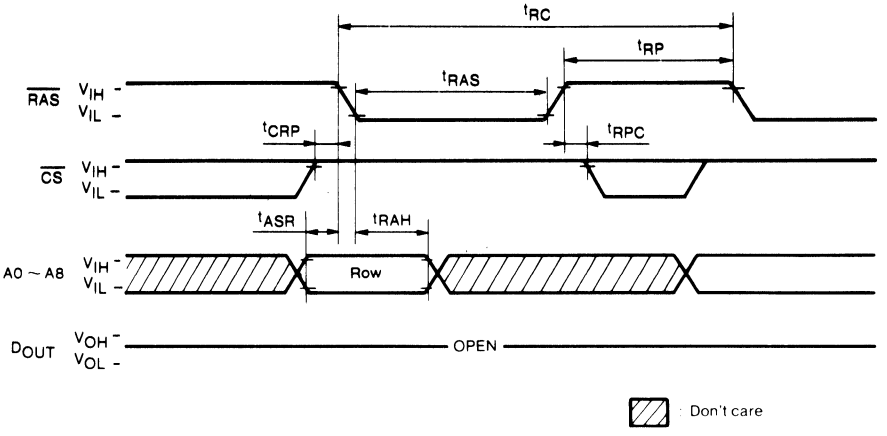
STATIC COLUMN MODE READ/WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE

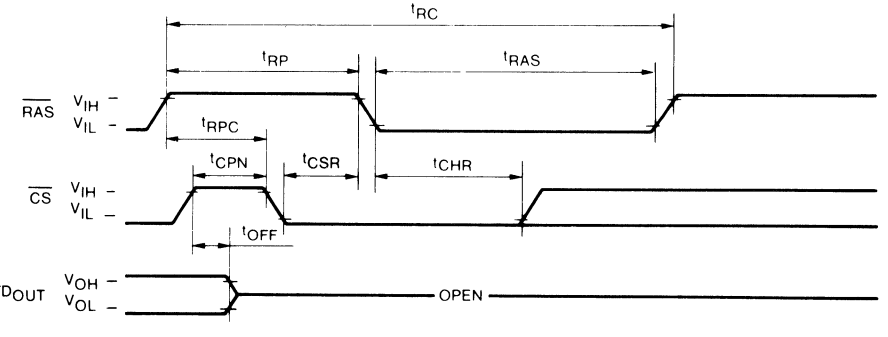


$\overline{RAS}$ ONLY REFRESH CYCLE



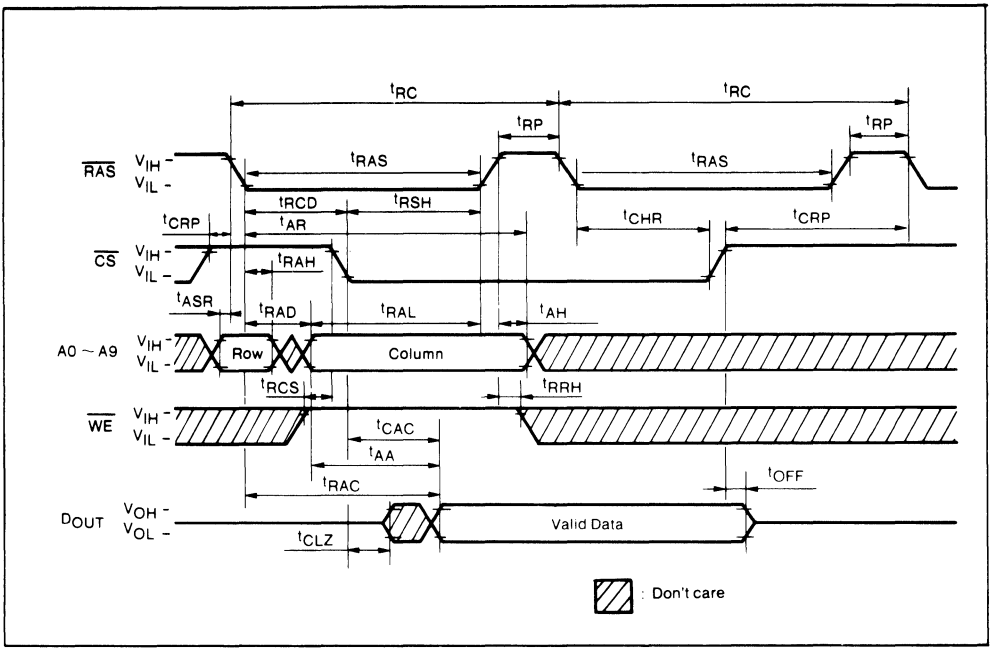
NOTE: $\overline{WE}$ = Don't care, A9 = Don't care

$\overline{CS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE

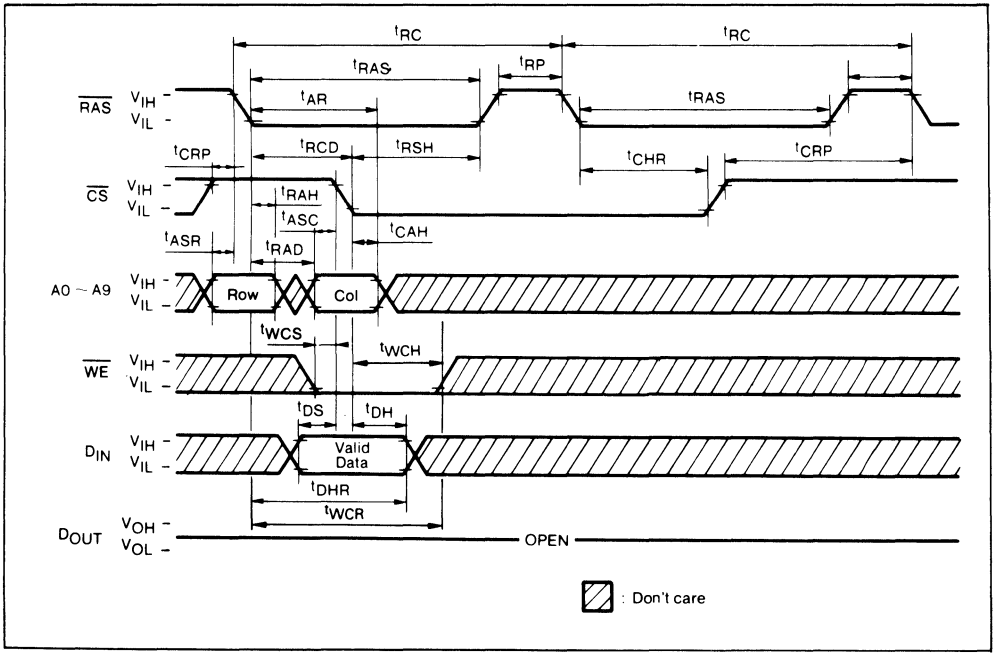


NOTE: $\overline{WE}$ = Don't care, A0 ~ A9 = Don't care

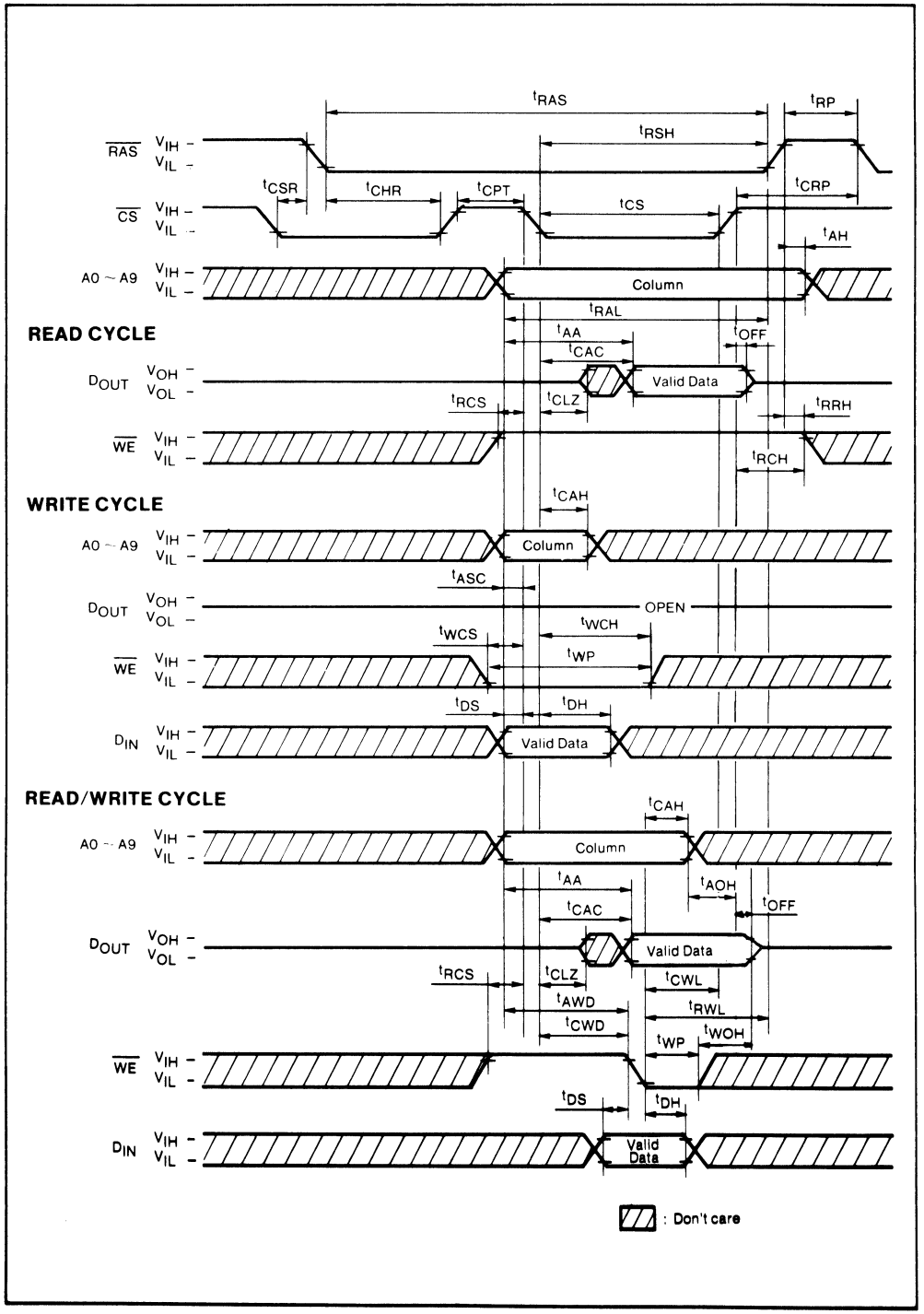
HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST



MSM514256A

262,144-WORD × 4-BITS DYNAMIC RAM

GENERAL DESCRIPTION

The MSM514256A is a new generation dynamic RAM organized as 262,144 words by 4 bits. The technology used to fabricate the MSM514256A is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

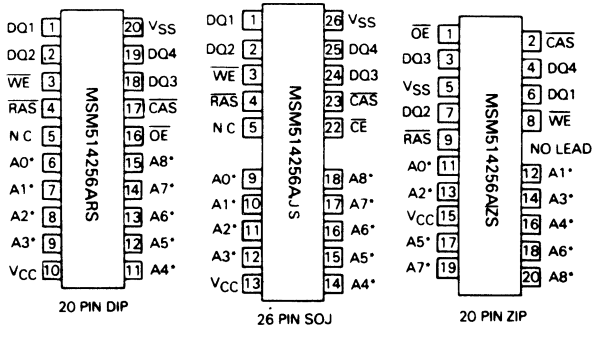
FEATURES

- Silicon gate, tripple polysilicon CMOS, 1-transistor memory cell
- Family organization
- 262,144 words by 4 bits

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM514256A-70	70ns	140ns	468mW	5.5mW
MSM514256A-8A/80	80ns	160ns	413mW	
MSM514256A-1A/10	100ns	190ns	358mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Output impedance controllable through early write and $\overline{OE}$ operations
- Fast page mode, read/write capability
- $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$ only refresh capability
- "Gated" $\overline{CAS}$
- Built-in V_{BB} generator circuit

PIN CONFIGURATION (TOP VIEW)

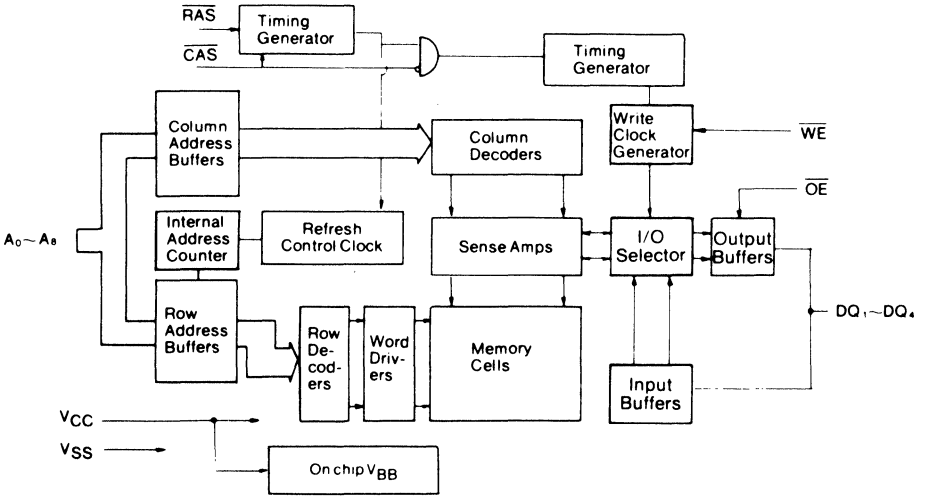


* Refresh Address

Pin Names	Function
A0 to A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1 to DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
NC	No Connection

4

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions		MSM514256 A-8A		MSM514256 A-1A		MSM514256 A-70		MSM514256 A-80		MSM514256 A-10		Unit	Noto
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0mA		2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2mA		0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0V ≦ VI ≦ 6.5V; all oter pins not under test = 0V		−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable 0V ≦ VO ≦ 5.5V		−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, T_{RC} = min		−	75	−	65	−	85	−	75	−	65	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = Hz	TTL	−	2	−	2	−	2	−	2	−	2	mA	
			MOS	−	1	−	1	−	1	−	1	−	1		
Average power supply current* ($\overline{RAS}$ only represh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min		−	75	−	65	−	85	−	75	−	65	mA	
Average power supply current* ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$		−	75	−	65	−	85	−	75	−	65	mA	
Average power supply current* (Fast page mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min		−	60	−	60	−	75	−	65	−	60	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A8)	C_{IN1}	−	−	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	−	−	7	pF
Output capacitance (DQ1 to DQ4)	$C_{I/O}$	−	−	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSM514256 A-8A		MSM514256 A-1A		MSM514256 A-70		MSM514256 A-80		MSM514256 A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REP}	–	8	–	8	–	8	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	160	–	190	–	140	–	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	215	–	255	–	195	–	215	–	255	–	ns	
Fast page mode cycle time	t_{PC}	55	–	55	–	45	–	50	–	55	–	ns	
Fast page mode read/write cycle time	t_{PRWC}	110	–	120	–	100	–	105	–	120	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	70	–	80	–	100	ns	4.5
Access time from $\overline{CAS}$	t_{CAC}	–	25	–	30	–	20	–	20	–	25	ns	4.5
Access time fro columu address	t_{AA}	–	40	–	50	–	35	–	40	–	50	ns	4.6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	50	–	50	–	40	–	45	–	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	0	–	0	–	0	–	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ prechrge time	t_{RP}	70	–	80	–	60	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	70	10000	80	10000	100	10000	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100000	100	100000	70	100000	80	100000	100	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25	–	30	–	20	–	20	–	25	–	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	30	10000	20	10000	20	10000	25	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	100	–	70	–	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	55	25	70	22	50	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	17	35	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	12	–	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	15	–	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	75	–	55	–	60	–	75	–	ns	

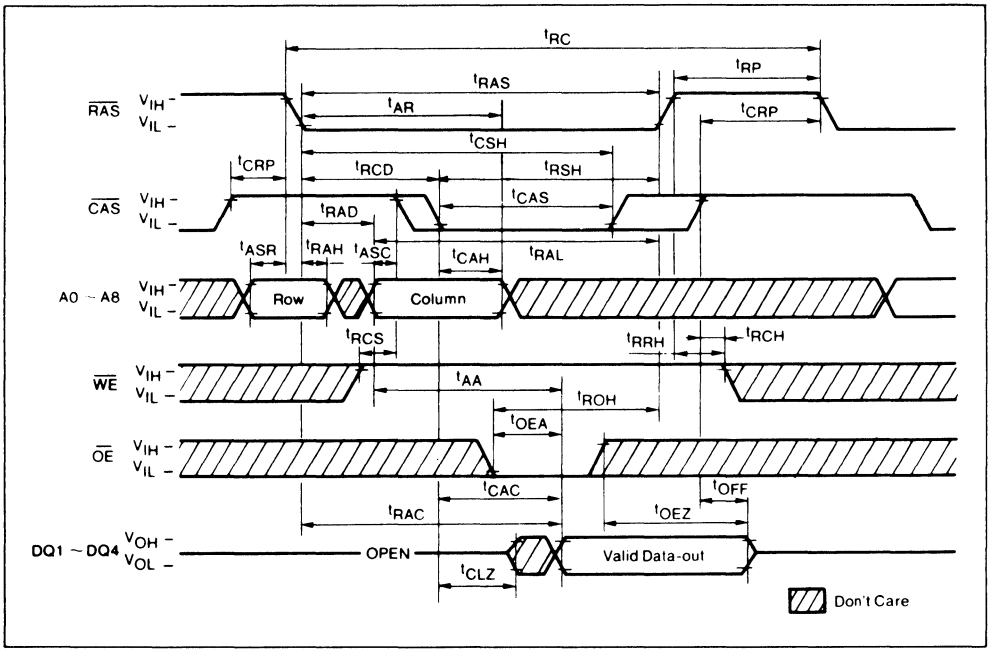
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM514256 A-8A		MSM514256 A-1A		MSM514256 A-70		MSM514256 A-80		MSM514256 A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Column address to $\overline{RAS}$ qead time	t_{RAL}	40	–	50	–	35	–	40	–	50	–	ns	
Read command set-up time	t_{RCS}	0	–	0	–	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	0	–	0	–	ns	8
Write connand hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	55	–	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	0	–	0	–	0	–	ns	7
Write command hold time	t_{WCH}	15	–	20	–	15	–	15	–	20	–	ns	
Write command pulse width	t_{WP}	15	–	20	–	15	–	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	20	–	20	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	25	–	20	–	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	15	–	15	–	20	–	ns	
Data-ds hold time from $\overline{RAS}$	t_{DHR}	60	–	75	–	55	–	60	–	75	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	55	–	65	–	50	–	50	–	60	–	ns	7
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	110	–	135	–	100	–	110	–	135	–	ns	7
Column address to $\overline{WE}$ delay time	t_{AWD}	70	–	85	–	65	–	70	–	85	–	ns	7
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	10	–	ns	8
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time (CAS before $\overline{RAS}$)	t_{CHR}	30	–	30	–	30	–	30	–	30	–	ns	
$\overline{CAS}$ active delay fron $\overline{RAS}$ preharge	t_{RPC}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	50	–	40	–	40	–	50	–	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	–	15	–	10	–	10	–	15	–	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	20	–	20	–	20	–	20	–	20	–	ns	
Access time from $\overline{OE}$	t_{OEA}	–	20	–	25	–	20	–	20	–	25	ns	
$\overline{OE}$ delay time	t_{ODE}	20	–	25	–	20	–	20	–	25	–	ns	
$\overline{OE}$ to data output guffer turn-off delay	t_{OEZ}	0	20	0	25	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20	–	25	–	20	–	20	–	25	–	ns	

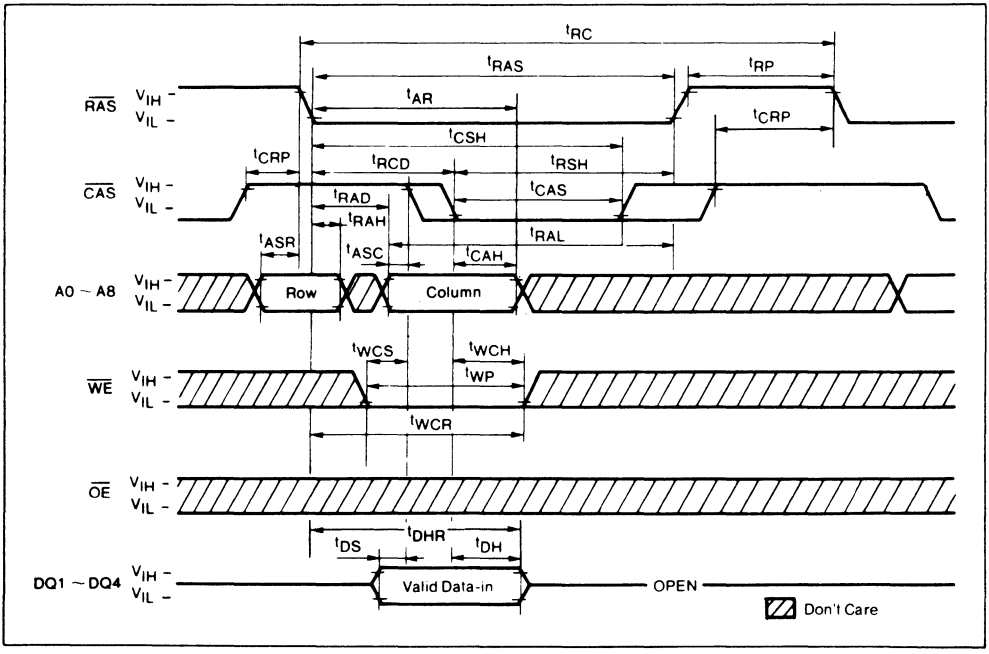
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusiveiy by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

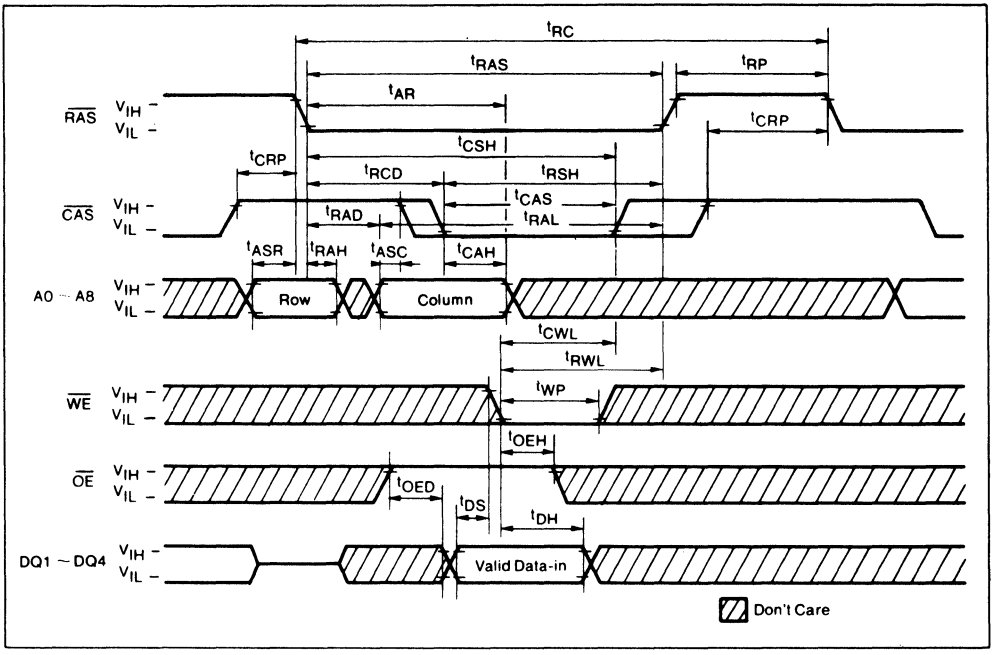
READ CYCLE



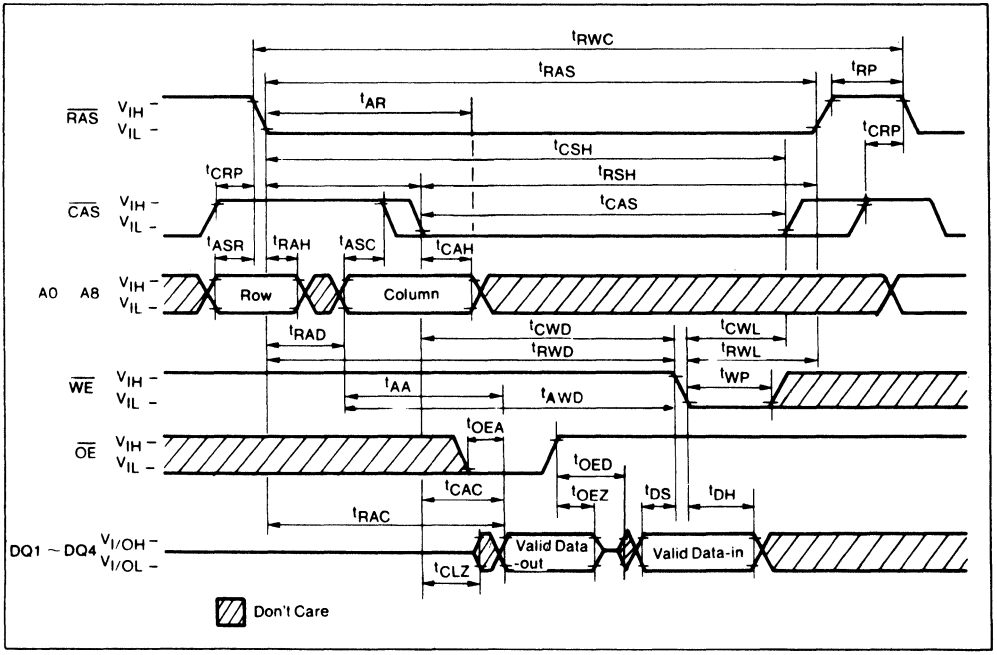
WRITE CYCLE (EARLY WRITE)



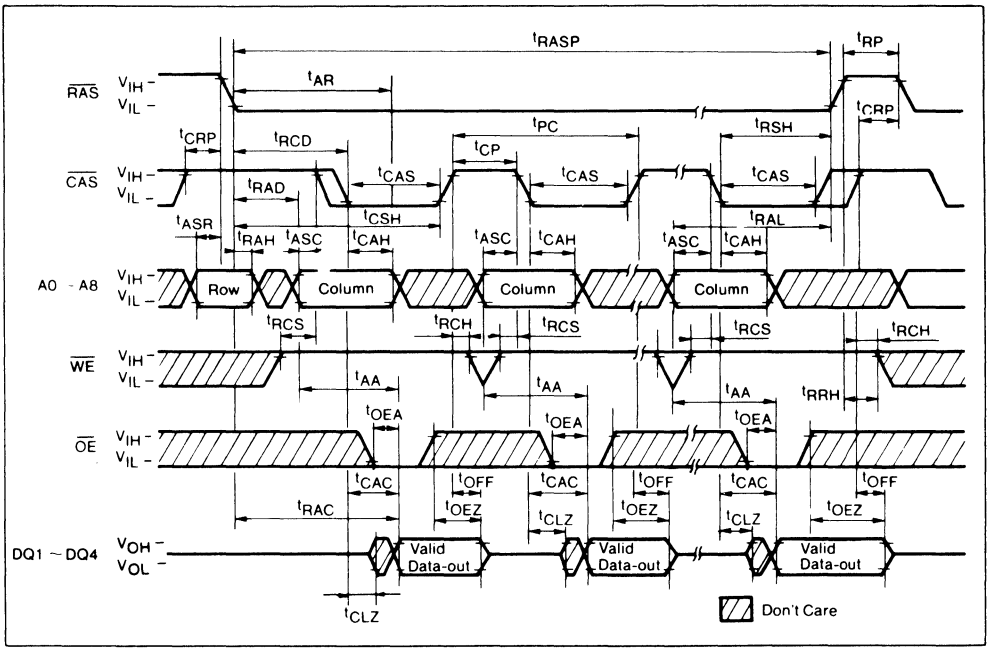
WRITE CYCLE ($\overline{OE}$ CONTROL WRITE)



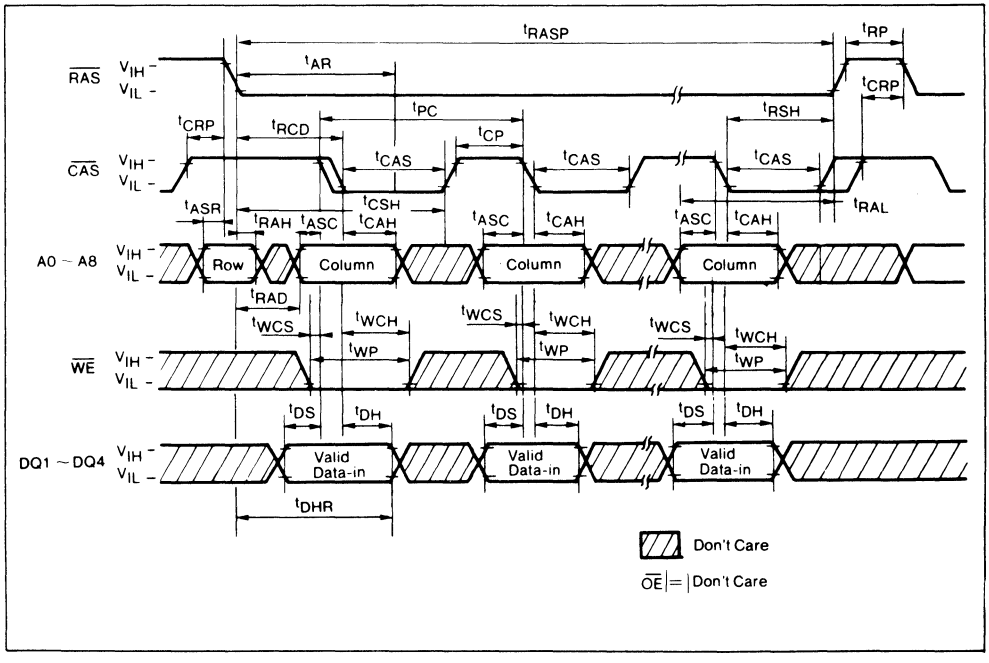
READ/WRITE CYCLE



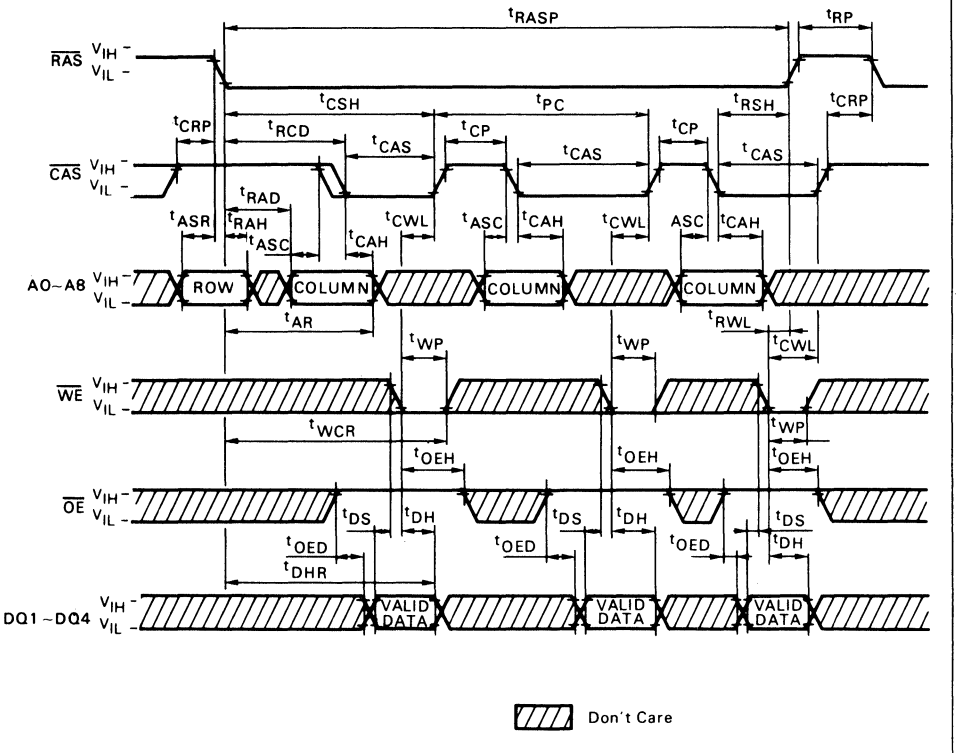
FAST PAGE MODE READ CYCLE



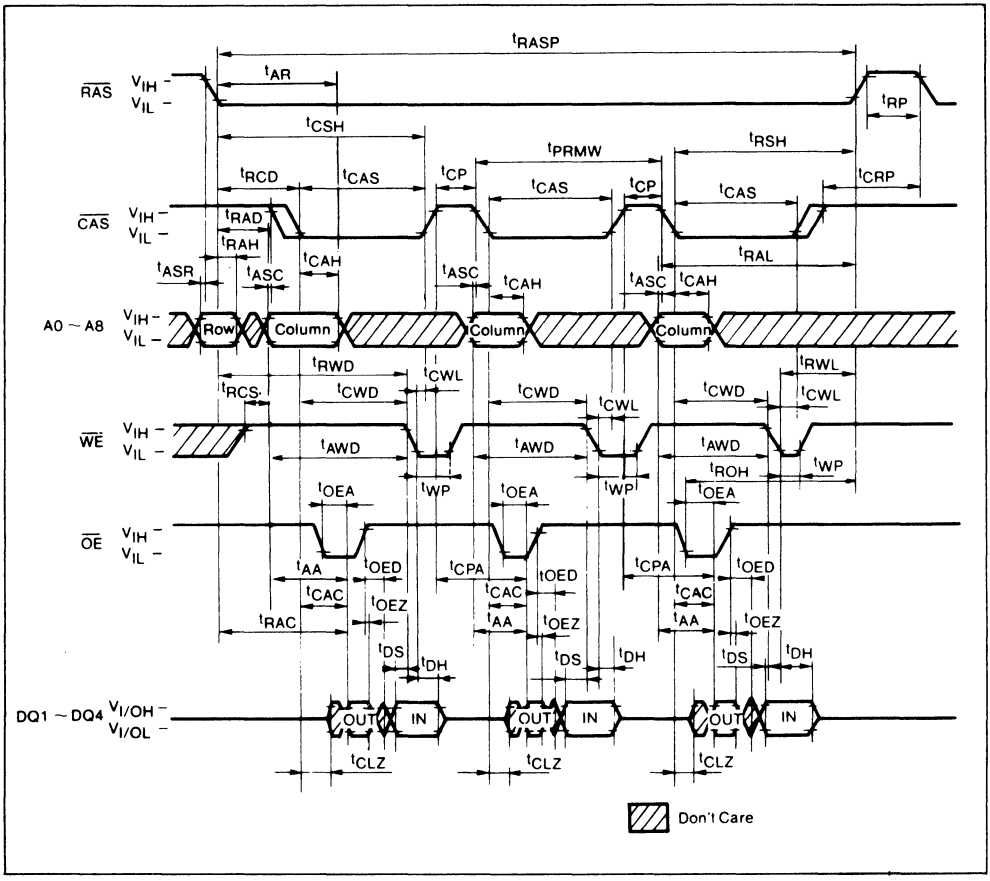
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



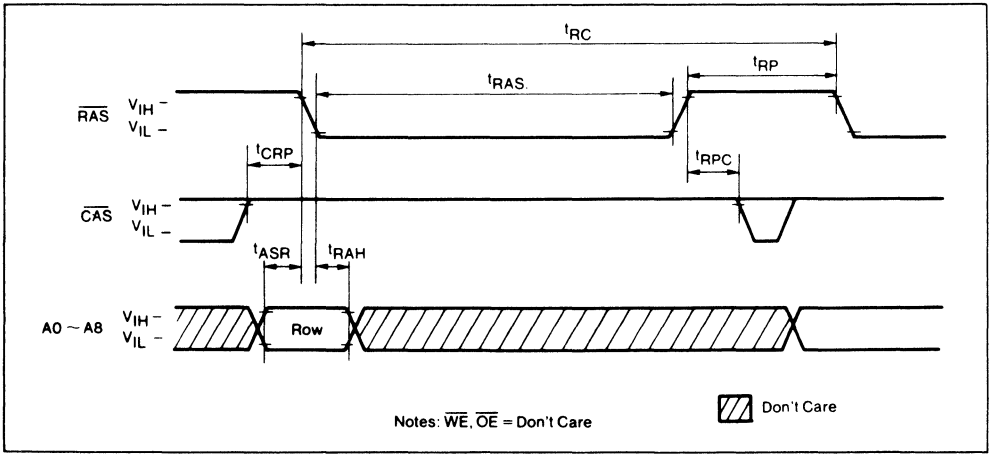
FAST PAGE MODE WRITE CYCLE($\overline{OE}$ CONTROL WRITE)



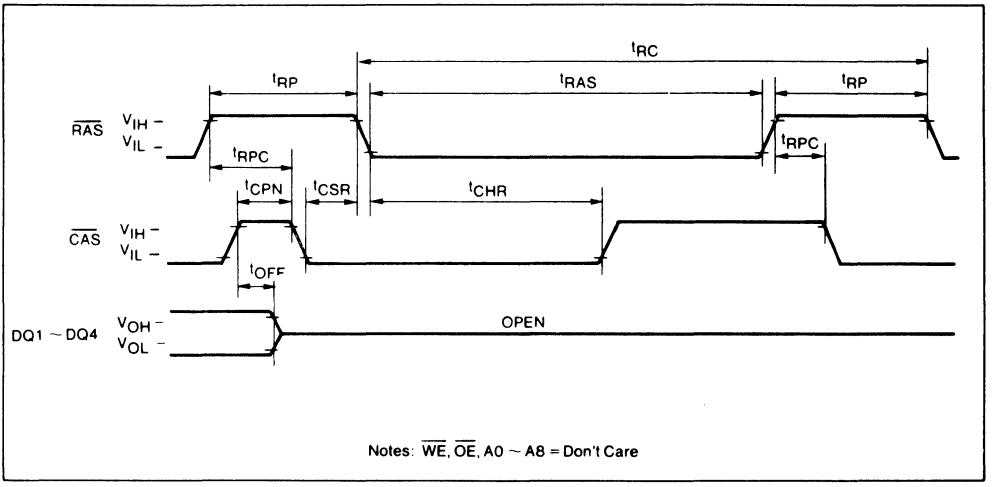
FAST PAGE MODE READ/WRITE CYCLE



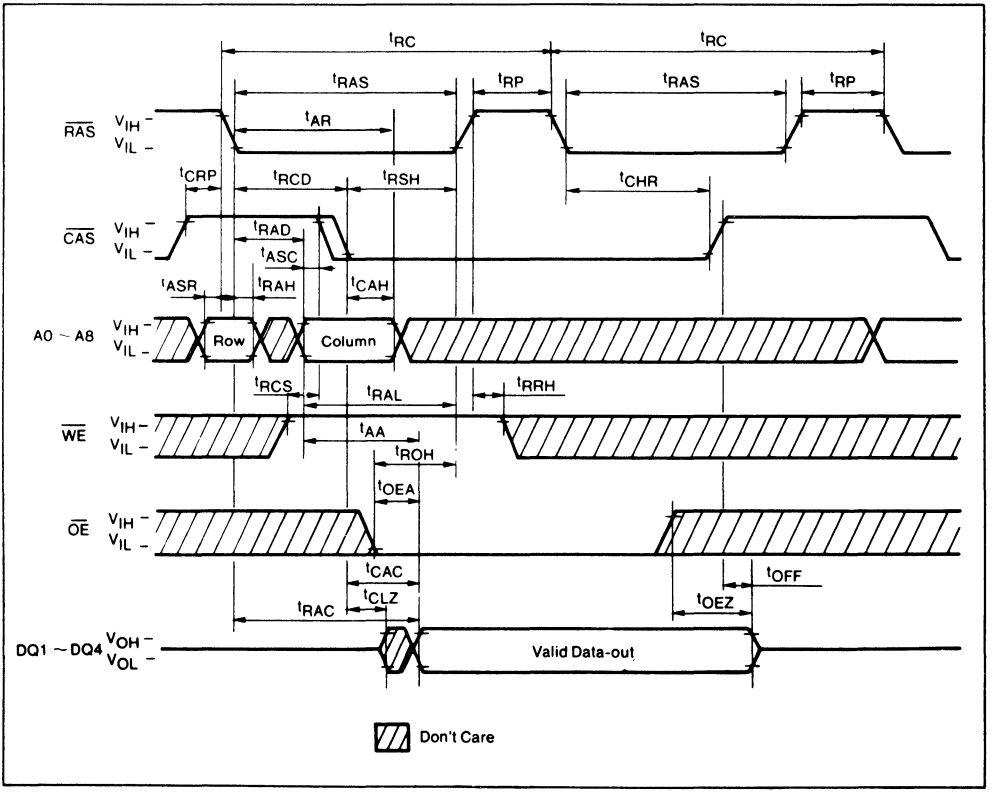
RAS ONLY REFRESH CYCLE



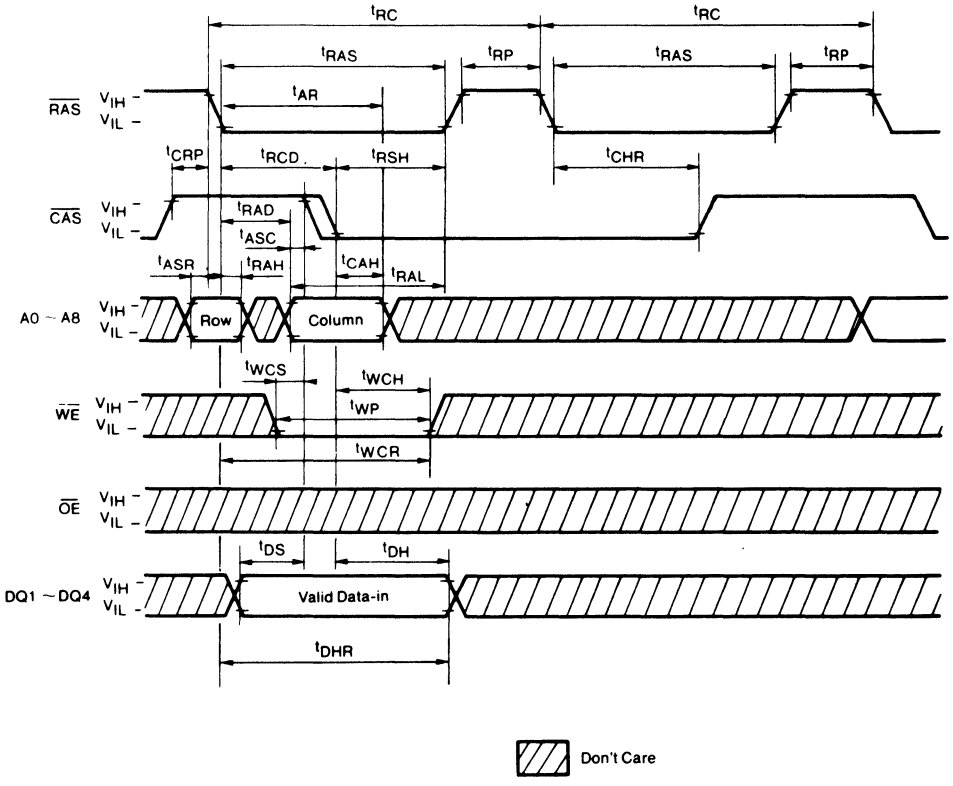
$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



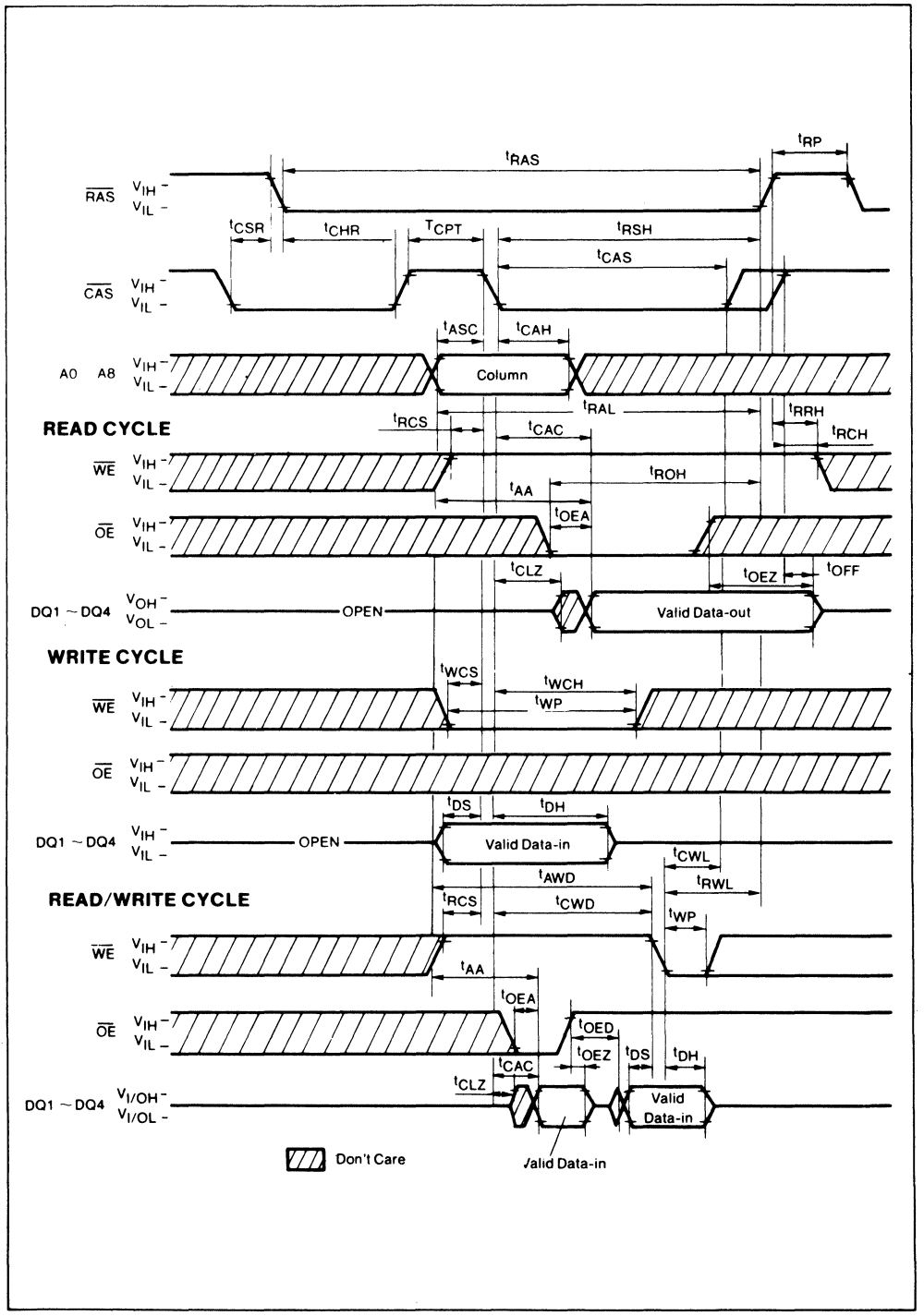
HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



CAS BEFORE RAS REFRESH COUNTER TEST



OKI semiconductor

MSM514258A

262,144-WORD × 4-BITS DYNAMIC RAM

GENERAL DESCRIPTION

The MSM514258A is a new generation dynamic RAM organized as 262,144 words by 4 bit. The technology used to fabricate the MSM514258A is OKI's CMOS silicon gate process technology. The device operates at a single +5V power supply. Its I/O pins are TTL compatible.

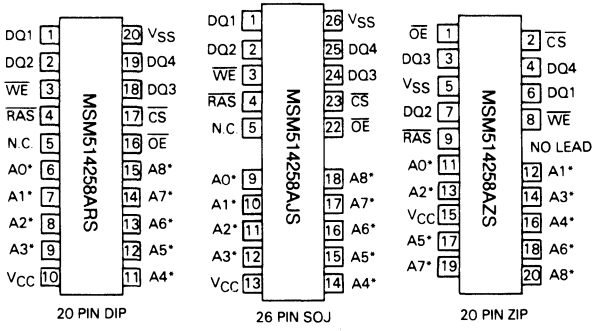
FEATURES

- Silicon gate, tripple polysilicon CMOS, 1-transistor memory cell
- Family organization
- 262,144 words by 4 bits

Family	Access Time (MAX)	Cycle Time (MIN)	Power Dissipation	
			Operating (MAX)	Standby (MAX)
MSM514258A-70	70ns	140ns	468mW	5.5mW
MSM514258A-8A/80	80ns	160ns	413mW	
MSM514258A-1A/10	100ns	190ns	358mW	

- Single +5V supply, ±10% tolerance
- Input: TTL compatible, address input, data input latch
- Output: TTL compatible, tristate, nonlatch
- Refresh: 512 cycles/8 ms
- Output impedance controllable through early write and $\overline{OE}$ operations
- Static column mode, read/write capability capability
- $\overline{CS}$ before $\overline{RAS}$ refresh, Hidden refresh, $\overline{RAS}$ only refresh capability
- Built-in V_{BB} generator circuit

PIN CONFIGURATION (TOP VIEW)

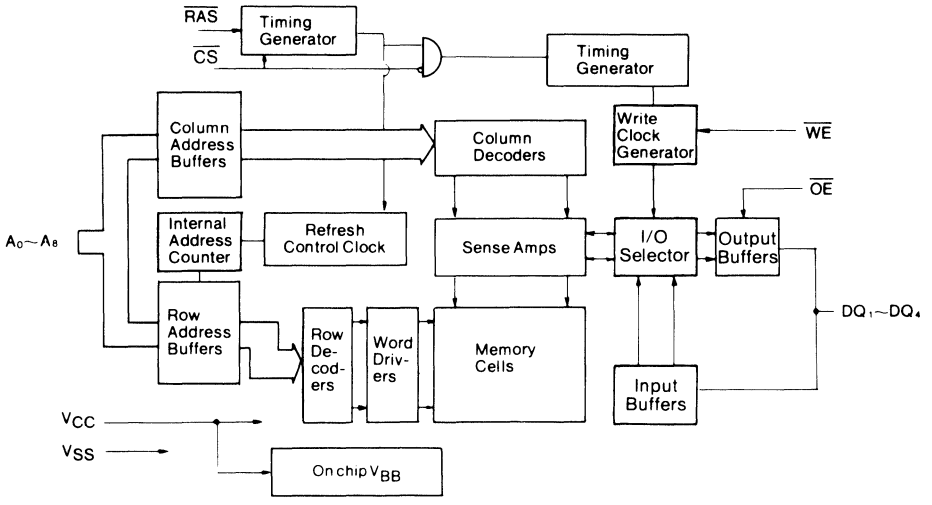


* Refresh Address

Pin Names	Function
A0 to A8	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip select input
DQ1 to DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply (+5V)
V_{SS}	Ground (0V)
N.C.	No Connection

4

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit
Voltage on any pin relative to V_{SS}	VT	Ta = 25°C	−1.0 to +7.0	V
Short circuit output current	Ios	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	Topr	–	0 to +70	°C
Storage temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to +70°)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
	V_{SS}	–	0	0	0	V
Input high voltage	V_{IH}	–	2.4	–	6.5	V
Input low voltage	V_{IL}	–	−1.0	–	0.8	V

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 514258A-8A		MSM 514258A-1A		MSM 514258A-70		MSM 514258A-80		MSM 514258A-10		Unit	Noto
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2mA	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	OV≦VI≦6.5V; all oter pins not under test = OV	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} disable OV≦VO≦5.5V	−10	10	−10	10	−10	10	−10	10	−10	10	μA	
Average power supply current* (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ cycling, t_{RC} = min	–	75	–	65	–	85	–	75	–	65	mA	
Power supply current* (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IH}, D_{OUT} = Hz — TTL	–	2	–	2	–	2	–	2	–	2	mA	
		$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IH}, D_{OUT} = Hz — MOS	–	1	–	1	–	1	–	1	–	1		
Average power supply current* ($\overline{RAS}$ only represh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min	–	75	–	65	–	85	–	75	–	65	mA	
Average power supply current* ($\overline{CS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CS}$ before $\overline{RAS}$	–	75	–	65	–	85	–	75	–	65	mA	
Average power supply current* (Static column mode)	I_{CC9}	$\overline{RAS}$ = V_{IL}, $\overline{CS}$ cycling, t_{SC} = min	–	60	–	60	–	75	–	65	–	60	mA	

***Note:** I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A8)	C_{IN1}	–	–	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	–	–	7	pF
Output capacitance (DQ1 to DQ4)	$C_{I/O}$	–	–	7	pF

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSM 514258A-8A		MSM 514258A-1A		MSM 514258A-70		MSM 514258A-80		MSM 514258A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REP}	–	8	–	8	–	8	–	8	–	8	ms	
Random read or write cycle time	t_{RC}	160	–	190	–	140	–	160	–	190	–	ns	
Read or write cycle time	t_{RWC}	215	–	255	–	195	–	215	–	255	–	ns	
Static column mode cycle time	t_{SC}	55	–	55	–	45	–	50	–	55	–	ns	
Static column mode read/write cycle time	t_{SRWC}	110	–	135	–	100	–	110	–	135	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	100	–	70	–	80	–	100	ns	4,5,6
Access time from $\overline{CS}$	t_{CAC}	–	25	–	30	–	20	–	20	–	25	ns	4, 5
Access time from column address	t_{AA}	–	40	–	50	–	35	–	40	–	50	ns	4,6,7
Access time from last write	t_{ALW}	–	75	–	95	–	65	–	75	–	95	ns	4, 7
Output low impedance time from $\overline{CS}$	t_{CLZ}	0	–	0	–	0	–	0	–	0	–	ns	4
Data output hold time reference to column address	t_{AOH}	5	–	5	–	5	–	5	–	5	–	ns	
Data output enable time reference to $\overline{WE}$	t_{OW}	–	30	–	30	–	30	–	30	–	30	ns	
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ prechrge time	t_{RP}	70	–	80	–	60	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	70	10000	80	10000	100	10000	ns	
$\overline{RAS}$pulse width (Static column mode cycle only)	t_{RASC}	80	100000	100	100000	70	100000	80	100000	100	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25	–	30	–	20	–	20	–	25	–	ns	
$\overline{CS}$ precharge time (static column mode)	t_{CP}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{CS}$ pulse width	t_{CS}	25	10000	30	10000	20	10000	20	10000	25	10000	ns	
$\overline{CS}$ pulse width (Static column mode cycle only)	t_{CSC}	25	100000	30	100000	20	100000	20	100000	25	100000	ns	
$\overline{CS}$ hold time	t_{CSH}	80	–	100	–	70	–	80	–	100	–	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	25	55	25	70	22	50	22	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	17	35	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	10	–	10	–	ns	
Row address set-up time	t_{ASR}	0	–	0	–	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	15	–	15	–	12	–	12	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	20	–	15	–	15	–	20	–	ns	

AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM 514258A-8A		MSM 514258A-1A		MSM 514258A-70		MSM 514258A-80		MSM 514258A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	50	–	35	–	40	–	50	–	ns	
Column adress hold time reference to $\overline{RAS}$ (WRITE CYCLE)	t_{AWR}	60	–	75	–	55	–	60	–	75	–	ns	
Column address hold time reference to $\overline{RAS}$	t_{AR}	95	–	115	–	85	–	95	–	115	–	ns	
Column address hold time reference to $\overline{RAS}$ precharge	t_{AH}	10	–	10	–	10	–	10	–	10	–	ns	
Column address hold time reference to $\overline{WE}$	t_{AHLW}	75	–	95	–	65	–	75	–	95	–	ns	
Last write to column address delay	t_{LWAD}	20	35	25	45	20	30	20	35	25	45	ns	7
Read command se-up time	t_{RCS}	0	–	0	–	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	0	–	0	–	ns	9
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	75	–	55	–	60	–	75	–	ns	
Write command set-up time	t_{WCS}	0	–	0	–	0	–	0	–	0	–	ns	8
Write command pulse width	t_{WP}	15	–	20	–	15	–	15	–	20	–	ns	
Write invalid time	t_{WI}	10	–	10	–	10	–	10	–	10	–	ns	
Write command hole time (Dout disable)	t_{WCH}	15	–	20	–	15	–	15	–	20	–	ns	8
Data-in hold time from$\overline{RAS}$	t_{DHR}	60	–	75	–	55	–	60	–	75	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	20	–	20	–	25	–	ns	
Write command to $\overline{CS}$ lead time	t_{CWL}	20	–	25	–	20	–	20	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	20	–	15	–	15	–	20	–	ns	
$\overline{CS}$ to $\overline{WE}$ delay	t_{CWD}	55	–	65	–	50	–	50	–	60	–	ns	8
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	110	–	135	–	100	–	110	–	135	–	ns	8
Column address to $\overline{WE}$ delay time	t_{AWD}	70	–	85	–	65	–	70	–	85	–	ns	8
$\overline{RAS}$ to second $\overline{WE}$ delay	t_{RSWD}	95	–	115	–	80	–	95	–	115	–	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	10	–	10	–	ns	9
$\overline{RAS}$ to $\overline{CS}$ set-up time ($\overline{CS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CS}$ hold time ($\overline{CS}$ before $\overline{RAS}$)	t_{CHR}	30	–	30	–	30	–	30	–	30	–	ns	
$\overline{CS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	10	–	10	–	ns	

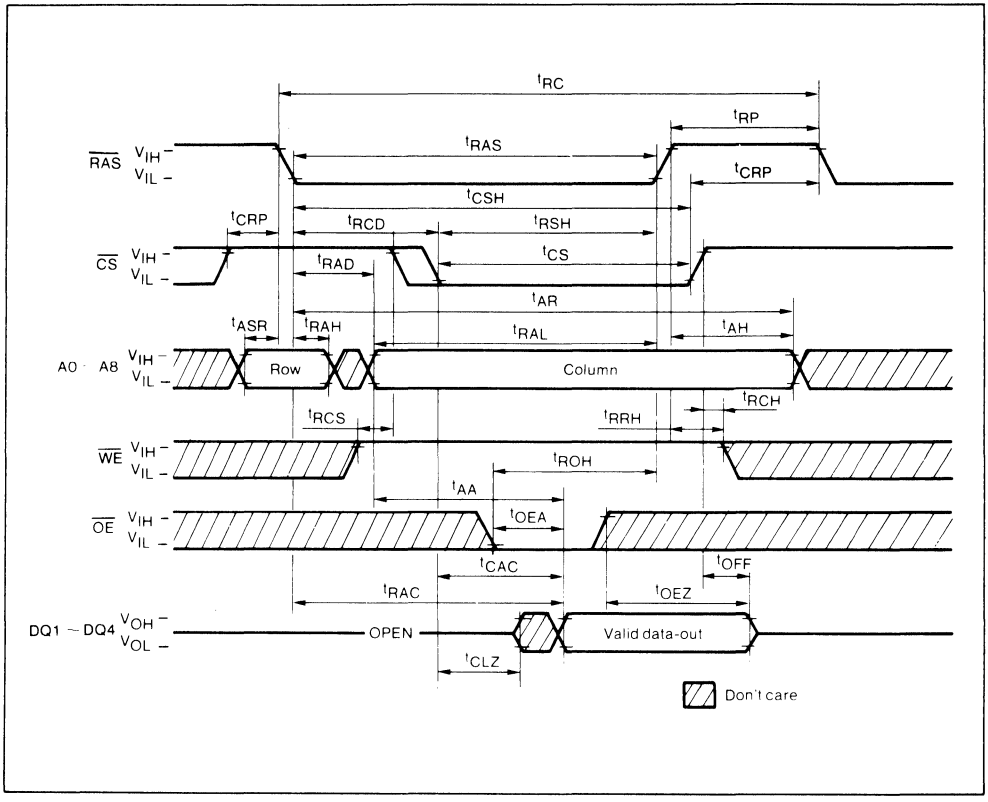
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSM 514258A-8A		MSM 514258A-1A		MSM 514258A-70		MSM 514258A-80		MSM 514258A-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$\overline{CS}$ precharge time (Refrech counter test)	t_{CPT}	40	–	50	–	40	–	40	–	50	–	ns	
$\overline{CS}$ precharge time	t_{CPN}	10	–	15	–	10	–	10	–	15	–	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	20	–	20	–	20	–	20	–	20	–	ns	
Access time from $\overline{OE}$	t_{OEA}	–	25	–	30	–	20	–	20	–	25	ns	
$\overline{OE}$ delay time	t_{OED}	20	–	25	–	20	–	20	–	25	–	ns	
$\overline{OE}$ to data outkut buffer turn-off delay	t_{OEZ}	0	20	0	25	0	20	0	20	0	25	ns	
$\overline{OE}$ command hold time	t_{OEH}	20	–	25	–	20	–	20	–	25	–	ns	

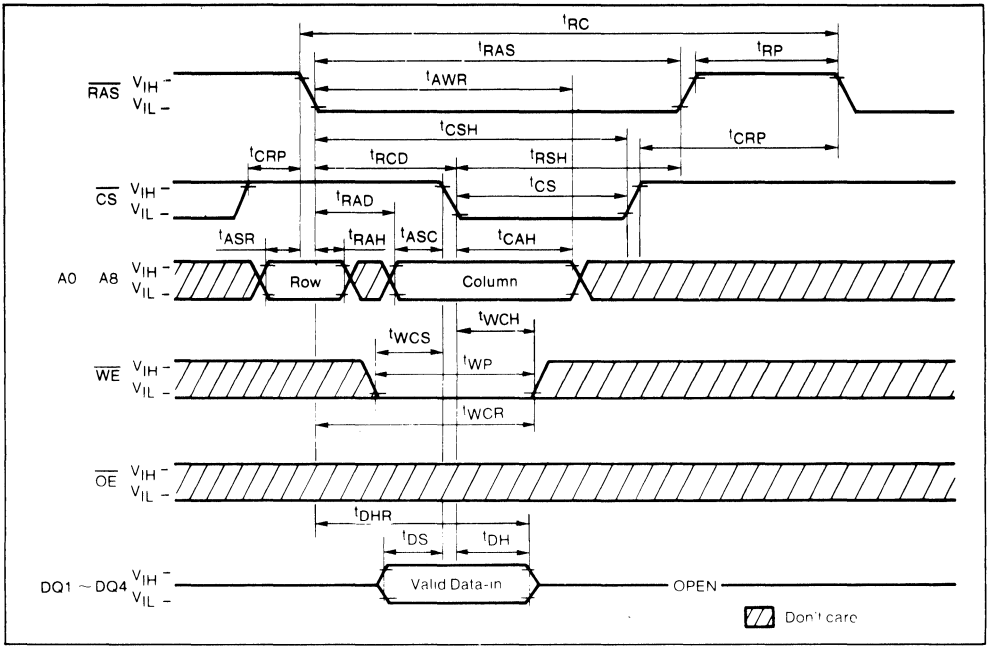
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Operation within the t_{LWAD} (max.), limit insures that t_{ALW} (max.) can be met. t_{LWAD} (max.) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max.) limit, then access time is controlled exclusively t_{AA}.
8. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not a restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.) the cycle is read/write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

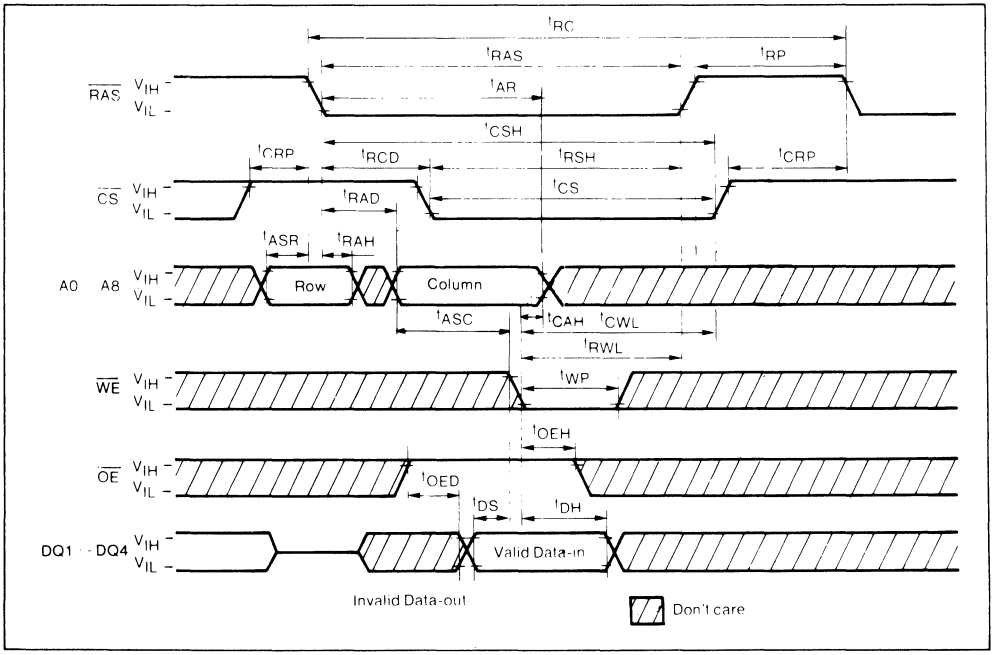
READ CYCLE


tRC
tRP
RAS VIH
VIL
tRAS
tCRP
tCSH
tCRP
tRCD
tRSH
CS VIH
VIL
tRAD
tCS
tAR
tASR
tRAH
tRAL
tAH
A0 - A8 VIH
VIL
Row
Column
tRCS
tRRH
tRCH
WE VIH
VIL
tROH
tAA
OE VIH
VIL
tOEA
tCAC
tOFF
tRAC
tOEZ
DQ1 - DQ4 VOH
VOL
OPEN
Valid data-out
tCLZ
Don't care

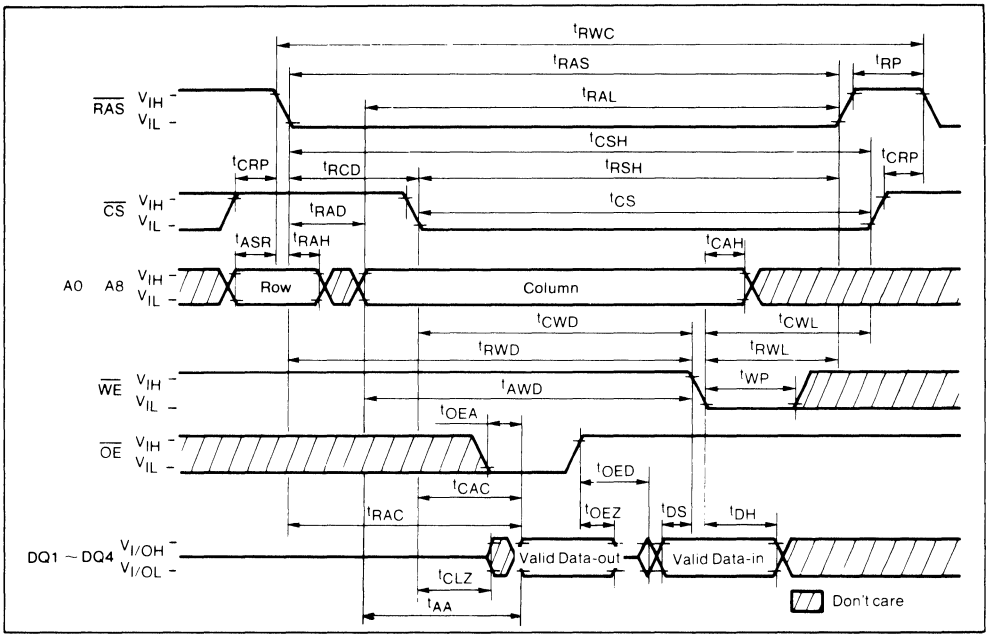
WRITE CYCLE (EARLY WRITE)



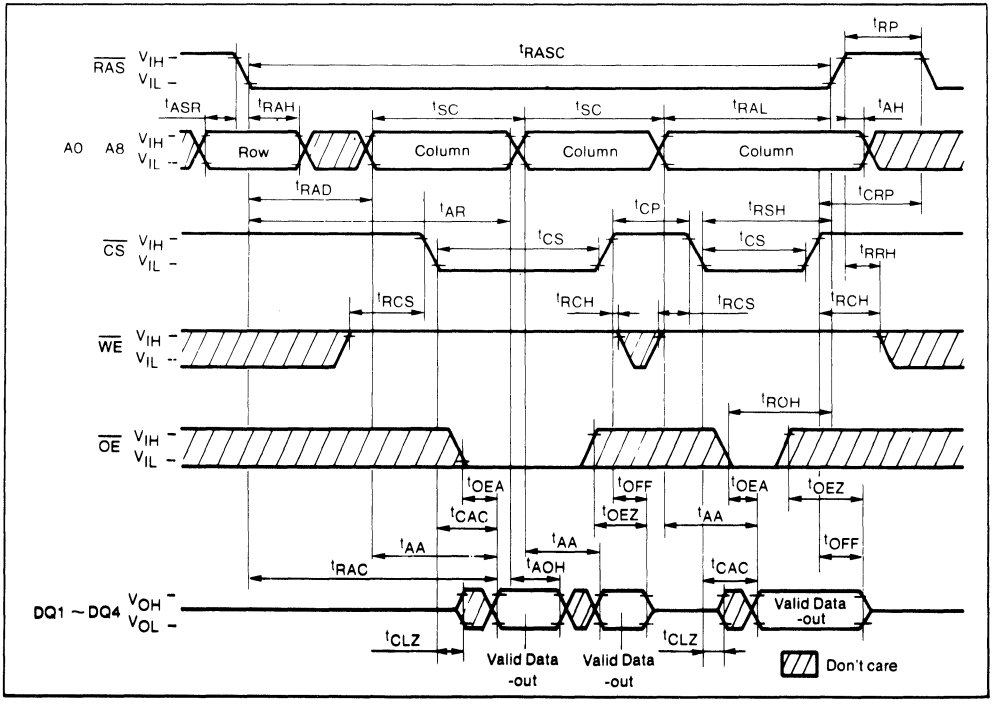
WRITE (OE CONTROL WRITE)



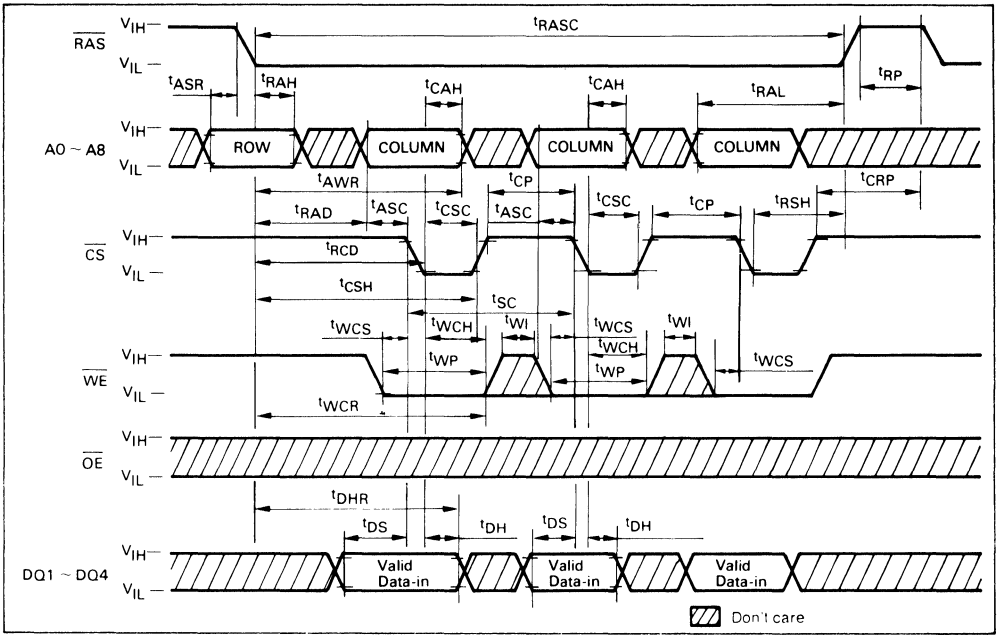
READ/WRITE CYCLE



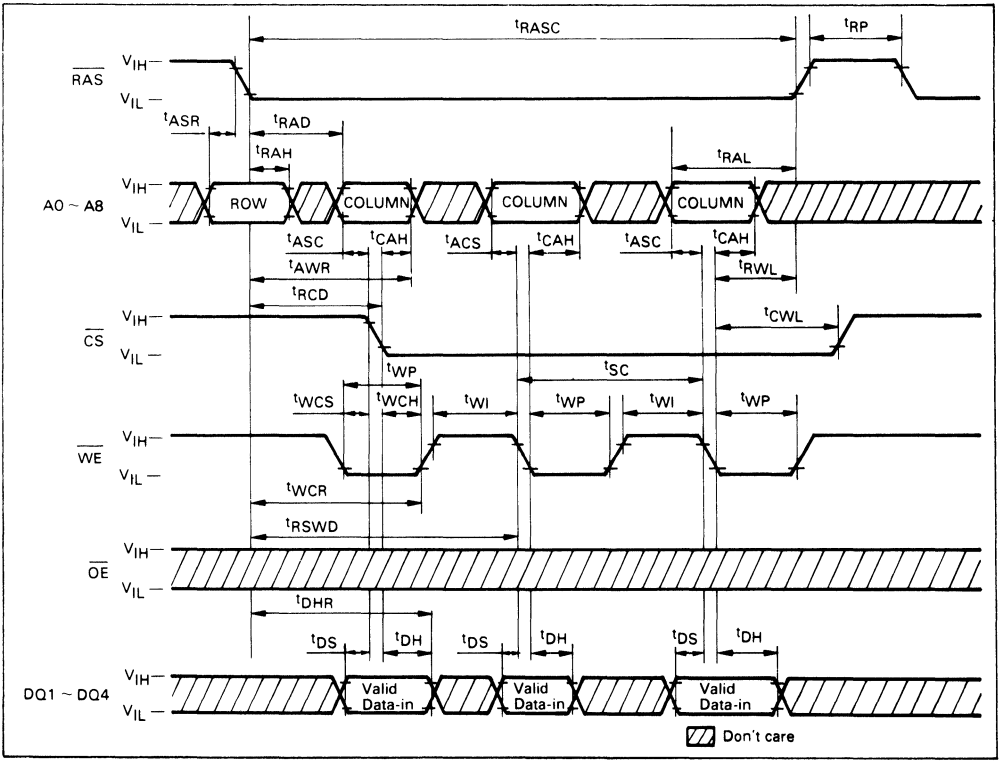
STATIC COLUMN MODE READ CYCLE



● STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



● STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



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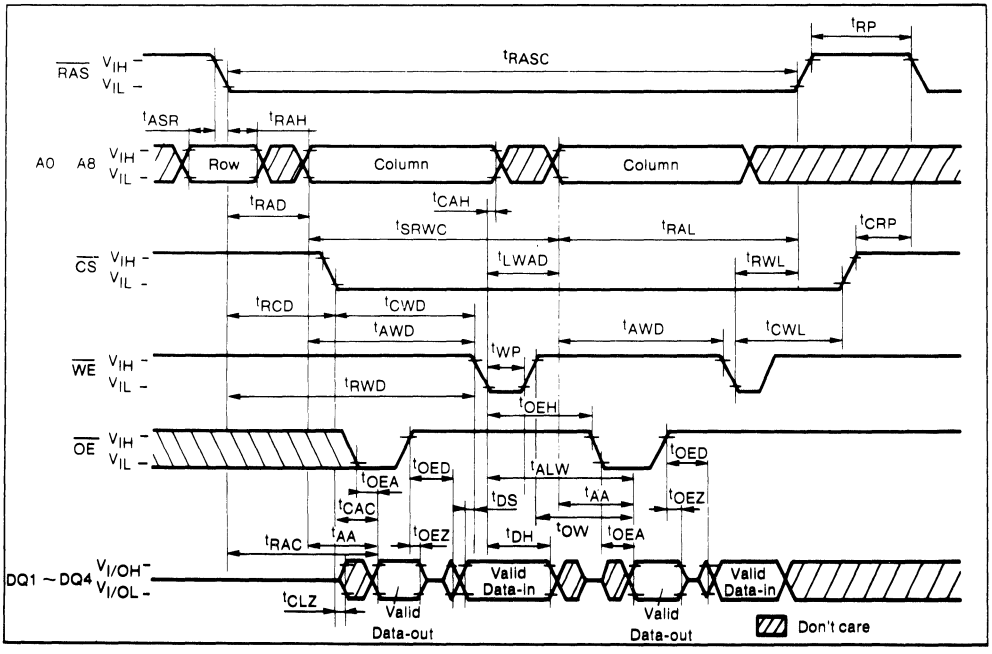
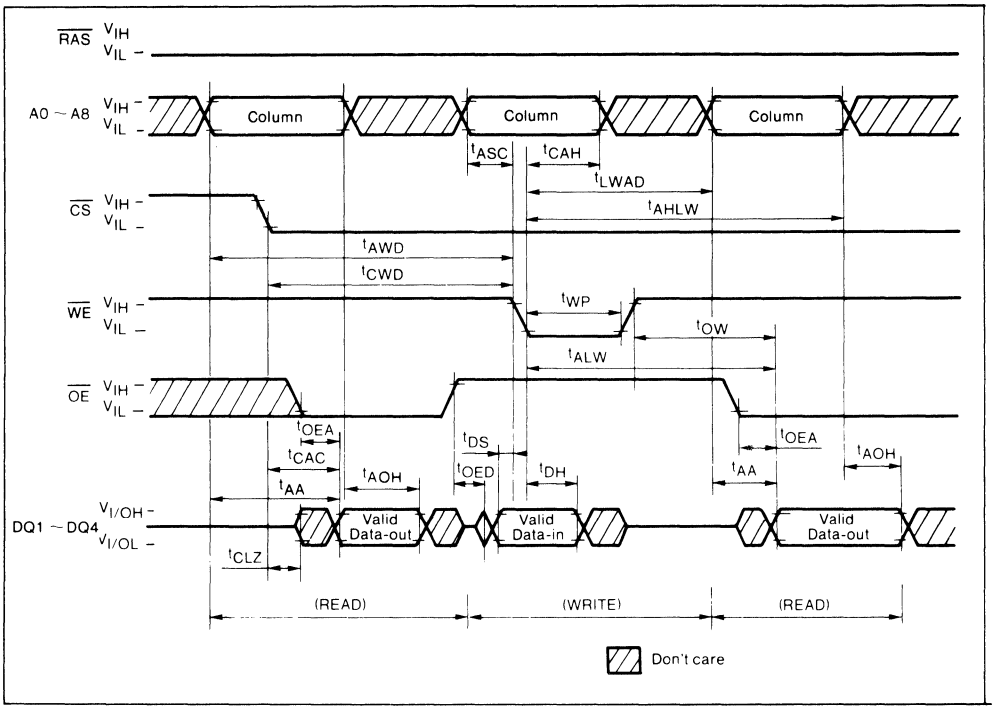
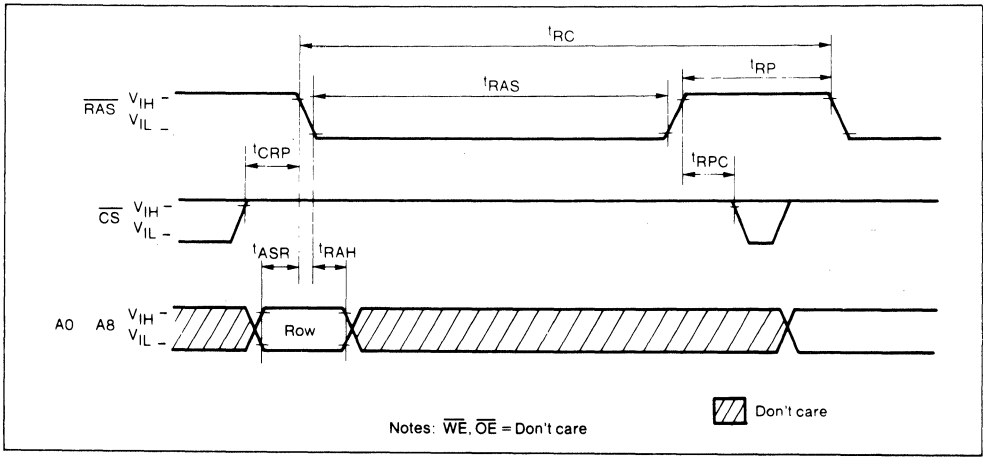
STATIC COLUMN MODE READ/WRITE CYCLE



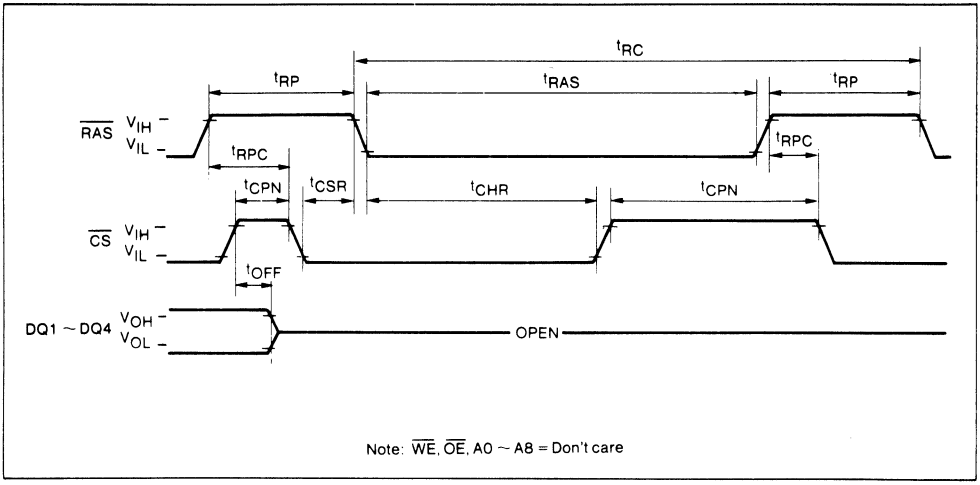
STATIC COLUMN MODE READ/WRITE MIXED CYCLE



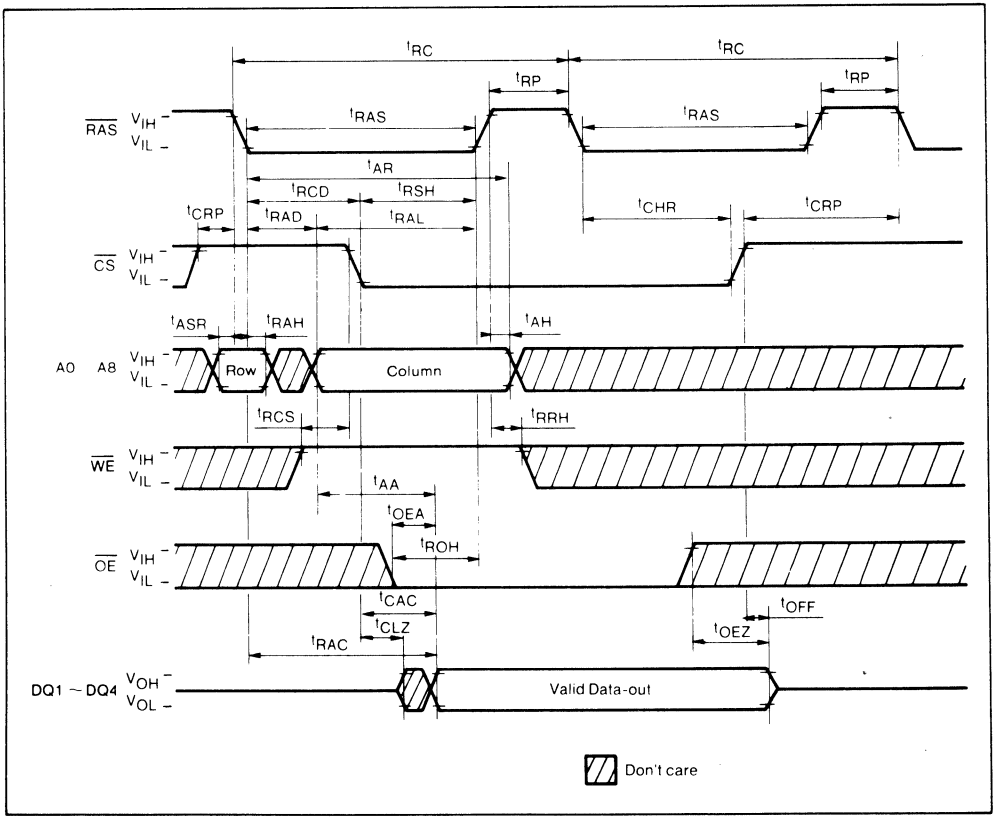
RAS ONLY REFRESH CYCLE



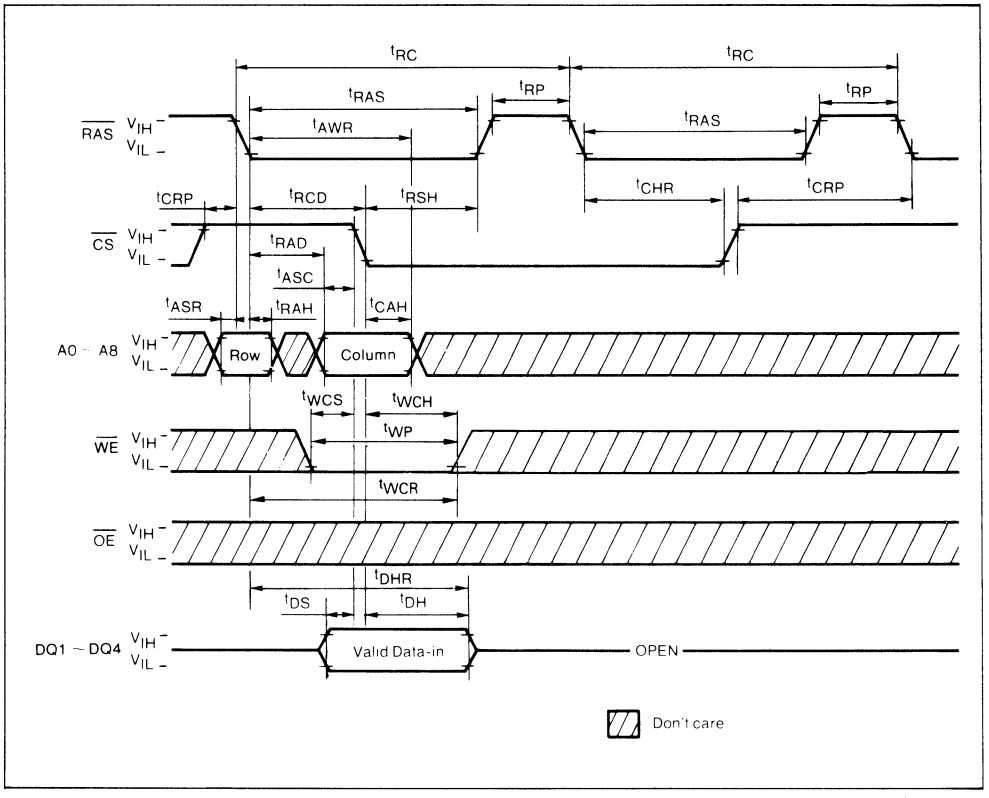
$\overline{CS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



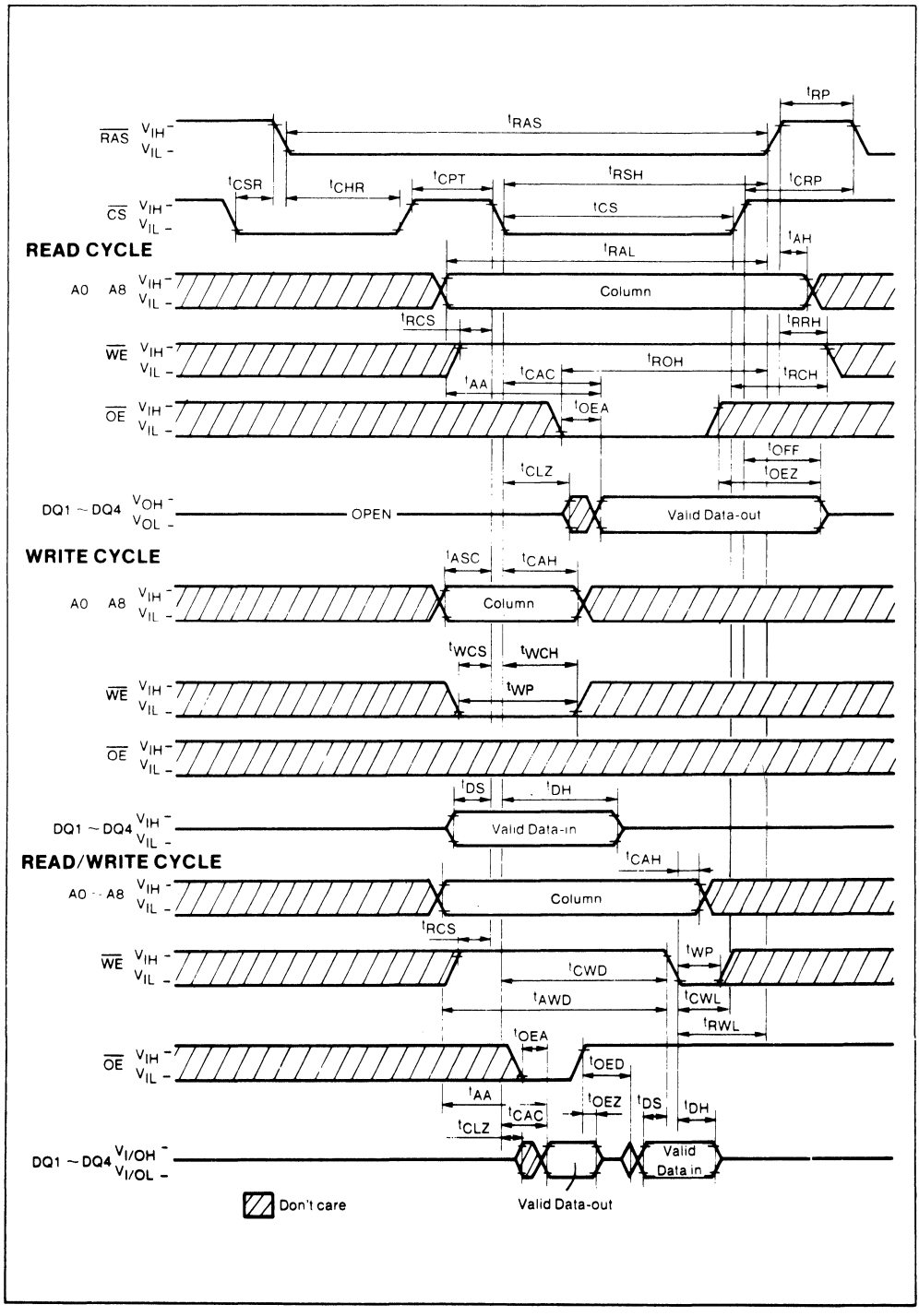
HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST



OKI semiconductor
MSM514100

4,194,304-WORD x 1-BIT DYNAMIC RAM: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The MSM514100 is a new generation dynamic RAM organized as 4,194,304 words by 1 bit. The technology used to fabricate the MSM514100 is OKI's CMOS silicon gate process technology. The device operates at a single + 5 V power supply. Its I/O pins are TTL compatible.

4

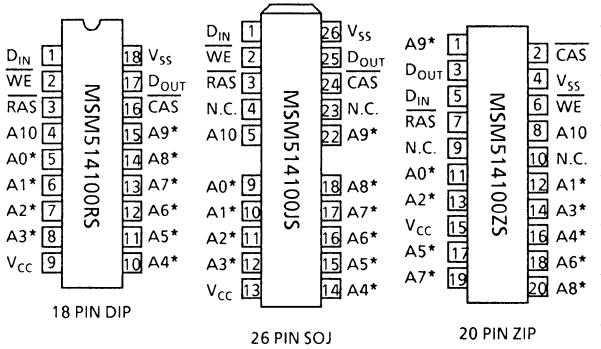
FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 4,194,304 word by 1 bit organization
- 350 mil 26-pin plastic SOJ, 400 mil 20-pin plastic ZIP, 400 mil 18-pin plastic DIP
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
					Operating (MAX)	Standby (MAX)
	t_{RAC}	t_{AA}	t_{CAC}			
MSM514100-8	80 ns	40 ns	20 ns	160 ns	495 mW	5.5 mW (MOS level)
MSM514100-8A	80 ns	40 ns	25 ns	160 ns	495 mW	
MSM514100-10	100 ns	50 ns	25 ns	190 ns	440 mW	

- Single + 5 V supply, ± 10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- Common I/O capability using "Early Write" operation
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Multi bit test mode capability
- Built-in V_{BB} generator circuit

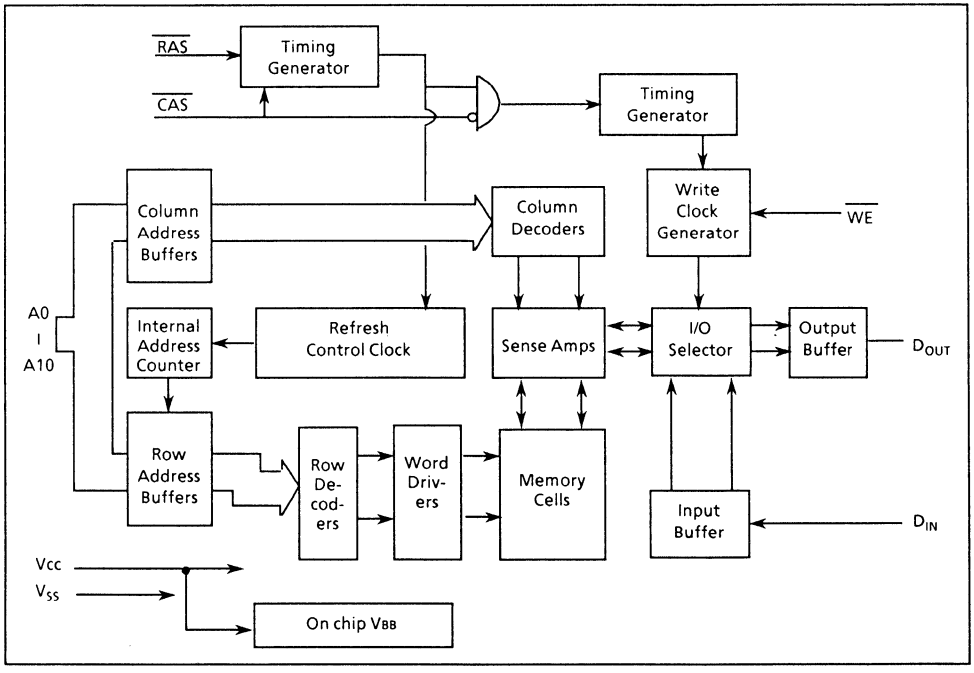
PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
A0 to A10	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply < + 5V >
V_{SS}	Ground <0V>
N.C.	No Connection

4

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit	Note
Voltage on any pin relative to V_{SS}	VT	Ta = 25 °C	− 1.0 to + 7.0	V	1
Short circuit output current	Ios	Ta = 25 °C	50	mA	1
Power dissipation	P_D	Ta = 25 °C	1	W	1
Operating temperature	Topr	−	0 to + 70	°C	1
Storage temperature	Tstg	−	− 55 to + 150	°C	1

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to + 70°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	2
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	−	6.5	V	2
Input low voltage	V_{IL}	− 1.0	−	0.8	V	2

Notes: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 514100-8		MSM 514100-8A		MSM 514100-10		Unit	Note
			MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0 V ≤ VI ≤ 6.5V; all other pins not under test = 0 V	−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} = disable 0 V ≤ VO ≤ 5.5 V	−10	10	−10	10	−10	10	μA	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	−	90	−	90	−	80	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, D_{OUT} = Hz — TTL	−	2	−	2	−	2	mA	
		MOS	−	1	−	1	−	1		
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min	−	90	−	90	−	80	mA	1, 2
Power supply current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} = enable	−	5	−	5	−	5	mA	1
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$	−	90	−	90	−	80	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min	−	80	−	80	−	70	mA	1, 3

Notes: 1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A10, D_{IN})	C_{IN1}	−	−	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	−	−	7	pF
Output capacitance (D_{OUT})	C_{OUT}	−	−	7	pF

AC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to +70°C) Note 1, 2, 3, 10, 11

Parameter	Symbol	MSM 514100-8		MSM 514100-8A		MSM 514100-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	160	–	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	185	–	190	–	220	–	ns	
Fast page mode cycle time	t_{PC}	55	–	55	–	65	–	ns	
Fast page mode read/write cycle time	t_{PRWC}	80	–	80	–	95	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	80	–	100	ns	4, 5
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	–	25	ns	4, 5
Access time from column address	t_{AA}	–	40	–	40	–	50	ns	4, 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	45	–	45	–	55	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	0	–	ns	4
Output buffer turn-off delay time	t_{OFF}	0	20	0	20	0	25	ns	7
Transition time	t_T	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	–	16	–	16	–	16	ms	
$\overline{RAS}$ precharge time	t_{RP}	70	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	25	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	80	–	100	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	55	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	40	20	50	ns	6
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	40	–	50	–	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSM 514100-8		MSM 514100-8A		MSM 514100-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	8
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	9
Write command hold time	t_{WCH}	15	–	15	–	20	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	60	–	75	–	ns	
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	25	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	60	–	75	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	20	–	25	–	25	–	ns	9
Column address to $\overline{WE}$ delay time	t_{AWD}	40	–	40	–	50	–	ns	9
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	–	80	–	100	–	ns	9
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	20	–	20	–	20	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	20	–	20	–	20	–	ns	
$\overline{RAS}$ to $\overline{WE}$ set-up time (Test mode)	t_{WSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{WE}$ hold time (Test mode)	t_{WHR}	20	–	20	–	20	–	ns	

Notes: 1. An initial pause of 200 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is achieved.
In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles is required.

2. The AC characteristics assume $t_T = 5$ ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2TTL loads and 100pF.

5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

7. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

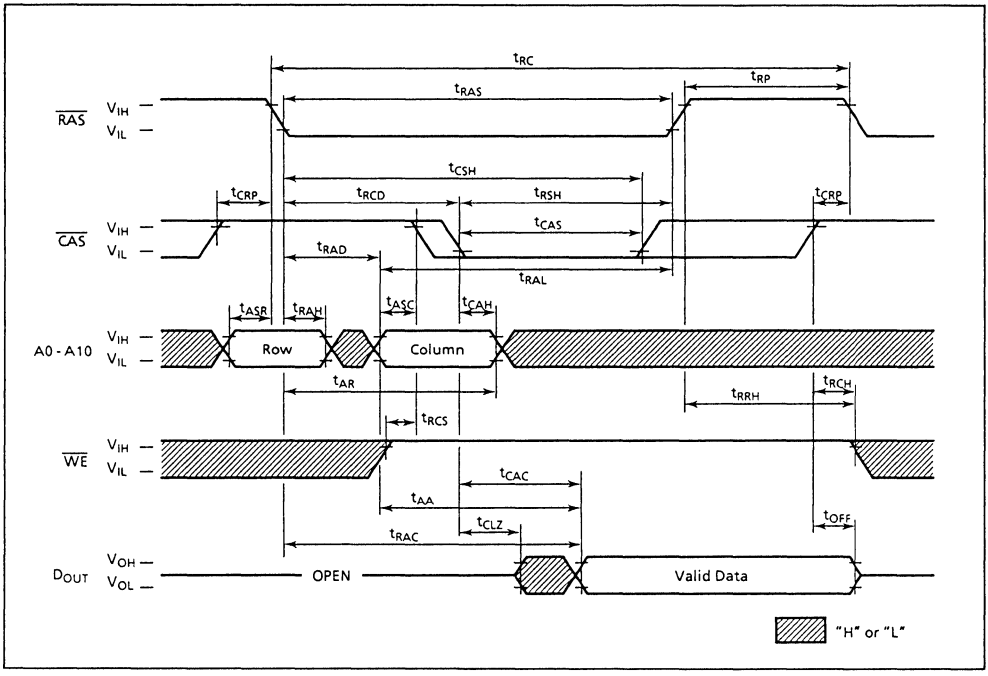
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

9. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

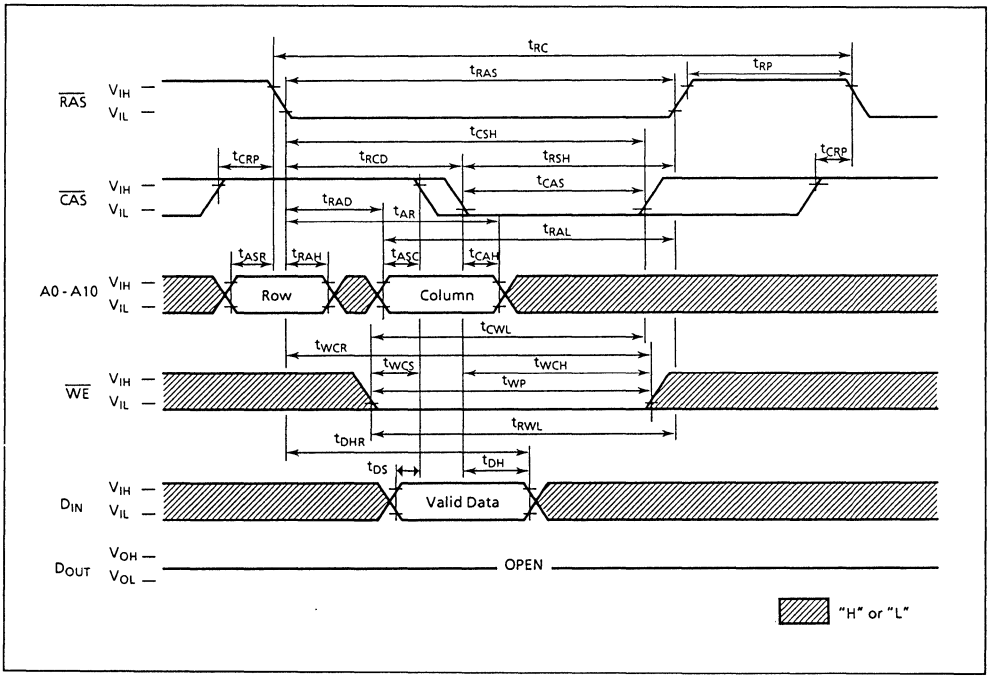
10. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remain in effect until the exit cycle is generated.
The test mode specified in this data sheet is 8-bit parallel test function.
RA10, CA10 and CA0 are not used. In a read cycle, if all internal bits are equal, the data output pin will indicate a high level. If any internal bits are not equal, then data output pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

11. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

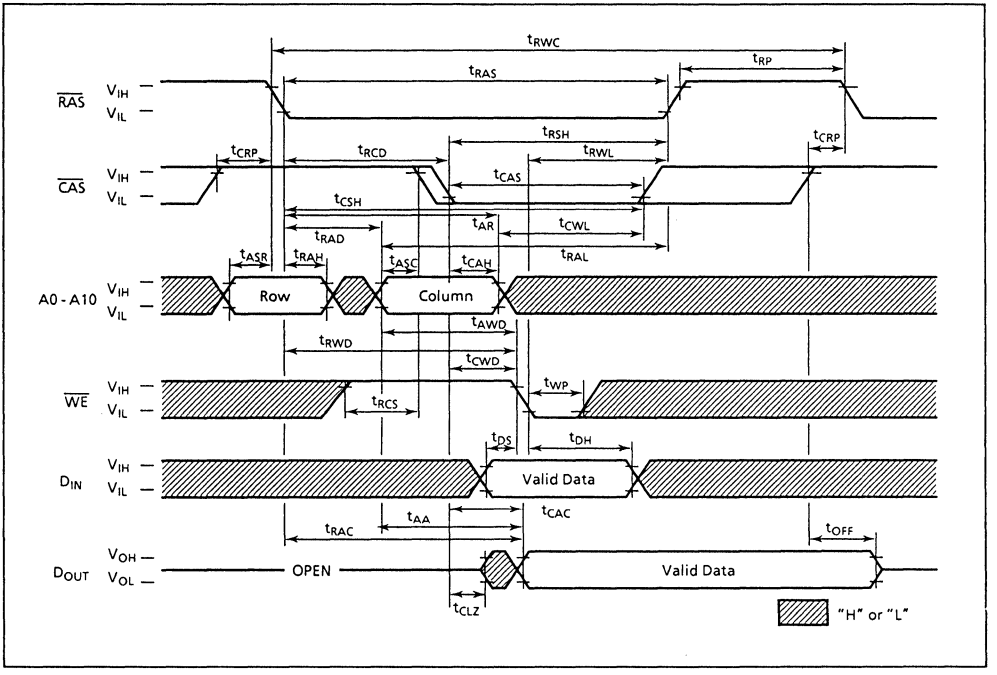
READ CYCLE



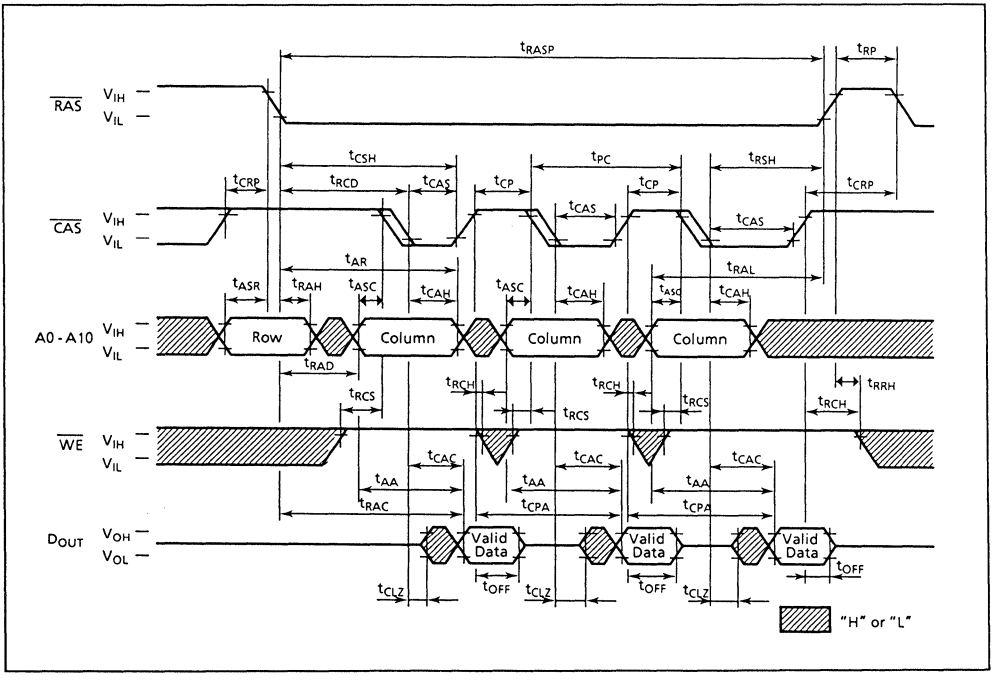
WRITE CYCLE (EARLY WRITE)



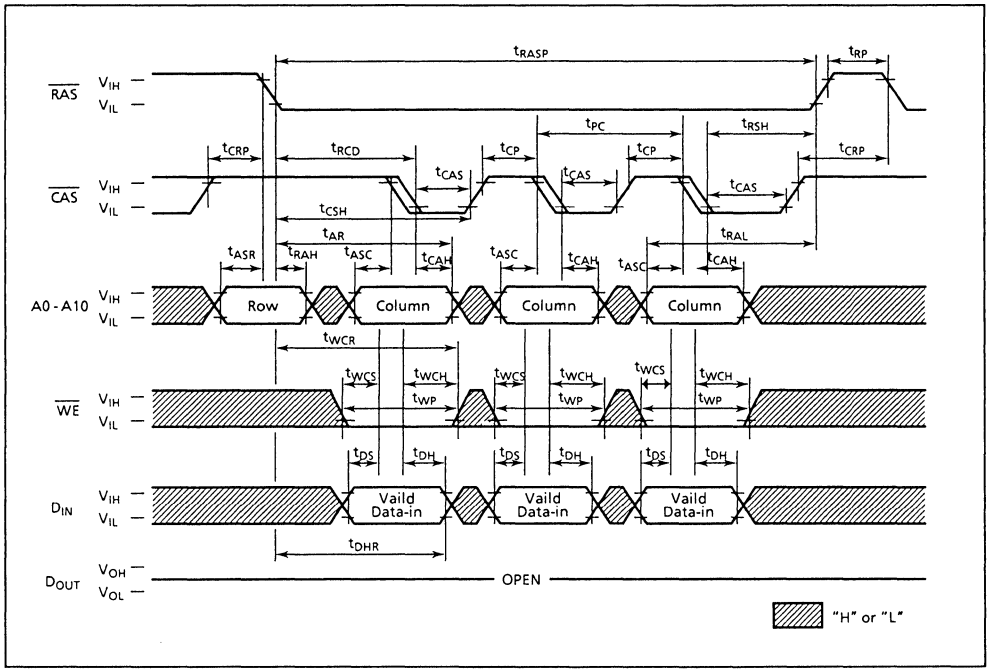
READ/WRTIE CYCLE



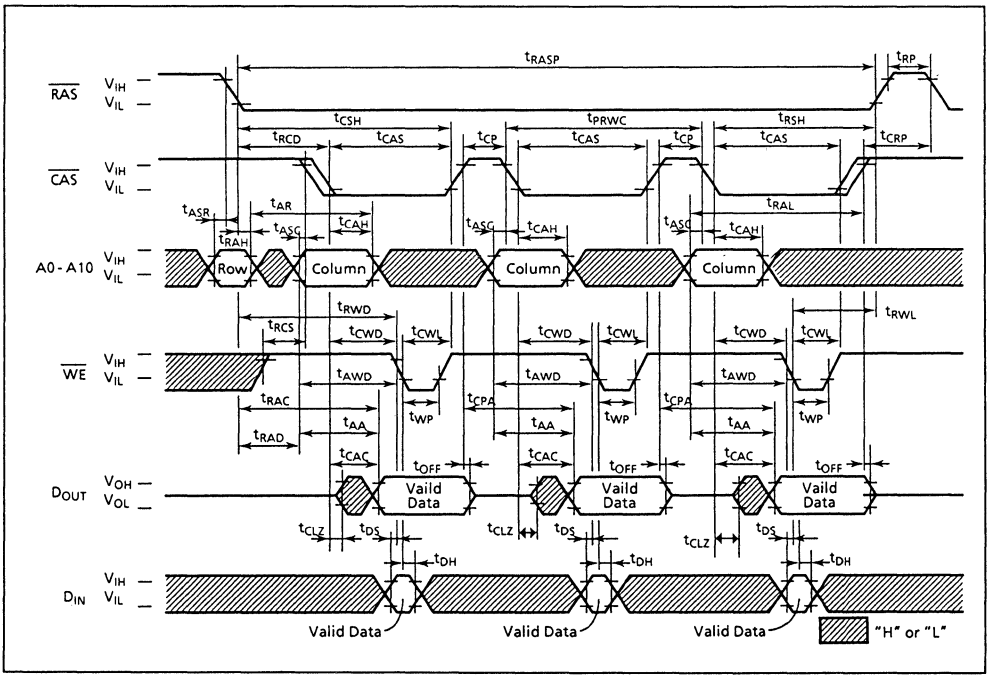
FAST PAGE MODE READ CYCLE



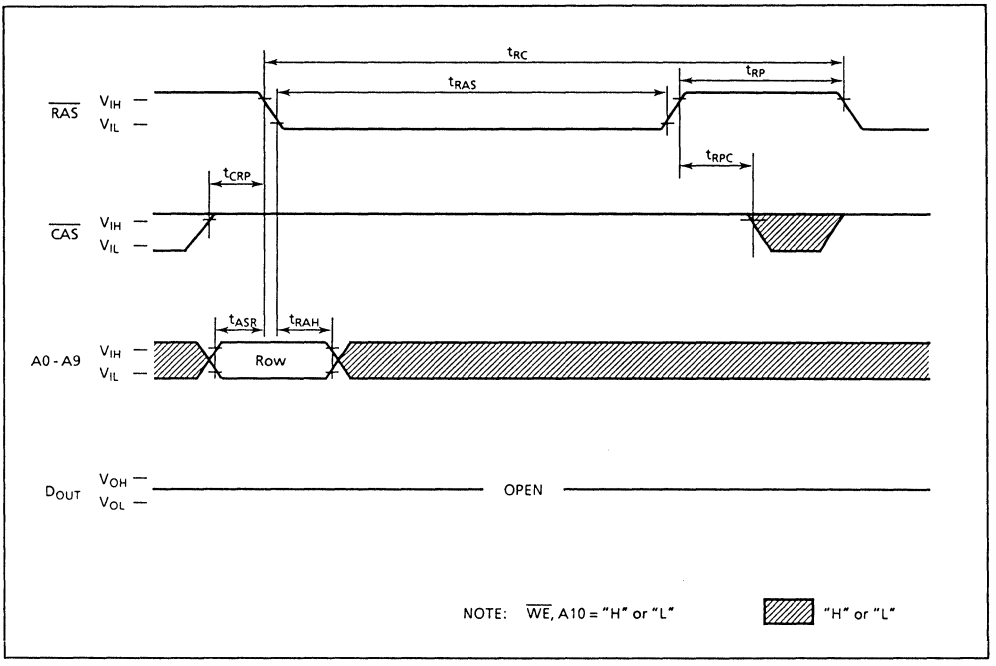
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



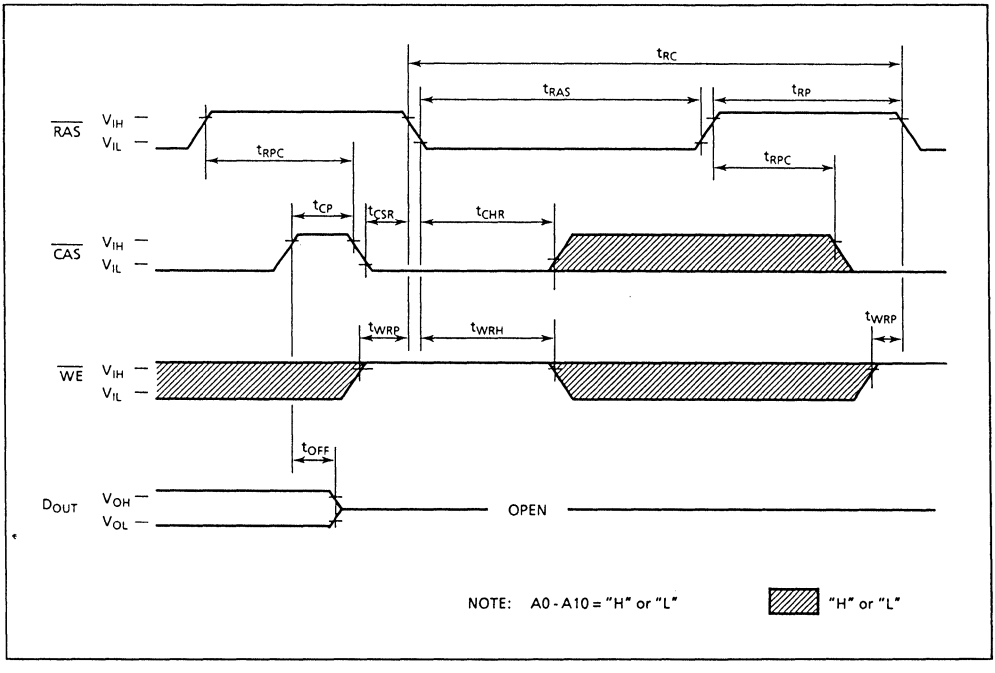
FAST PAGE MODE READ/WRITE CYCLE



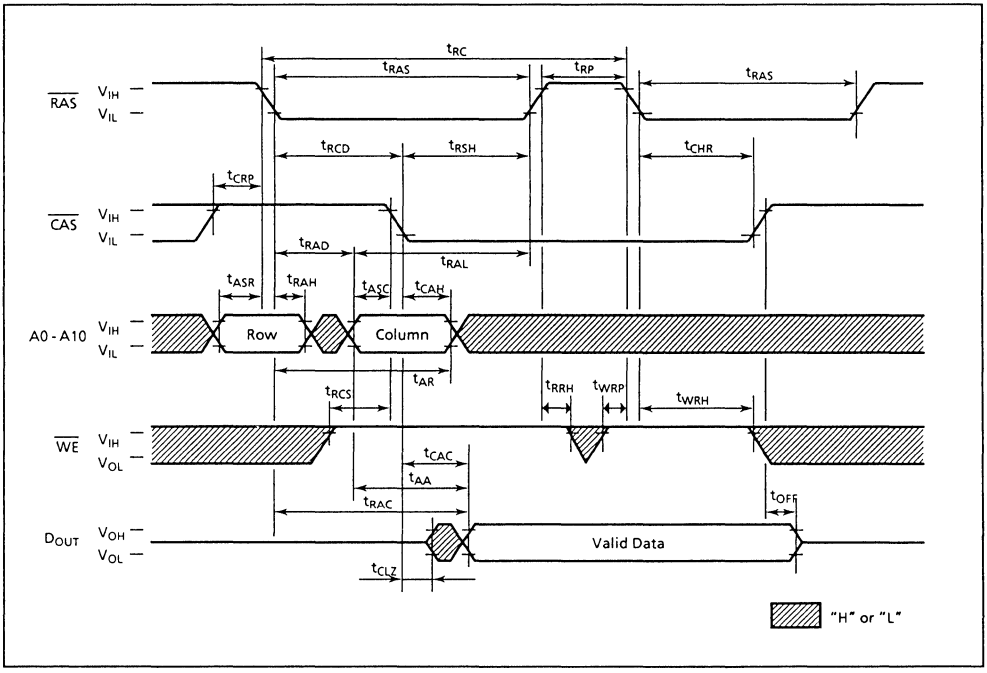
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



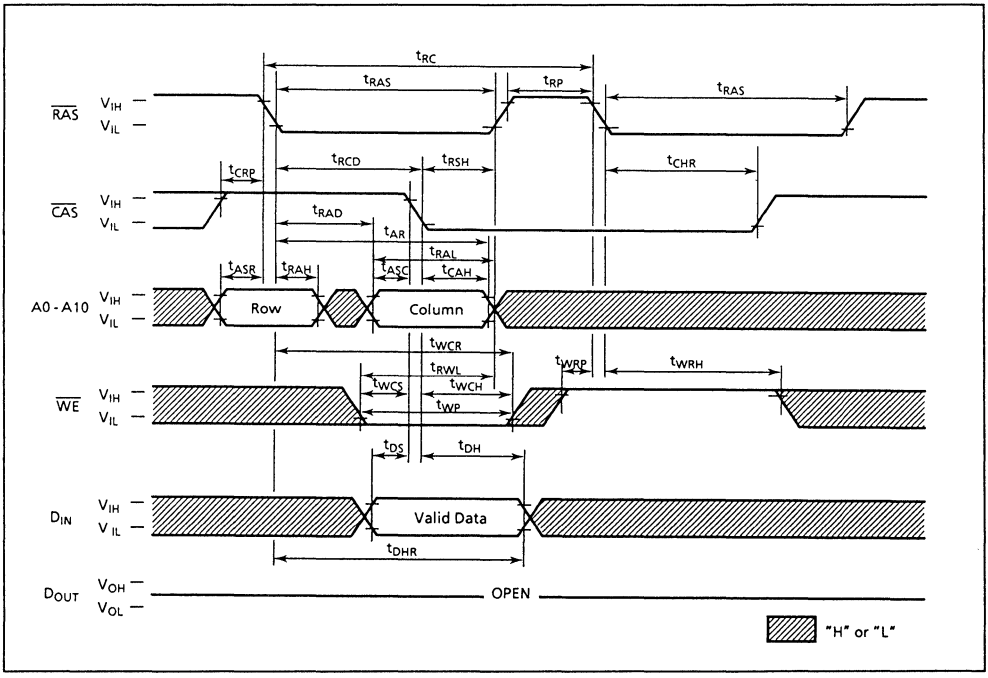
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ AUTO REFRESH CYCLE



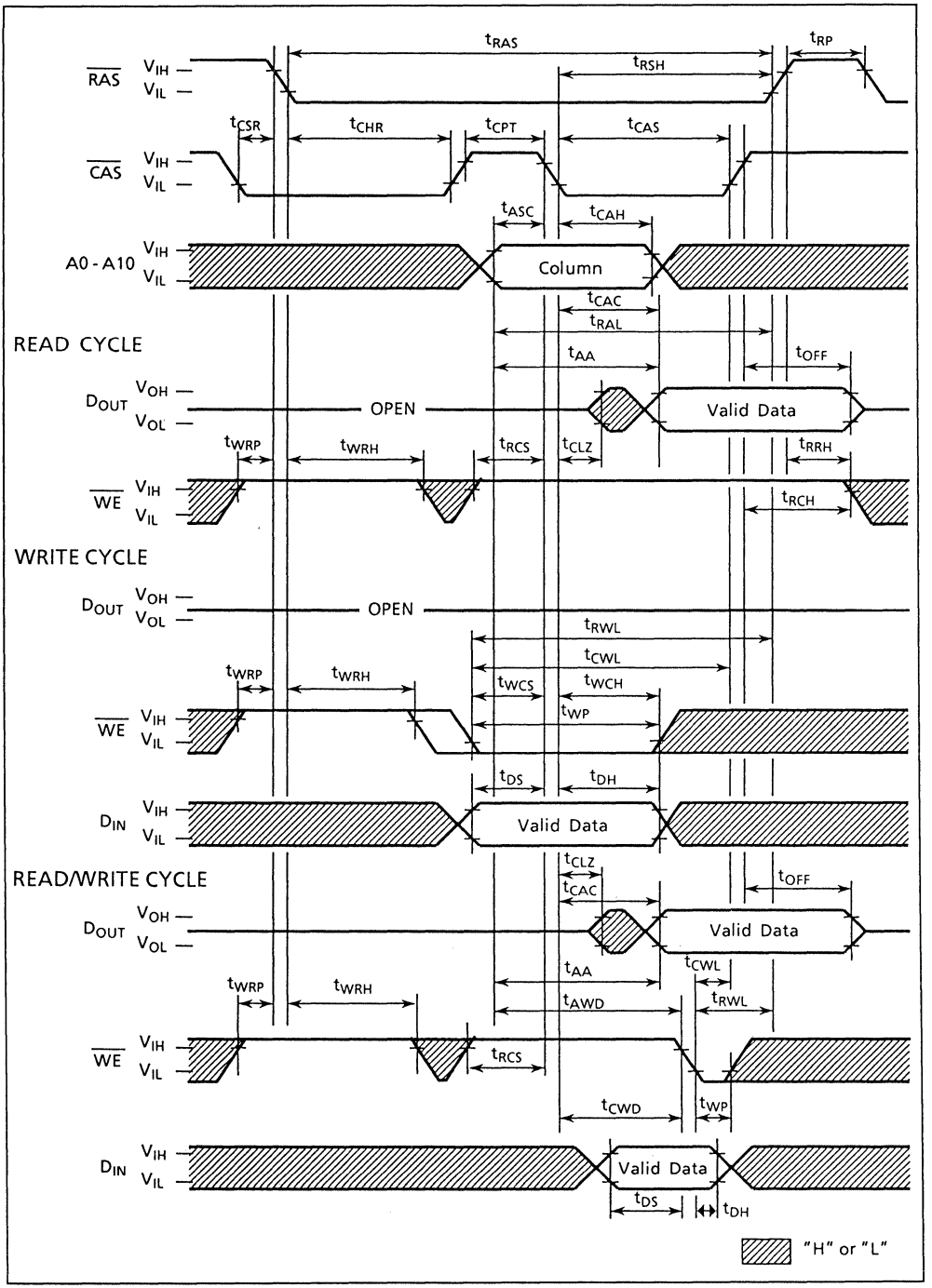
HIDDEN REFRESH READ CYCLE



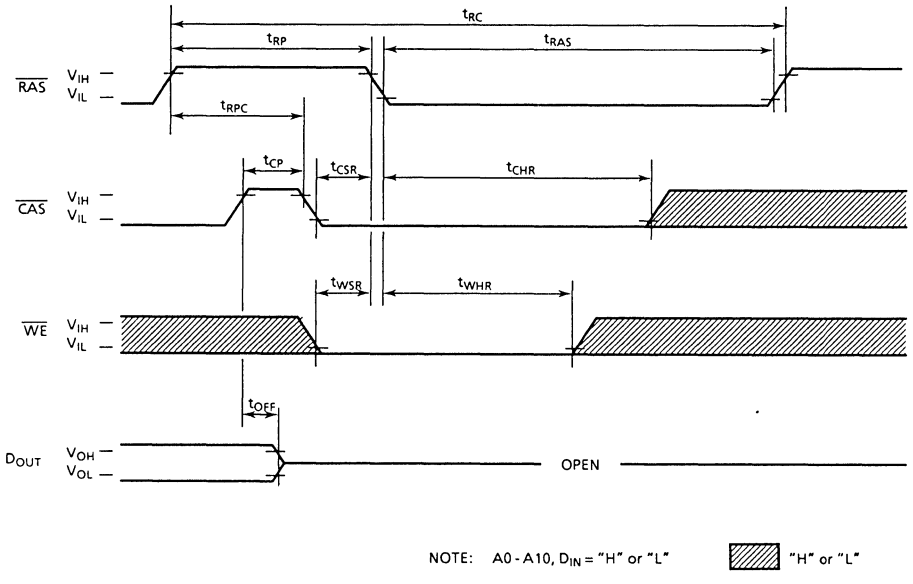
HIDDEN REFRESH WRITE CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TEST MODE INITIATE CYCLE



OKI semiconductor
MSM514102

4,194,304-WORD x 1-BIT DYNAMIC RAM: STATIC COLUMN MODE TYPE

GENERAL DESCRIPTION

The MSM514102 is a new generation dynamic RAM organized as 4,194,304 words by 1 bit. The technology used to fabricate the MSM514102 is OKI's CMOS silicon gate process technology. The device operates at a single + 5 V power supply. Its I/O pins are TTL compatible.

4

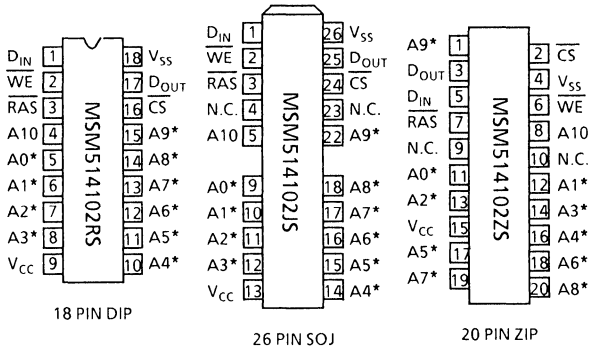
FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1-transistor memory cell
- 4,194,304 word by 1 bit organization
- 350 mil 26-pin plastic SOJ, 400 mil 20-pin plastic ZIP, 400 mil 18-pin plastic DIP
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
					Operating (MAX)	Standby (MAX)
	t_{RAC}	t_{AA}	t_{CAC}			
MSM514102-8	80 ns	40 ns	20 ns	160 ns	495 mW	5.5 mW (MOS level)
MSM514102-8A	80 ns	40 ns	25 ns	160 ns	495 mW	
MSM514102-10	100 ns	50 ns	25 ns	190 ns	440 mW	

- Single + 5 V supply, ± 10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- Common I/O capability using "Early Write" operation
- $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{CS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Multi bit test mode capability
- Built-in V_{BB} generator circuit

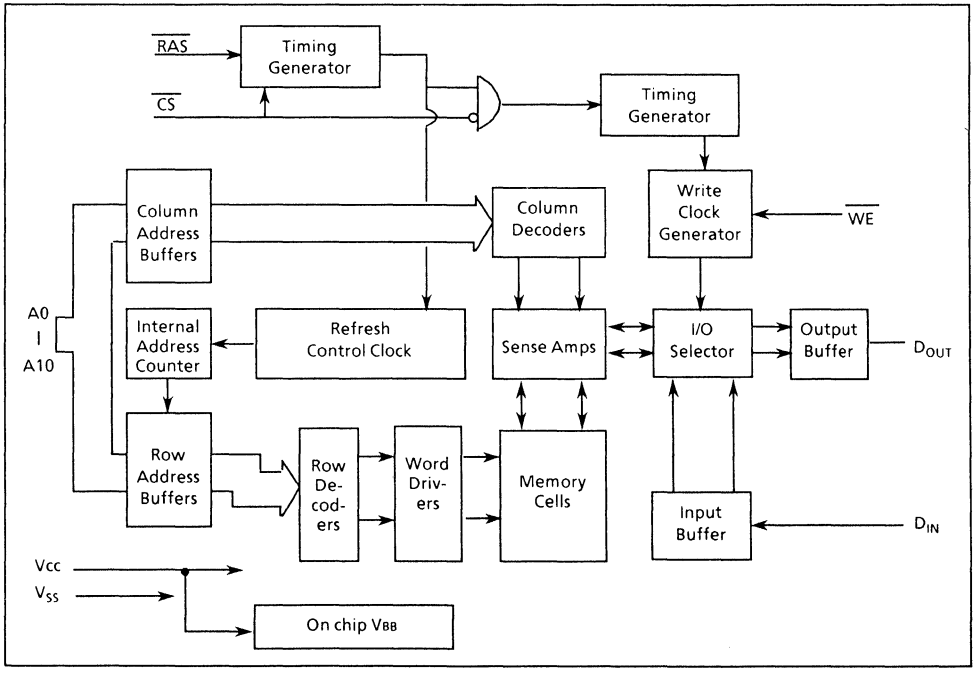
PIN CONFIGURATION (TOP VIEW)



* Refresh Address

Pin Names	Function
A0 to A10	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply < + 5V >
V_{SS}	Ground <0V>
N.C.	No Connection

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit	Note
Voltage on any pin relative to V_{SS}	VT	Ta = 25 °C	− 1.0 to + 7.0	V	1
Short circuit output current	Ios	Ta = 25 °C	50	mA	1
Power dissipation	P_D	Ta = 25 °C	1	W	1
Operating temperature	Topr	−	0 to + 70	°C	1
Storage temperature	Tstg	−	− 55 to + 150	°C	1

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to + 70°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	2
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	−	6.5	V	2
Input low voltage	V_{IL}	− 1.0	−	0.8	V	2

Notes: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 514102-8		MSM 514102-8A		MSM 514102-10		Unit	Note
			MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0 V ≤ VI ≤ 6.5V; all other pins not under test = 0 V	−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} = disable 0 V ≤ VO ≤ 5.5 V	−10	10	−10	10	−10	10	μA	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ cycling, t_{RC} = min	−	90	−	90	−	80	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IH}, D_{OUT} = Hz — TTL	−	2	−	2	−	2	mA	
		$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IH}, D_{OUT} = Hz — MOS	−	1	−	1	−	1	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CS}$ = V_{IH}, t_{RC} = min	−	90	−	90	−	80	mA	1, 2
Power supply current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL}, D_{OUT} = enable	−	5	−	5	−	5	mA	1
Average power supply current ($\overline{CS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CS}$ before $\overline{RAS}$	−	90	−	90	−	80	mA	1
Average power supply current (Static column mode)	I_{CC9}	$\overline{RAS}$ = V_{IL}, $\overline{CS}$ = V_{IL}, t_{SC} = min	−	80	−	80	−	70	mA	1

Notes: 1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A10, D_{IN})	C_{IN1}	−	−	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WE}$)	C_{IN2}	−	−	7	pF
Output capacitance (D_{OUT})	C_{OUT}	−	−	7	pF

AC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to +70°C) Note 1, 2, 3, 11, 12

Parameter	Symbol	MSM 514102-8		MSM 514102-8A		MSM 514102-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	160	–	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	185	–	190	–	220	–	ns	
Static column mode cycle time	t_{SC}	45	–	45	–	55	–	ns	
Static column mode read/write cycle time	t_{SRWC}	70	–	70	–	80	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	80	–	100	ns	4, 5, 6
Access time from $\overline{CS}$	t_{CAC}	–	20	–	25	–	25	ns	4. 5
Access time from column address	t_{AA}	–	40	–	40	–	50	ns	4. 6, 7
Access time from last write	t_{ALW}	–	75	–	75	–	95	ns	4, 7
Data output enable time reference to $\overline{WE}$	t_{OW}	–	20	–	25	–	25	ns	
Output low impedance time from $\overline{CS}$	t_{CLZ}	0	–	0	–	0	–	ns	4
Data output hold time reference to column address	t_{AOH}	5	–	5	–	5	–	ns	
Data output hold time reference to $\overline{WE}$	t_{WOH}	0	–	0	–	0	–	ns	
Output buffer turn-off delay time	t_{OFF}	0	20	0	20	0	25	ns	8
Transition time	t_T	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	–	16	–	16	–	16	ms	
$\overline{RAS}$ precharge time	t_{RP}	70	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	80	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	25	–	ns	
$\overline{CS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{CS}$ pulse width	t_{CS}	20	100,000	25	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	80	–	80	–	100	–	ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	22	60	25	55	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	40	20	50	ns	6
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	20	–	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSM 514102-8		MSM 514102-8A		MSM 514102-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Column address hold time reference to $\overline{RAS}$ (WRITE CYCLE)	t_{AWR}	60	–	60	–	75	–	ns	
Column address hold time reference to $\overline{RAS}$	t_{AR}	95	–	95	–	115	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	40	–	50	–	ns	
Column address hold time reference to $\overline{RAS}$ precharge	t_{AH}	10	–	10	–	10	–	ns	
Column address hold time reference to $\overline{WE}$	t_{AHLW}	75	–	75	–	95	–	ns	
Last write to column address delay time	t_{LWAD}	20	35	20	35	25	45	ns	7
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time reference to $\overline{CS}$	t_{RCH}	0	–	0	–	0	–	ns	9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	9
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	10
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	60	–	75	–	ns	
Write invalid time	t_{WI}	10	–	10	–	10	–	ns	
Write command hold time (Dout disable)	t_{WH}	0	–	0	–	0	–	ns	10
Write command to $\overline{CS}$ lead time	t_{CWL}	20	–	25	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	25	–	ns	
$\overline{CS}$ to $\overline{WE}$ delay time	t_{CWD}	20	–	25	–	25	–	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	40	–	40	–	50	–	ns	10
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	–	80	–	100	–	ns	10
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	60	–	75	–	ns	
$\overline{CS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CS}$ set-up time ($\overline{CS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CS}$ hold time ($\overline{CS}$ before $\overline{RAS}$)	t_{CHR}	20	–	20	–	20	–	ns	
$\overline{CS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CS}$ before $\overline{RAS}$)	t_{WRP}	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CS}$ before $\overline{RAS}$)	t_{WRH}	20	–	20	–	20	–	ns	
$\overline{RAS}$ to $\overline{WE}$ set-up time (Test mode)	t_{WSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{WE}$ hold time (Test mode)	t_{WHR}	20	–	20	–	20	–	ns	

Notes: 1. An initial pause of 200 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is achieved.
In case of using internal refresh counter, a minimum of eight $\overline{CS}$ before $\overline{RAS}$ initialization cycles is required.

2. The AC characteristics assume $t_T = 5$ ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2TTL loads and 100pF.

5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

7. Operation within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met. t_{LWAD} (max.) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

8. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

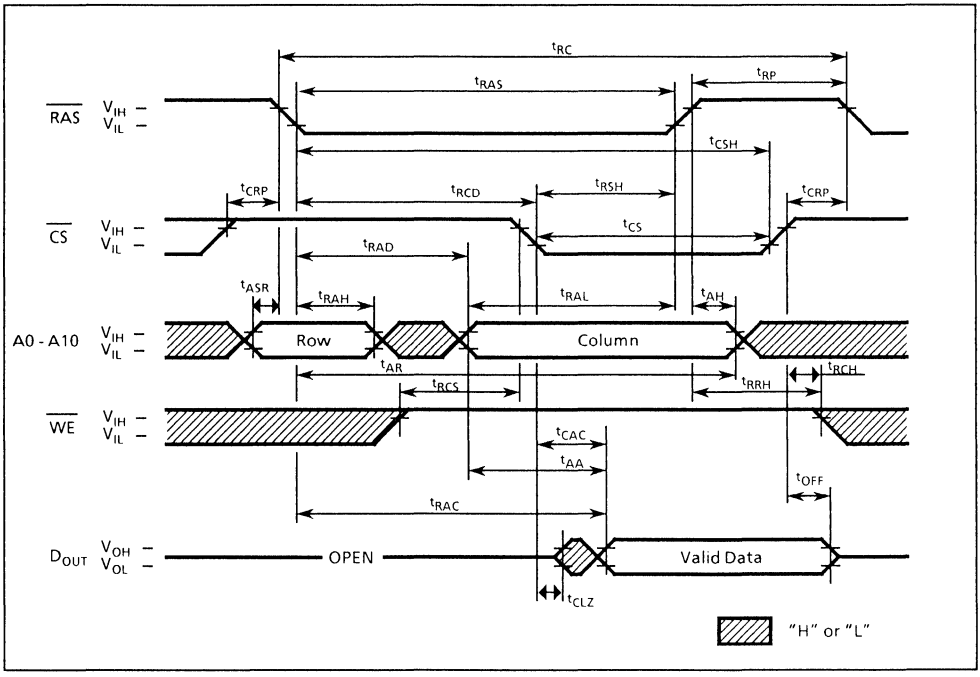
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

10. t_{WCS}, t_{WH}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) and $t_{WH} \geqq t_{WH}$ (min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

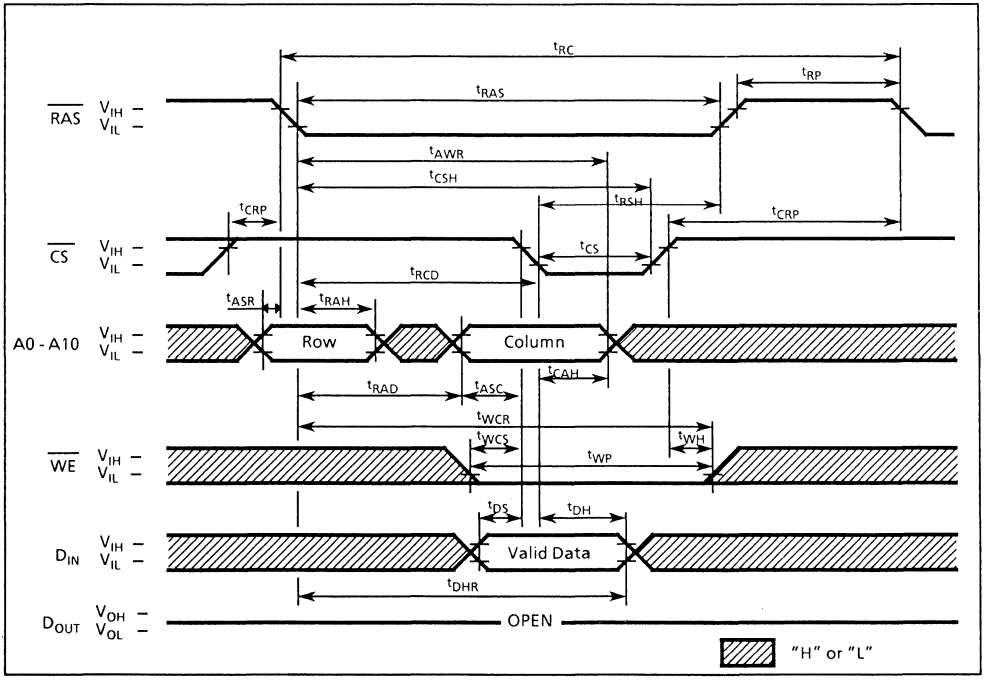
11. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CS}$ before $\overline{RAS}$ refresh cycle.
This mode is latched and remain in effect until the exit cycle is generated.
The test mode specified in this data sheet is 8-bit parallel test function.
RA10, CA10 and CA0 are not used. In a read cycle, if all internal bits are equal, the data output pin will indicate a high level. If any internal bits are not equal, then data output pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$ only refresh cycle or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle.

12. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

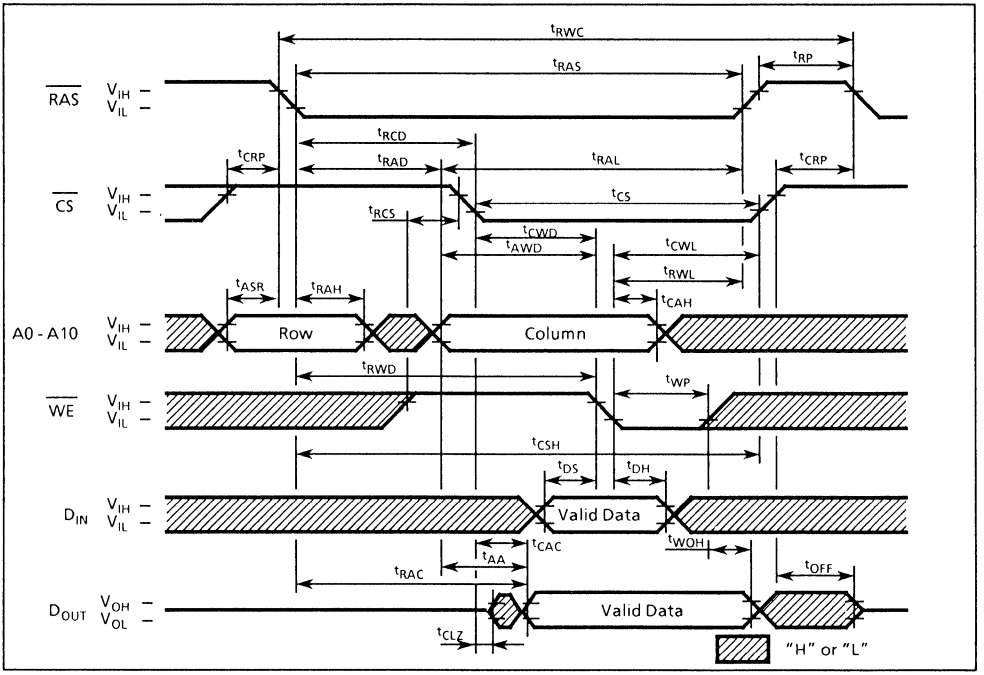
READ CYCLE



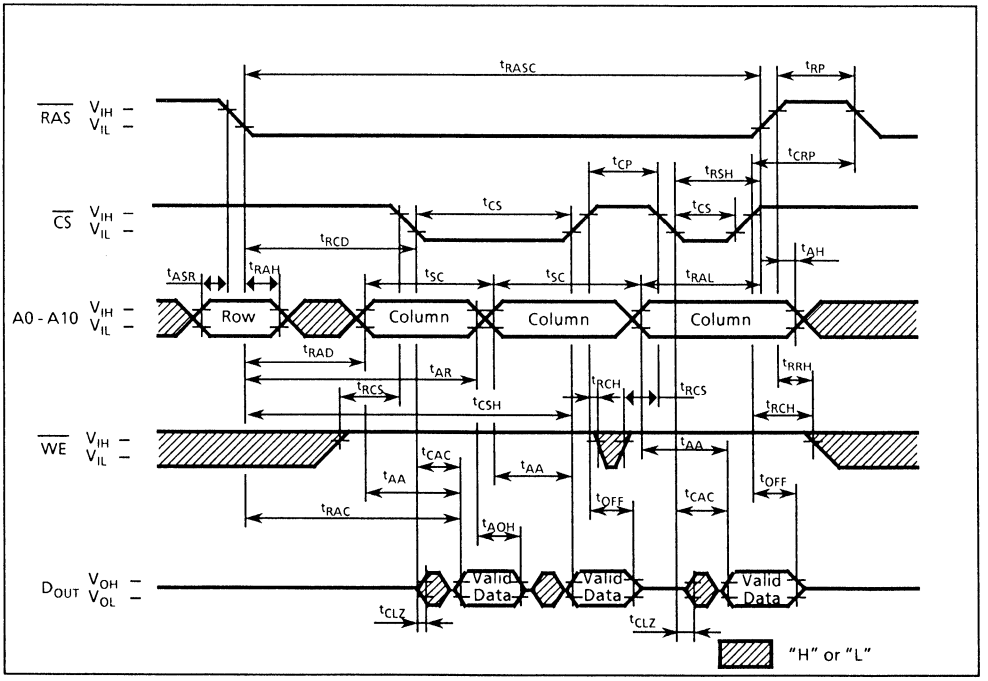
WRITE CYCLE (EARLY WRITE)



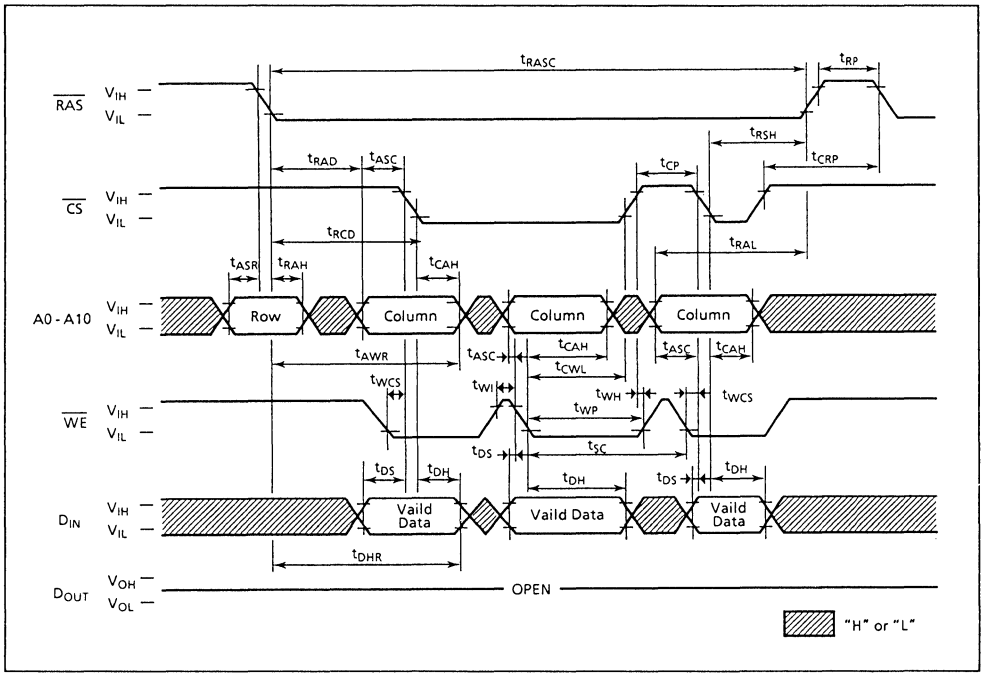
READ/WRITE CYCLE



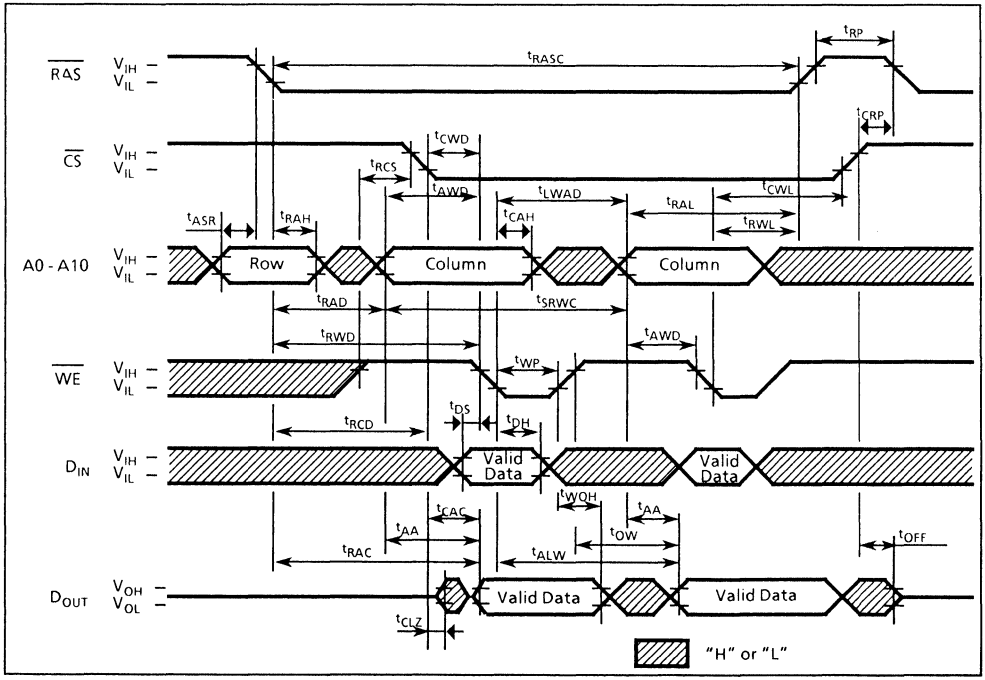
STATIC COLUMN MODE READ CYCLE



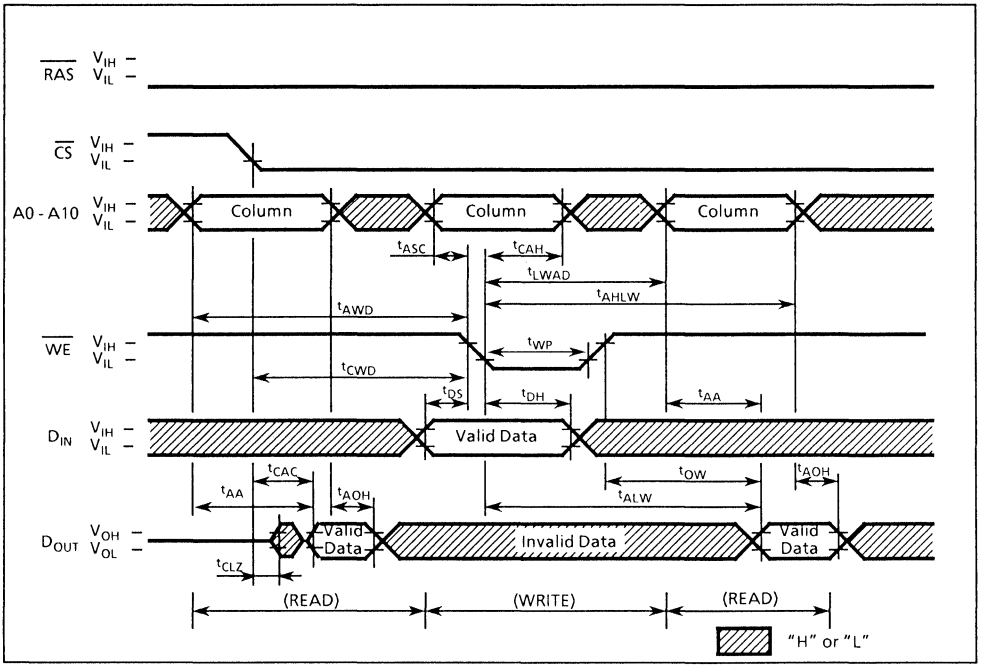
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



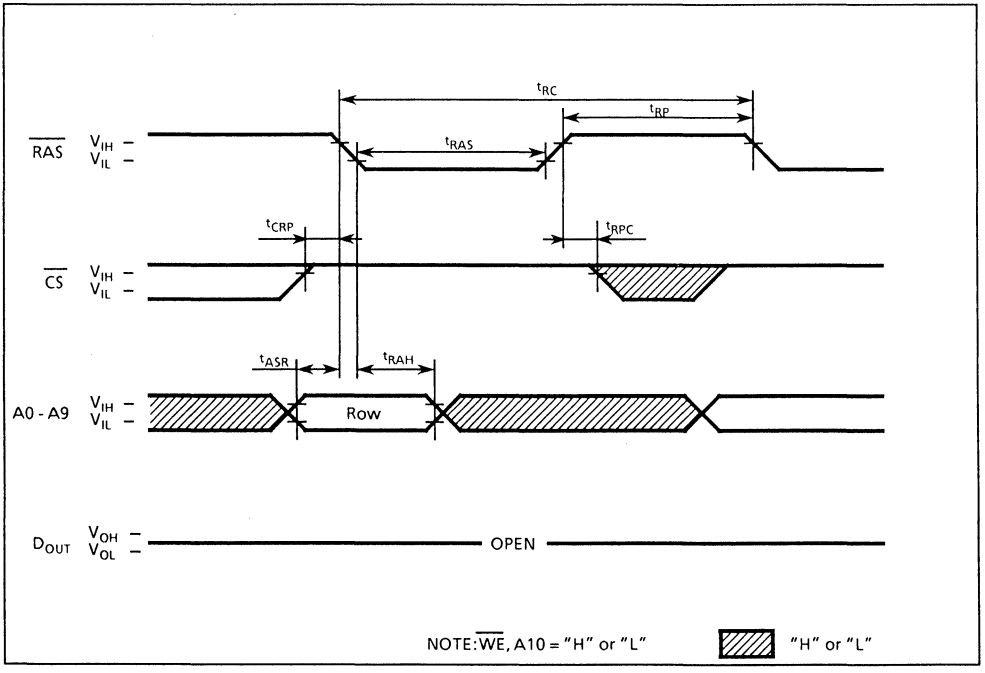
STATIC COLUMN MODE READ/WRITE CYCLE



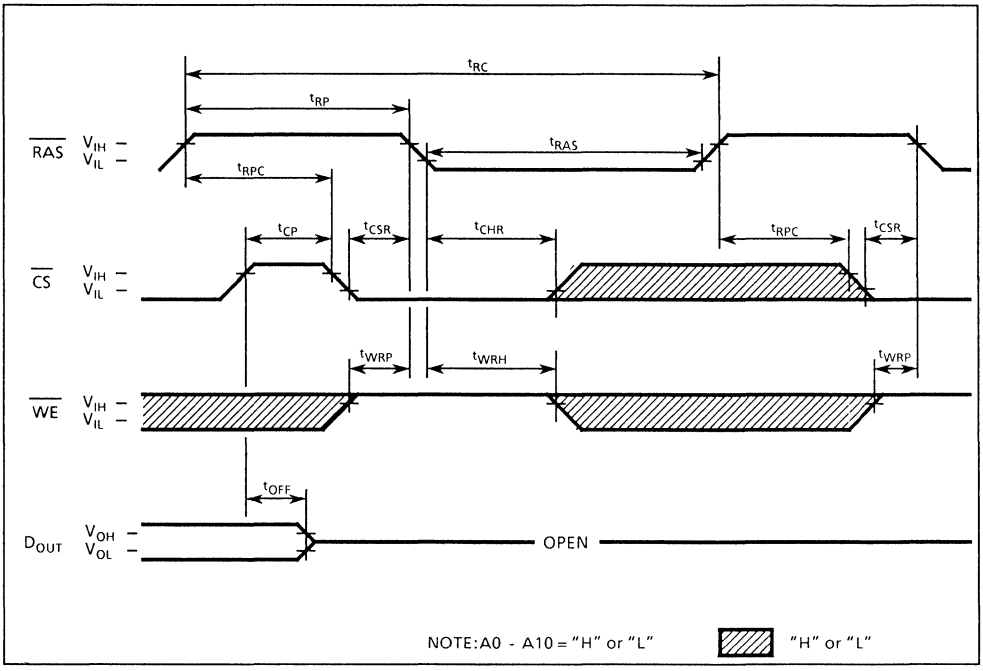
STATIC COLUMN MODE READ/WRITE MIXED CYCLE



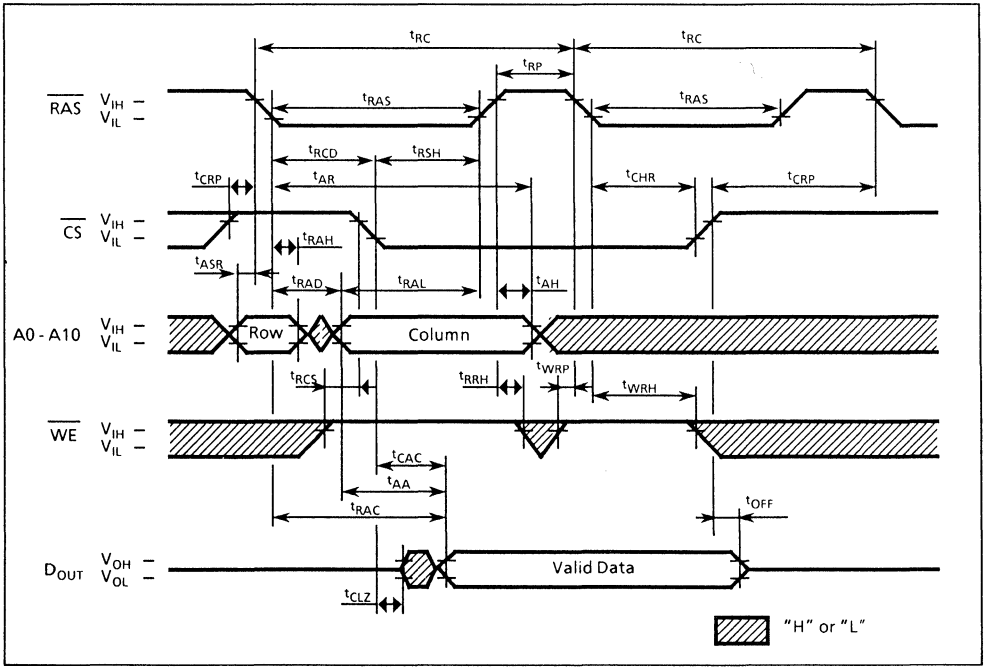
RAS ONLY REFRESH CYCLE



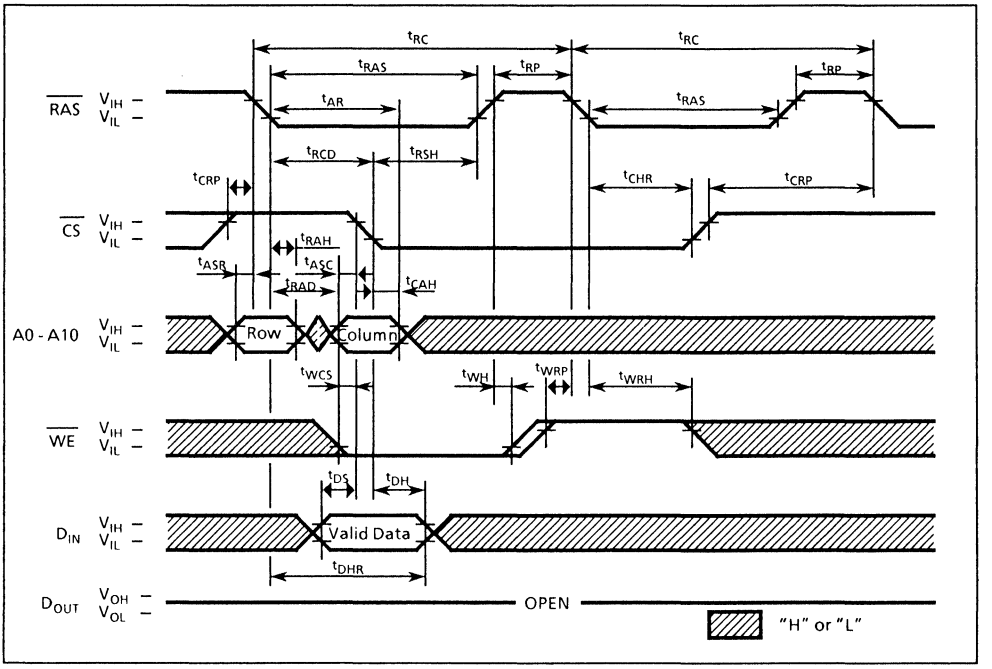
$\overline{CS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



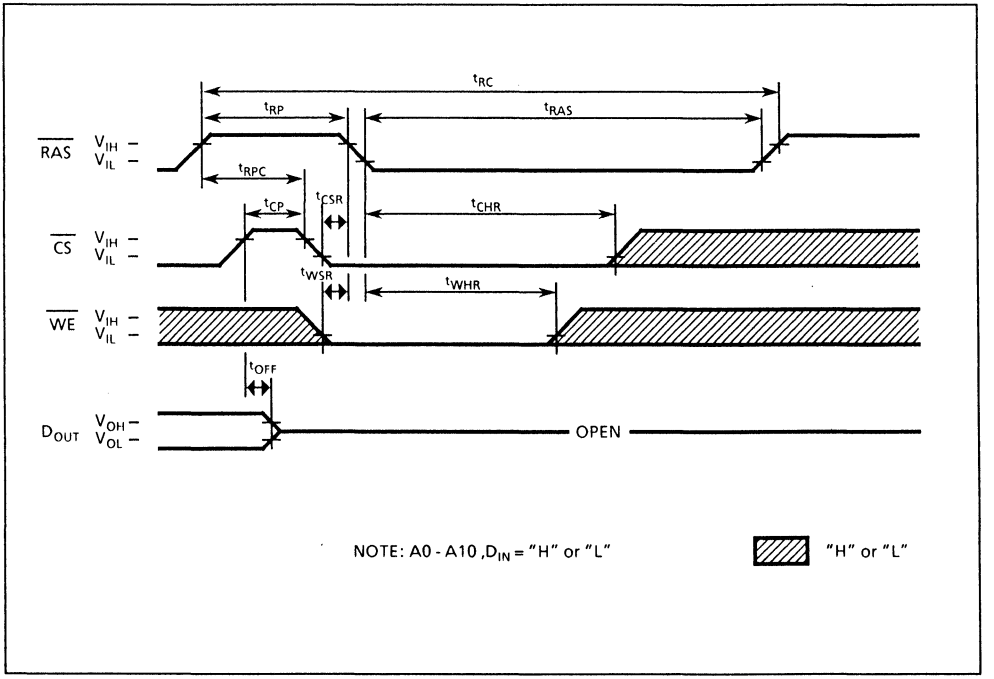
HIDDEN REFRESH READ CYCLE



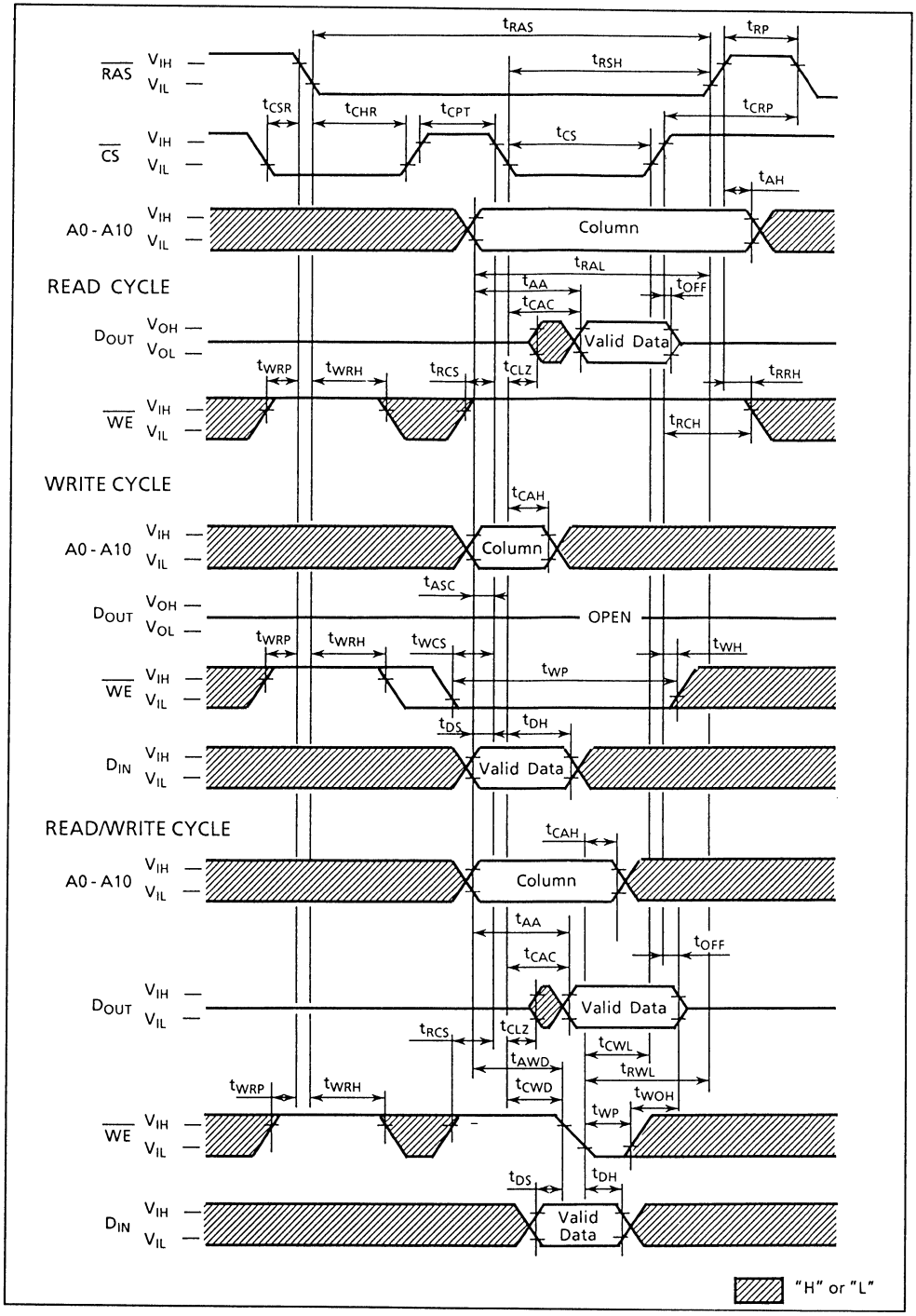
HIDDEN REFRESH WRITE CYCLE



TEST MODE INITIATE CYCLE



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



OKI semiconductor
MSM514400

1,048,576-WORD x 4-BIT DYNAMIC RAM: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The MSM514400 is a new generation dynamic RAM organized as 1,048,576 words by 4 bits. The technology used to fabricate the MSM514400 is OKI's CMOS silicon gate process technology. The device operates at a single + 5 V power supply. Its I/O pins are TTL compatible.

4

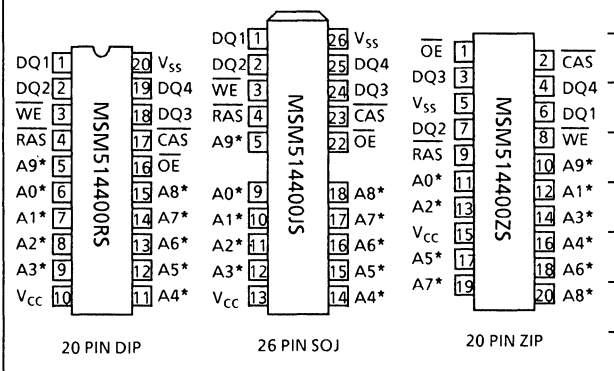
FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1 transistor memory cell
- 1,048,576 word by 4 bit organization
- 350 mil 26-pin plastic SOJ, 400 mil 20-pin plastic ZIP, 400 mil 20-pin plastic DIP
- Family organization

Family	Access Time (MAX)				Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (MAX)	Standby (MAX)
MSM514400-8	80 ns	40 ns	20 ns	20 ns	160 ns	495 mW	5.5 mW (MOS level)
MSM514400-8A	80 ns	40 ns	25 ns	25 ns	160 ns	495 mW	
MSM514400-10	100 ns	50 ns	25 ns	25 ns	190 ns	440 mW	

- Single + 5 V supply, ± 10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Multi bit test mode capability
- Built-in V_{BB} generator circuit

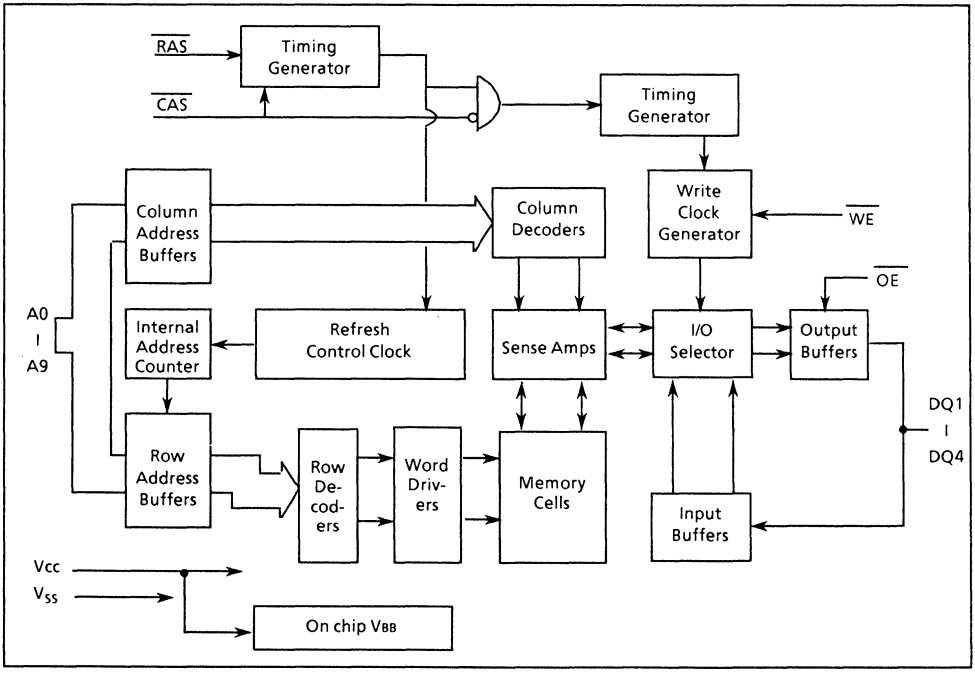
PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
A0 to A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
DQ1 to DQ4	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply < + 5V >
V_{SS}	Ground <0V>

* Refresh Address

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit	Note
Voltage on any pin relative to V_{SS}	VT	Ta = 25 °C	− 1.0 to + 7.0	V	1
Short circuit output current	Ios	Ta = 25 °C	50	mA	1
Power dissipation	P_D	Ta = 25 °C	1	W	1
Operating temperature	Topr	−	0 to + 70	°C	1
Storage temperature	Tstg	−	− 55 to + 150	°C	1

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to + 70°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	2
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	−	6.5	V	2
Input low voltage	V_{IL}	− 1.0	−	0.8	V	2

Notes: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 514400-8		MSM 514400-8A		MSM 514400-10		Unit	Note
			MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0V ≤ VI ≤ 6.5V; all other pins not under test = 0V	−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	DQ_i = disable 0V ≤ VO ≤ 5.5 V	−10	10	−10	10	−10	10	μA	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ cycling, t_{RC} = min	−	90	−	90	−	80	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IH}, DQ_i = Hz — TTL	−	2	−	2	−	2	mA	
		MOS	−	1	−	1	−	1	mA	
Average power supply current (RAS only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = min	−	90	−	90	−	80	mA	1, 2
Power supply current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, DQ_i = enable	−	5	−	5	−	5	mA	1
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before RAS	−	90	−	90	−	80	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min	−	80	−	80	−	70	mA	1, 3

Notes: 1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A9)	C_{IN1}	−	−	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	−	−	7	pF
Output capacitance (DQ1 to DQ4)	$C_{I/O}$	−	−	7	pF

AC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to +70°C) Note 1, 2, 3, 10, 11

Parameter	Symbol	MSM 514400-8		MSM 514400-8A		MSM 514400-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	160	–	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	215	–	220	–	255	–	ns	
Fast page mode cycle time	t_{PC}	55	–	55	–	65	–	ns	
Fast page mode read/write cycle time	t_{PRWC}	110	–	110	–	130	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	80	–	100	ns	4, 5
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	–	25	ns	4. 5
Access time from column address	t_{AA}	–	40	–	40	–	50	ns	4. 6
Access time from $\overline{OE}$	t_{OEA}	–	20	–	25	–	25	ns	
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	45	–	45	–	55	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	0	–	ns	
Output buffer turn-off delay time	t_{OFF}	0	20	0	20	0	25	ns	7
$\overline{OE}$ to data output buffer turn-off delay time	t_{OEZ}	0	20	0	20	0	25	ns	7
Transition time	t_T	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	–	16	–	16	–	16	ms	
$\overline{RAS}$ precharge time	t_{RP}	70	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	25	–	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	20	–	25	–	25	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	80	–	100	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	55	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	40	20	50	ns	6
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	40	–	50	–	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSM 514400-8		MSM 514400-8A		MSM 514400-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	8
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	9
Write command hold time	t_{WCH}	15	–	15	–	20	–	ns	
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	60	–	75	–	ns	
$\overline{OE}$ command hold time	t_{OEH}	20	–	25	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	25	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	60	–	75	–	ns	
$\overline{OE}$ to Data-in delay time	t_{OED}	20	–	20	–	25	–	ns	
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	50	–	55	–	60	–	ns	9
Column address to $\overline{WE}$ delay time	t_{AWD}	70	–	70	–	85	–	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	110	–	110	–	135	–	ns	9
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	20	–	20	–	20	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	20	–	20	–	20	–	ns	
$\overline{RAS}$ to $\overline{WE}$ set-up time (Test mode)	t_{WSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{WE}$ hold time (Test mode)	t_{WHR}	20	–	20	–	20	–	ns	

Notes: 1. An initial pause of 200 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is achieved.
In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles is required.

2. The AC characteristics assume $t_T = 5$ ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2TTL loads and 100pF.

5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

7. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

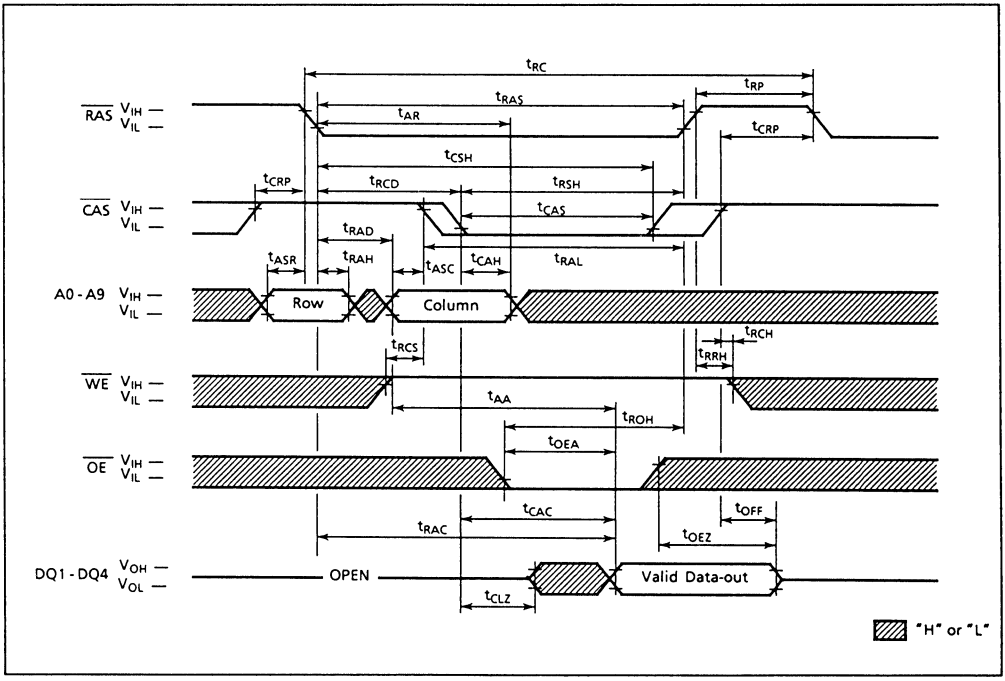
8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

9. t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

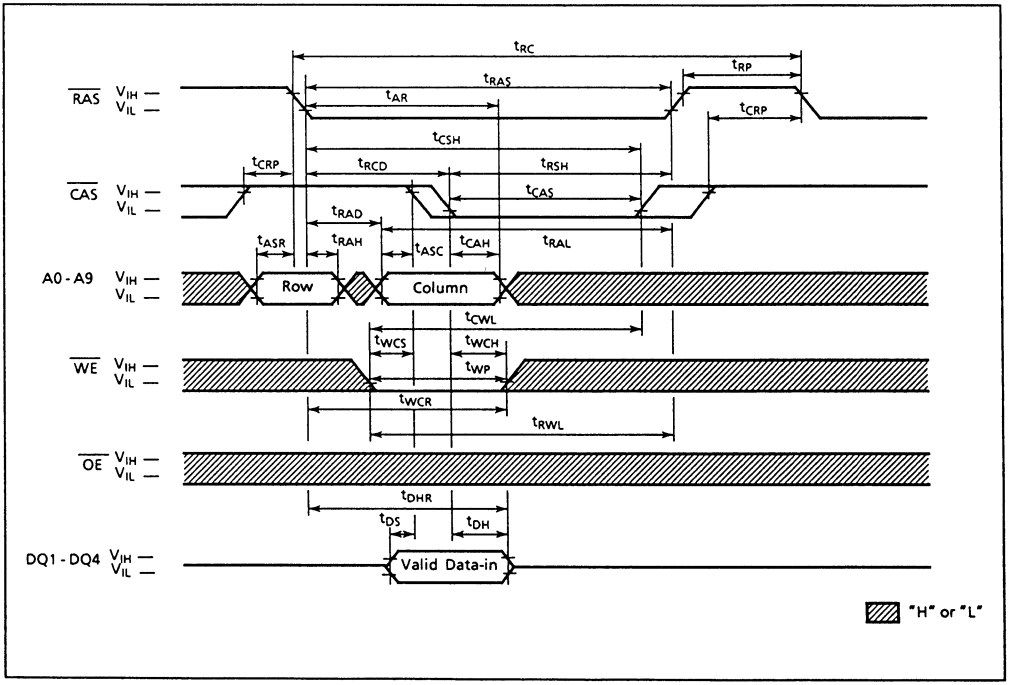
10. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remain in effect until the exit cycle is generated.
The test mode specified in this data sheet is 8-bit parallel test function.
CA0 is not used. In a read cycle, if two internal bits on one I/O pin are equal, the I/O pin will indicate a high level. If internal bits on one I/O pin are not equal, then the I/O pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

11. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

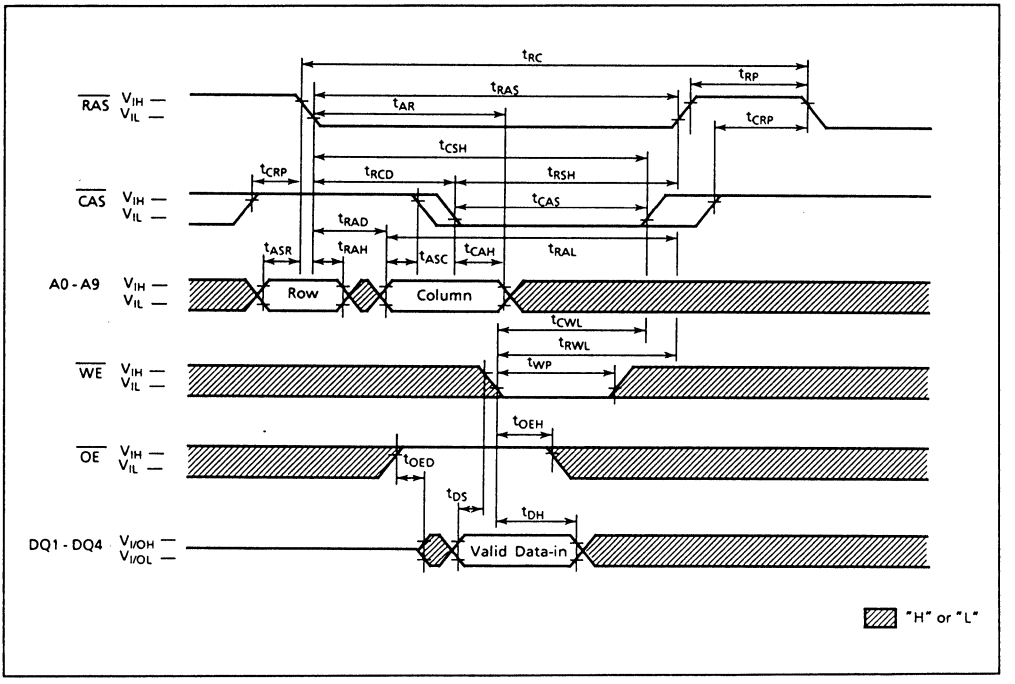
READ CYCLE



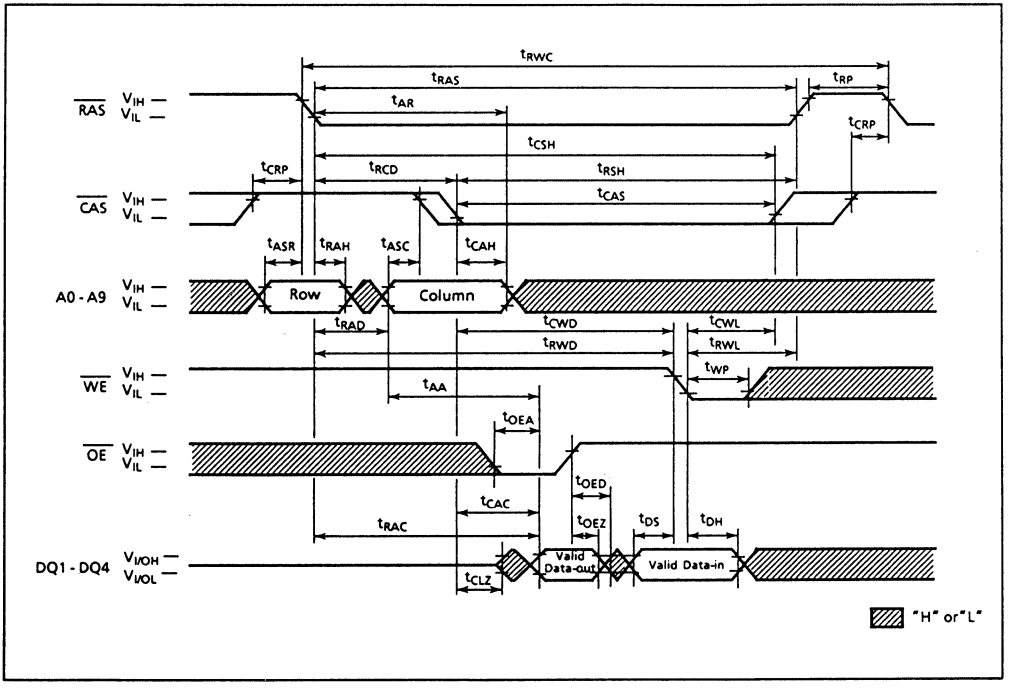
WRITE CYCLE (EARLY WRITE)



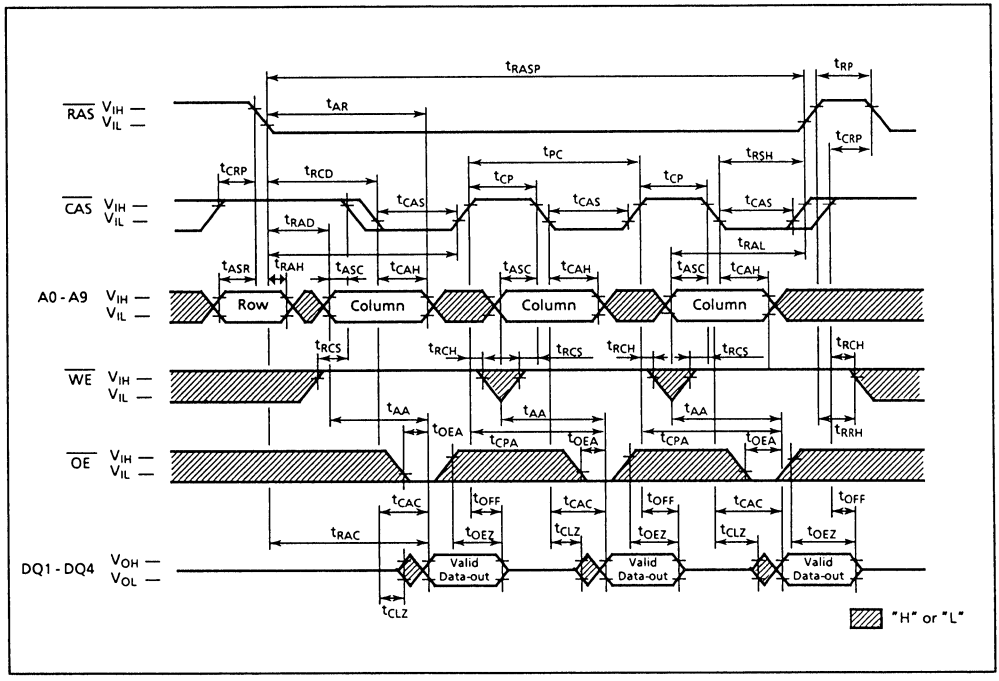
WRTIE CYCLE ($\overline{OE}$ CONTROL WRITE)



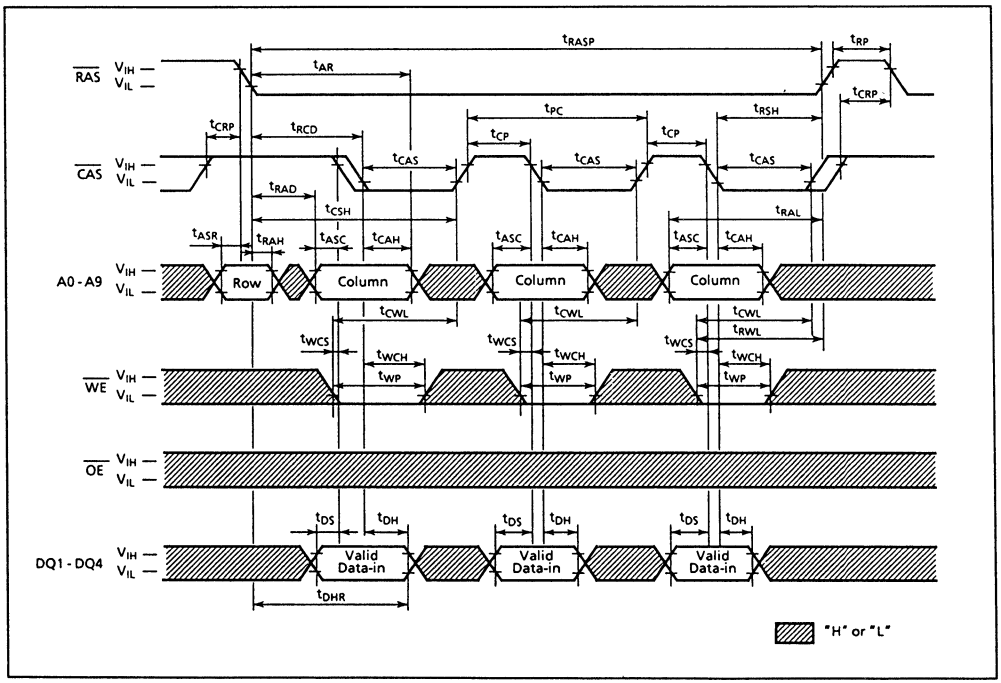
READ/WRTIE CYCLE



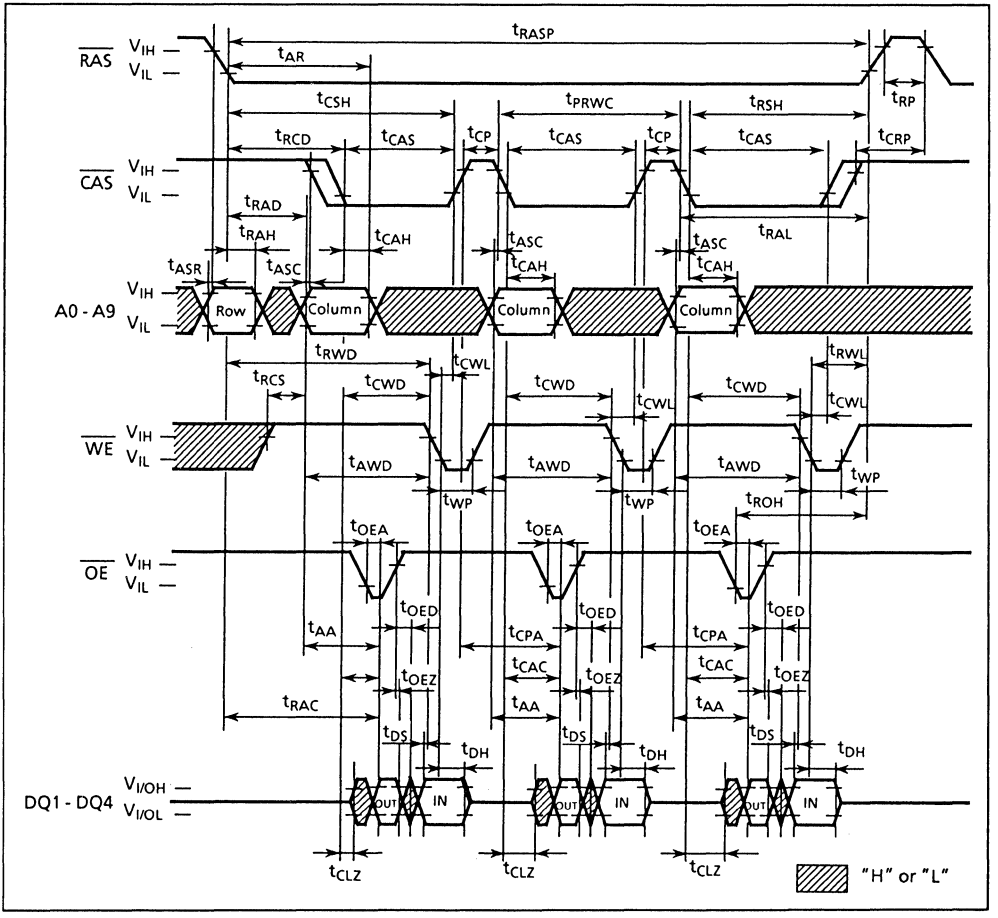
FAST PAGE MODE READ CYCLE



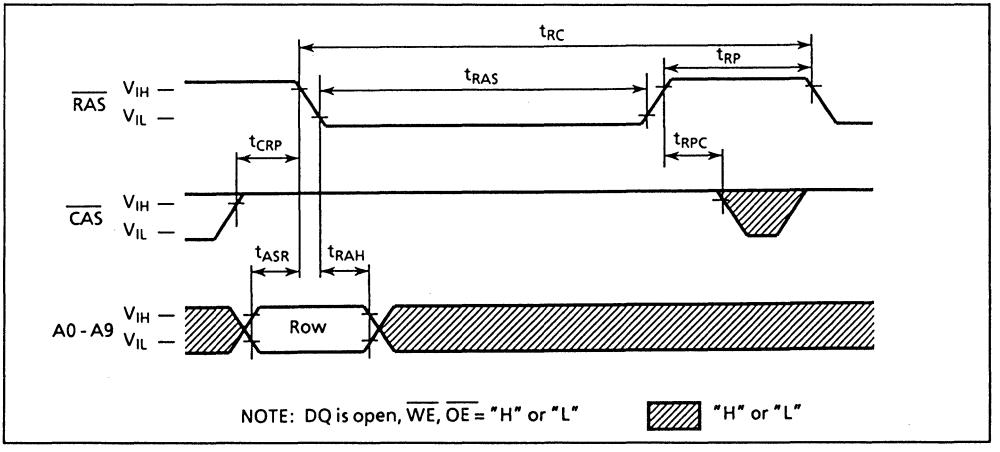
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



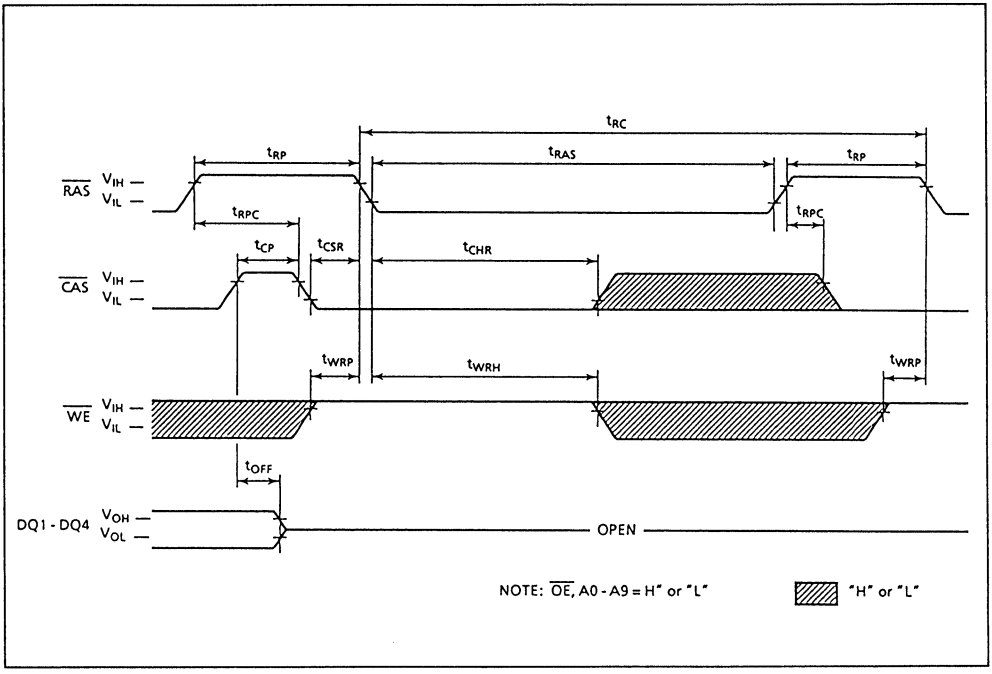
FAST PAGE MODE READ/WRITE CYCLE



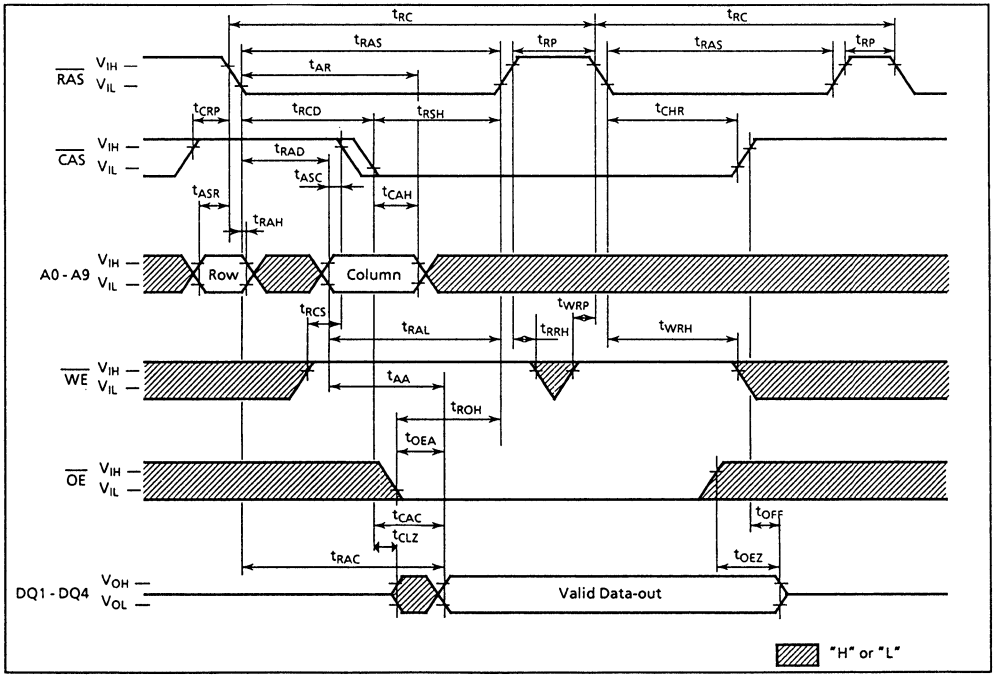
RAS ONLY REFRESH CYCLE



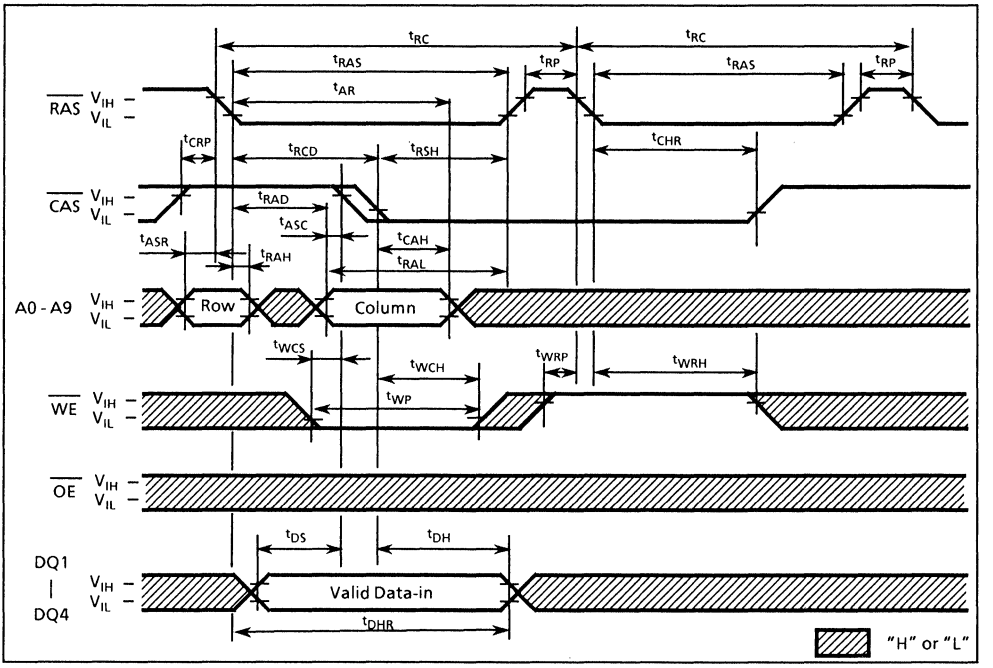
$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



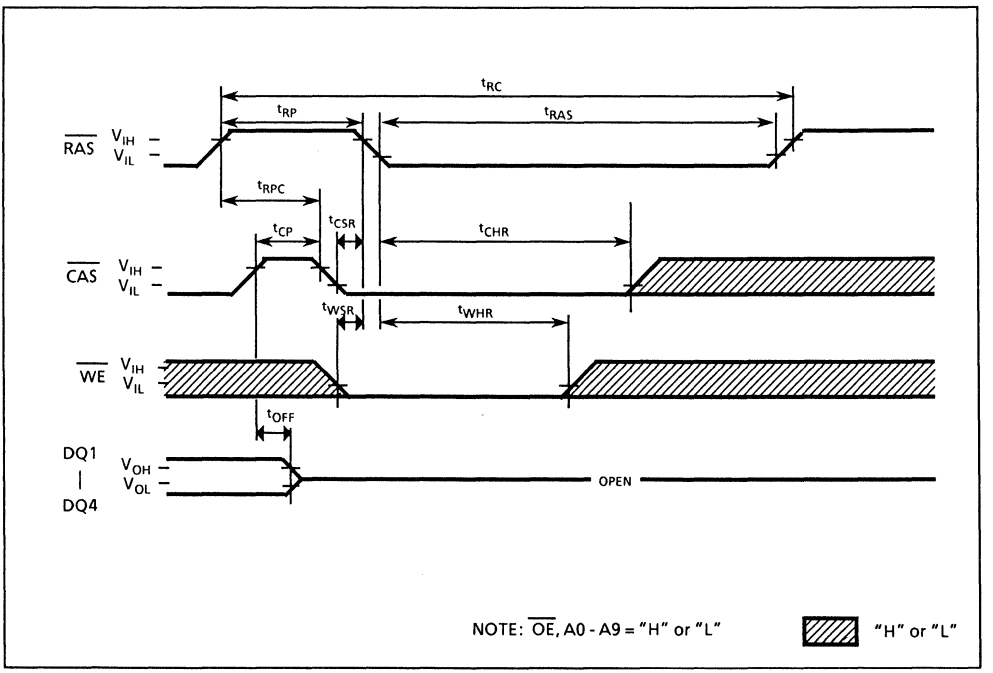
HIDDEN REFRESH READ CYCLE



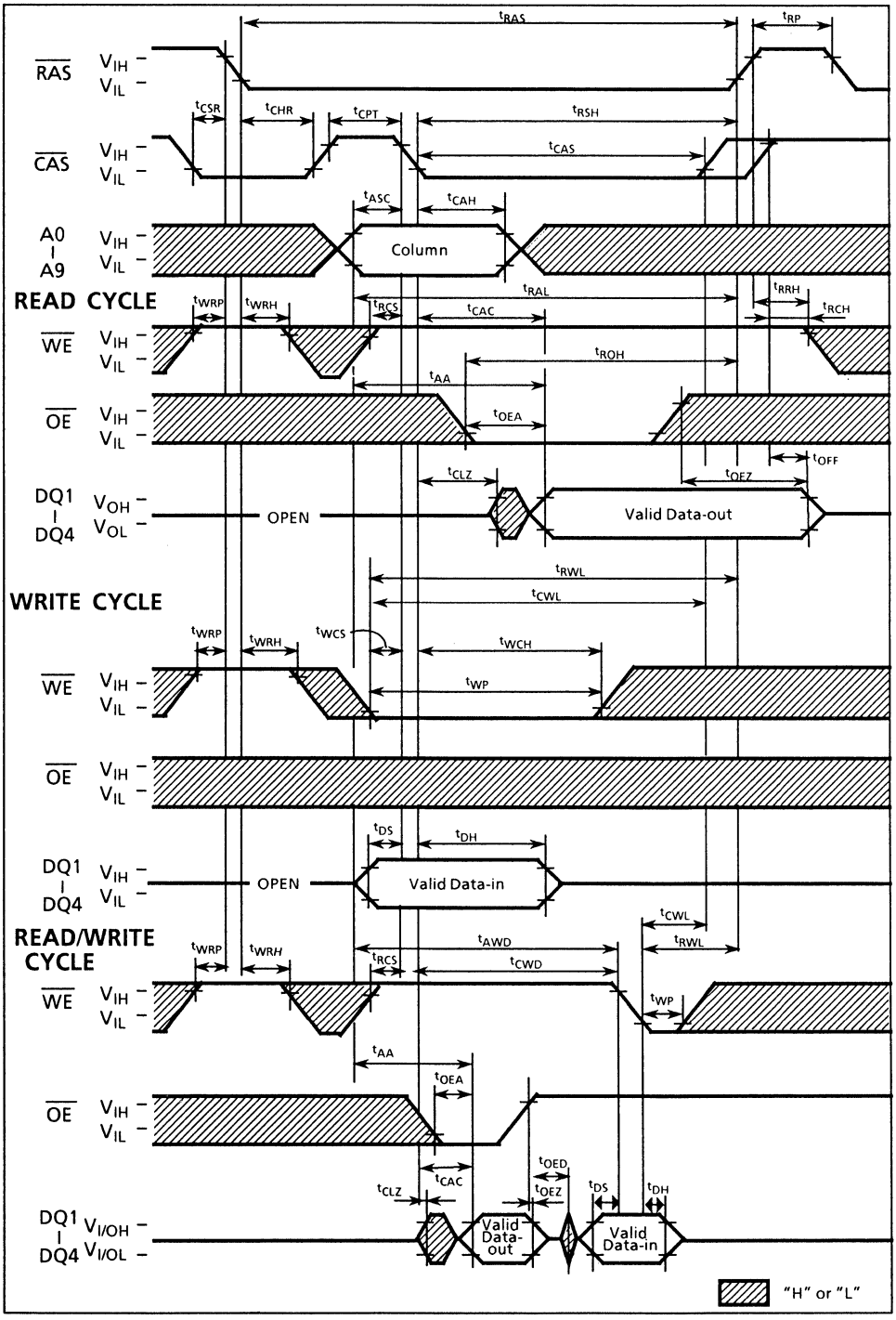
HIDDEN REFRESH WRITE CYCLE



TEST MODE INITIATE CYCLE



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



OKI semiconductor
MSM514402

1,048,576-WORD × 4-BIT DYNAMIC RAM: STATIC COLUMN MODE TYPE

GENERAL DESCRIPTION

The MSM514402 is a new generation dynamic RAM organized as 1,048,576 words by 4 bits. The technology used to fabricate the MSM514402 is OKI's CMOS silicon gate process technology. The device operates at a single + 5 V power supply. Its I/O pins are TTL compatible.

4

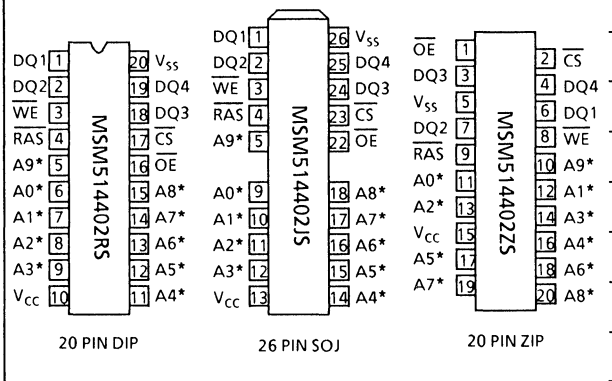
FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1-transistor memory cell
- 1,048,576 word by 4 bit organization
- 350 mil 26-pin plastic SOJ, 400 mil 20-pin plastic ZIP, 400 mil 20-pin plastic DIP
- Family organization

Family	Access Time (MAX)				Cycle Time (MIN)	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	t_{OEA}		Operating (MAX)	Standby (MAX)
MSM514402-8	80 ns	40 ns	20 ns	20 ns	160 ns	495 mW	5.5 mW (MOS level)
MSM514402-8A	80 ns	40 ns	25 ns	25 ns	160 ns	495 mW	
MSM514402-10	100 ns	50 ns	25 ns	25 ns	190 ns	440 mW	

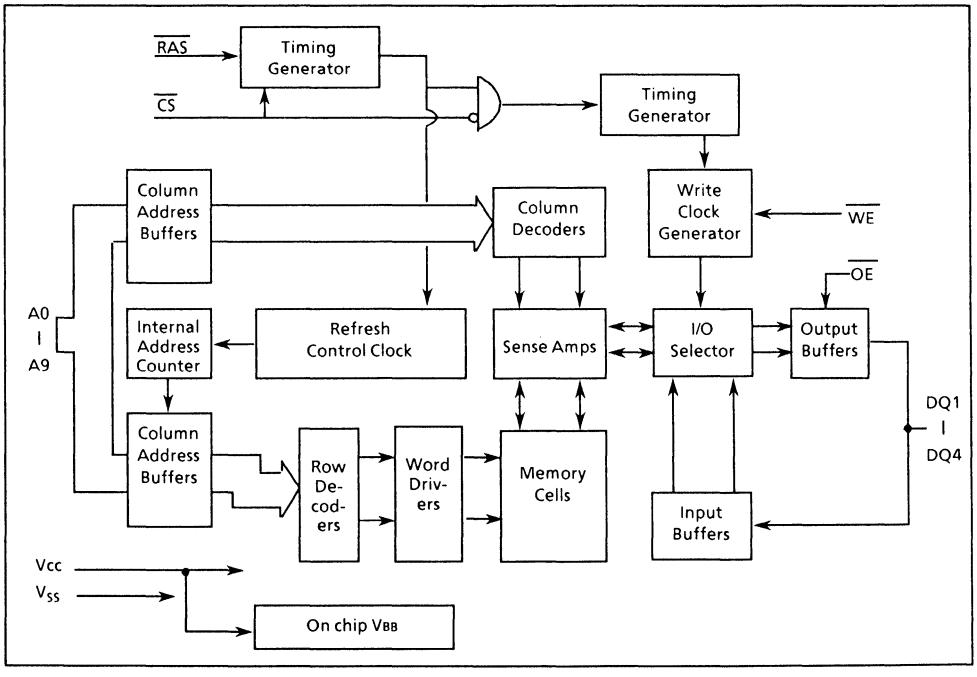
- Single + 5 V supply, ± 10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{CS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Multi bit test mode capability
- Built-in V_{BB} generator circuit

PIN CONFIGURATION (TOP VIEW)



Pin Names	Function
A0 to A9	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
DQ1 to DQ4	Data In / Data Out
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply < +5V >
V_{SS}	Ground < 0V >

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit	Note
Voltage on any pin relative to V_{SS}	VT	Ta = 25 °C	− 1.0 to + 7.0	V	1
Short circuit output current	Ios	Ta = 25 °C	50	mA	1
Power dissipation	P_D	Ta = 25 °C	1	W	1
Operating temperature	Topr	−	0 to + 70	°C	1
Storage temperature	Tstg	−	− 55 to + 150	°C	1

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to + 70°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	2
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	−	6.5	V	2
Input low voltage	V_{IL}	− 1.0	−	0.8	V	2

Notes: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions	MSM 514402-8		MSM 514402-8A		MSM 514402-10		Unit	Note
			MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA	0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0 V ≤ VI ≤ 6.5V; all other pins not under test = 0 V	−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	DQ_i = disable 0 V ≤ VO ≤ 5.5 V	−10	10	−10	10	−10	10	μA	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ cycling, t_{RC} = min	−	90	−	90	−	80	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IH}, DQ_i = Hz — TTL	−	2	−	2	−	2	mA	
		MOS	−	1	−	1	−	1	mA	
Average power supply current (RAS only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CS}$ = V_{IH}, t_{RC} = min	−	90	−	90	−	80	mA	1, 2
Power supply current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH}, $\overline{CS}$ = V_{IL}, DQ_i = enable	−	5	−	5	−	5	mA	1
Average power supply current ($\overline{CS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CS}$ before $\overline{RAS}$	−	90	−	90	−	80	mA	1
Average power supply current (Static Column mode)	I_{CC9}	$\overline{RAS}$ = V_{IL}, $\overline{CS}$ = V_{IL}, t_{SC} = min	−	80	−	80	−	70	mA	1

Notes: 1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A9)	C_{IN1}	−	−	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$)	C_{IN2}	−	−	7	pF
Output capacitance (DQ1 to DQ4)	$C_{I/O}$	−	−	7	pF

AC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to +70°C) Note 1, 2, 3, 11, 12

Parameter	Symbol	MSM 514402-8		MSM 514402-8A		MSM 514402-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	160	–	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	215	–	220	–	255	–	ns	
Static column mode cycle time	t_{SC}	45	–	45	–	55	–	ns	
Static column mode read/write cycle time	t_{SRWC}	100	–	100	–	115	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	80	–	100	ns	4.5,6
Access time from $\overline{CS}$	t_{CAC}	–	20	–	25	–	25	ns	4. 5
Access time from column address	t_{AA}	–	40	–	40	–	50	ns	4.6,7
Access time from last write	t_{ALW}	–	75	–	75	–	95	ns	4,7
Access time from $\overline{OE}$	t_{OEA}	–	20	–	25	–	25	ns	
Data output enable time reference to $\overline{WE}$	t_{OW}	–	20	–	25	–	25	ns	
Output low impedance time from $\overline{CS}$	t_{CLZ}	0	–	0	–	0	–	ns	4
Data output hold time reference to column address	t_{AOH}	5	–	5	–	5	–	ns	
Output buffer turn-off delay time	t_{OFF}	0	20	0	20	0	25	ns	8
$\overline{OE}$ to data output buffer turn-off delay time	t_{OEZ}	0	20	0	20	0	25	ns	8
Transition time	t_T	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	–	16	–	16	–	16	ms	
$\overline{RAS}$ precharge time	t_{RP}	70	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	80	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	25	–	ns	
$\overline{RAS}$ hold time reference to $\overline{OE}$	t_{ROH}	20	–	25	–	25	–	ns	
$\overline{CS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{CS}$ pulse width	t_{CS}	20	100,000	25	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	80	–	80	–	100	–	ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	22	60	25	55	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	40	20	50	ns	6
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	20	–	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSM 514402-8		MSM 514402-8A		MSM 514402-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Column address hold time reference to $\overline{RAS}$ (WRITE CYCLE)	t_{AWR}	60	–	60	–	75	–	ns	
Column address hold time reference to $\overline{RAS}$	t_{AR}	95	–	95	–	115	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	40	–	50	–	ns	
Column address hold time reference to $\overline{RAS}$ precharge	t_{AH}	10	–	10	–	10	–	ns	
Column address hold time reference to $\overline{WE}$	t_{AHLW}	75	–	75	–	95	–	ns	
Last write to column address delay time	t_{LWAD}	20	35	20	35	25	45	ns	7
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	9
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	10
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
$\overline{OE}$ command hold time	t_{OEH}	20	–	25	–	25	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	60	–	75	–	ns	
Write invalid time	t_{WI}	10	–	10	–	10	–	ns	
Write command hold time (D_{OUT} disable)	t_{WH}	0	–	0	–	0	–	ns	10
Write command to $\overline{CS}$ lead time	t_{CWL}	20	–	25	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	25	–	ns	
$\overline{CS}$ to $\overline{WE}$ delay time	t_{CWD}	50	–	55	–	60	–	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	70	–	70	–	85	–	ns	10
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	110	–	110	–	135	–	ns	10
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	60	–	75	–	ns	
$\overline{OE}$ to Data-in delay time	t_{OED}	20	–	20	–	25	–	ns	
$\overline{CS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CS}$ Set-up time ($\overline{CS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CS}$ hold time ($\overline{CS}$ before $\overline{RAS}$)	t_{CHR}	20	–	20	–	20	–	ns	
$\overline{CS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CS}$ before $\overline{RAS}$)	t_{WRP}	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CS}$ before $\overline{RAS}$)	t_{WRH}	20	–	20	–	20	–	ns	

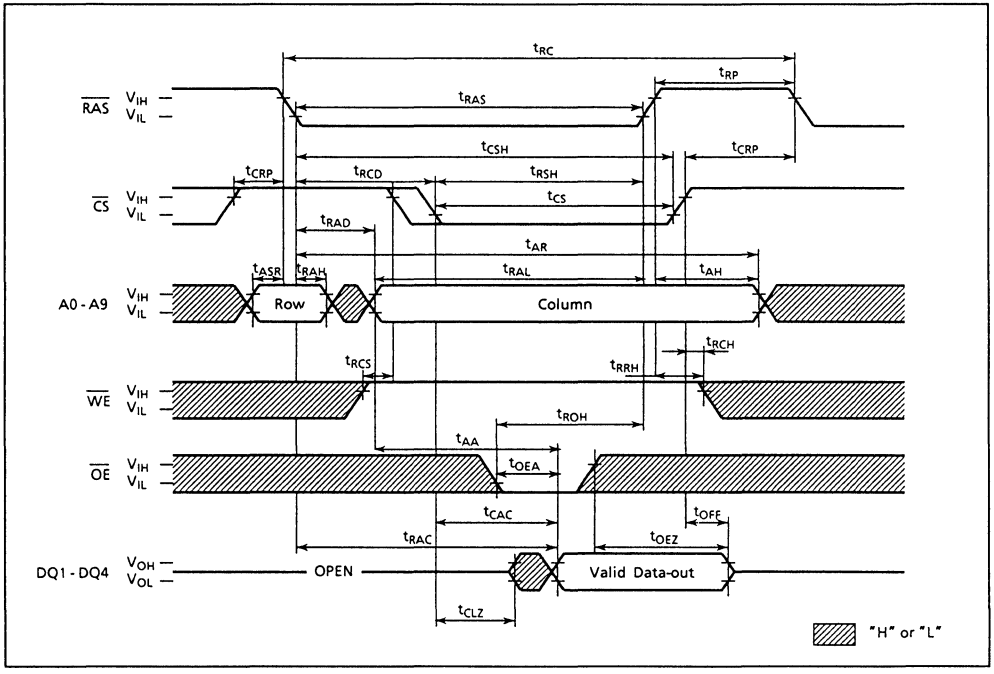
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSM 514402-8		MSM 514402-8A		MSM 514402-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
$\overline{RAS}$ to $\overline{WE}$ set-up time (Test mode)	t_{WSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{WE}$ hold time (Test mode)	t_{WHR}	20	–	20	–	20	–	ns	

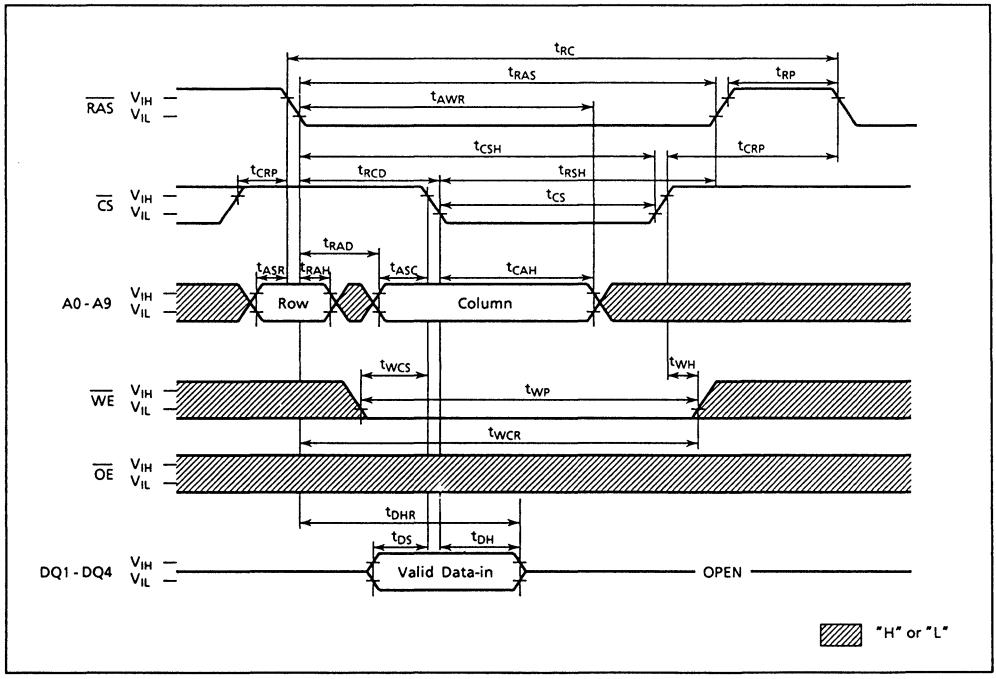
Notes: 1. An initial pause of 200 µs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is achieved.
In case of using internal refresh counter, a minimum of eight $\overline{CS}$ before $\overline{RAS}$ initialization cycles is required.

2. The AC characteristics assume $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL loads and 100pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Operation within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met. t_{LWAD} (max.) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max.) limit, then access time is controlled exclusively by T_{AA}.
8. t_{OFF} (max.) and t_{OEZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
10. t_{WCS}, t_{WH}, t_{CWD} t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) and $t_{WH} \geqq t_{WH}$ (min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
11. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remain in effect until the exit cycle is generated.
The test mode specified in this data sheet is 8-bit parallel test function.
CA0 is not used. In a read cycle, if two internal bits on one I/O pin are equal, the I/O pin will indicate a high level. If internal bits on one I/O pin are not equal, then I/O pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$ only refresh cycle or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle.
12. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

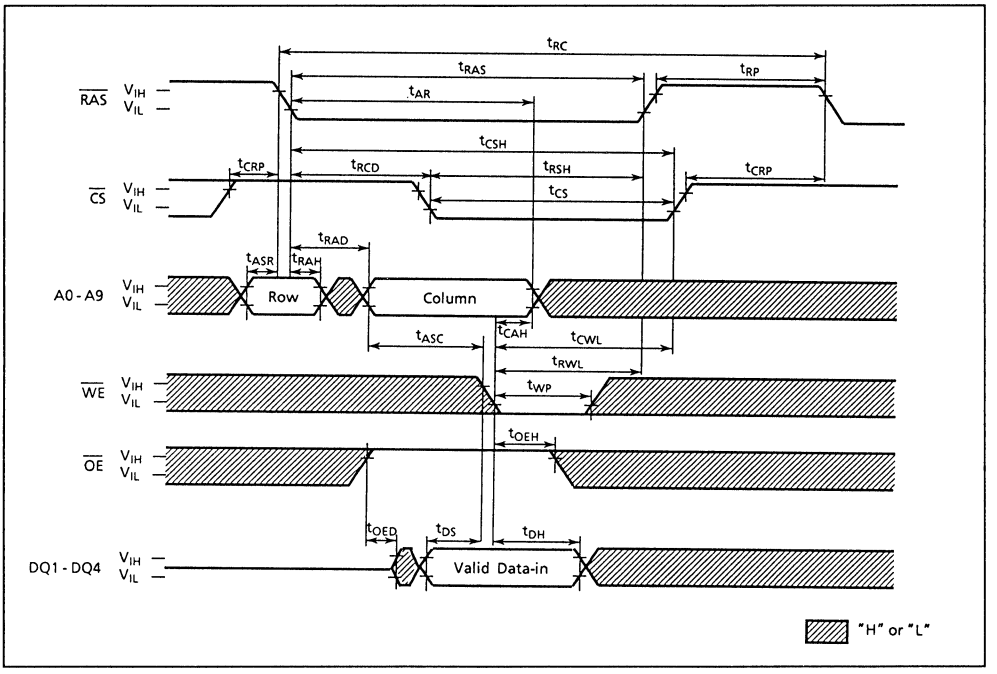
READ CYCLE



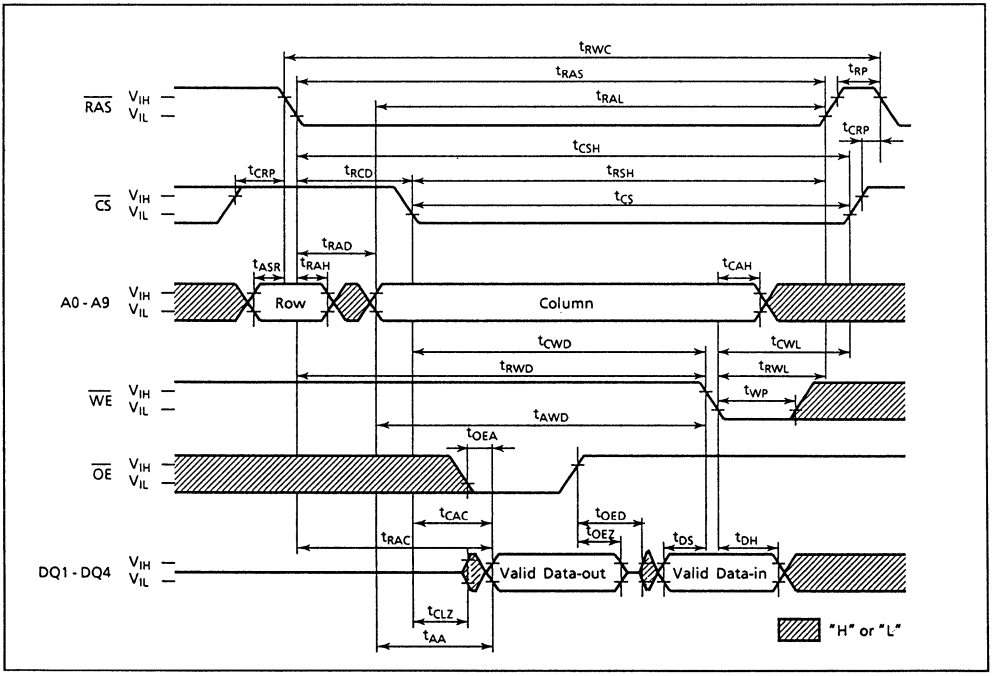
WRITE CYCLE (EARLY WRITE)



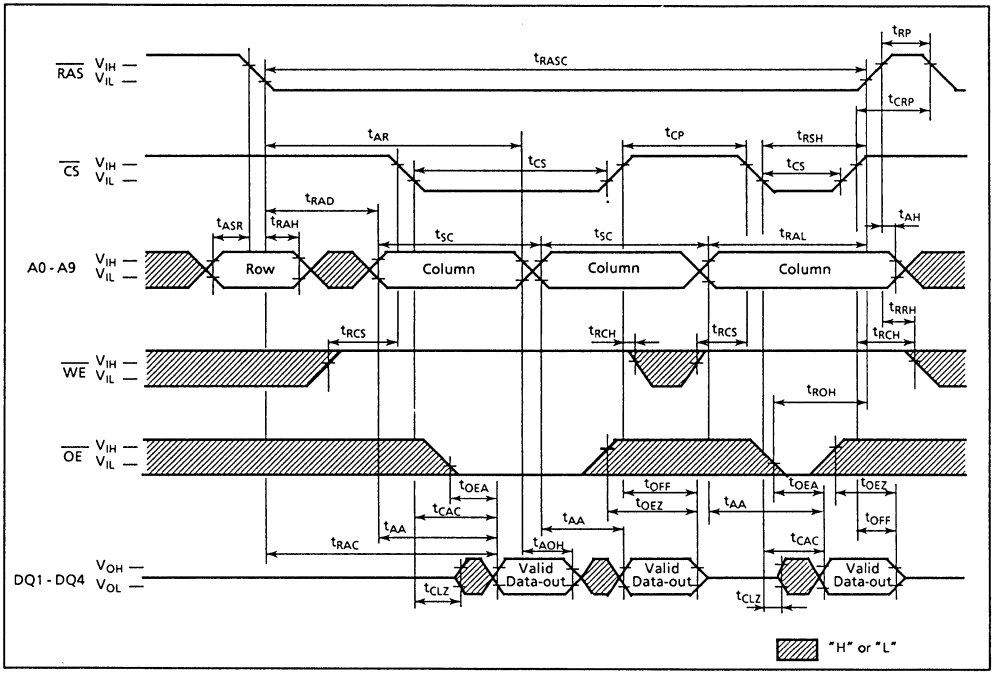
WRITE CYCLE ($\overline{OE}$ CONTROL WRITE)



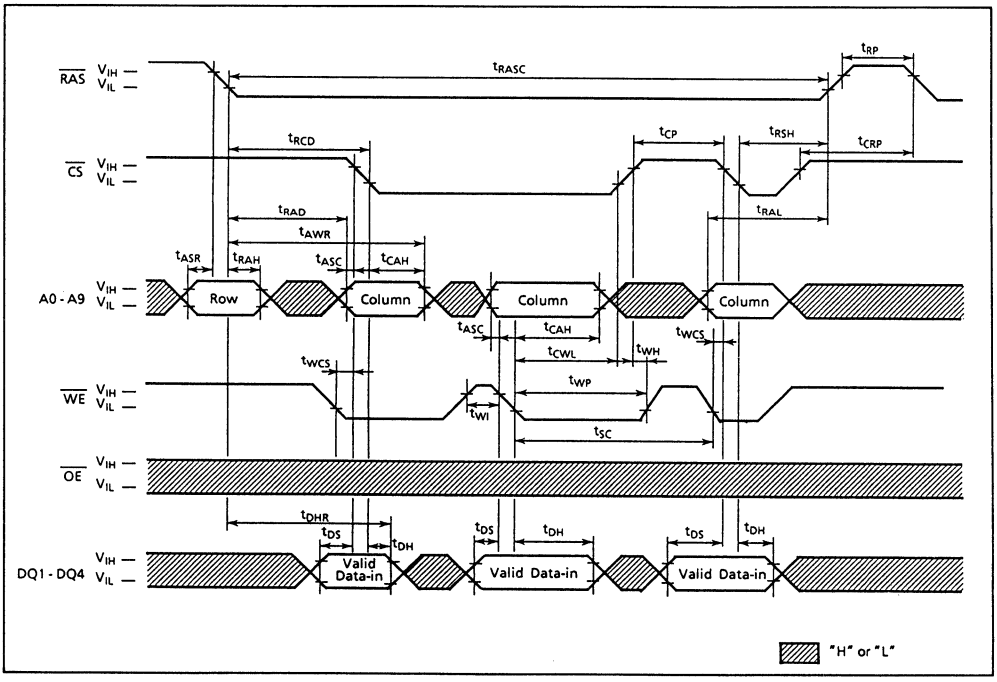
READ/WRITE CYCLE



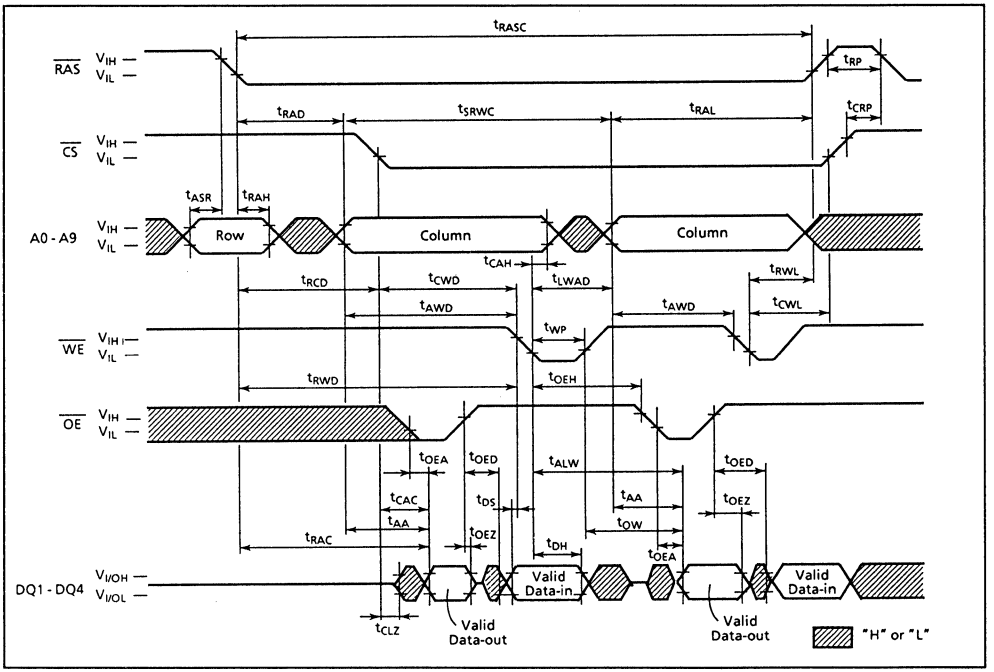
STATIC COLUMN MODE READ CYCLE



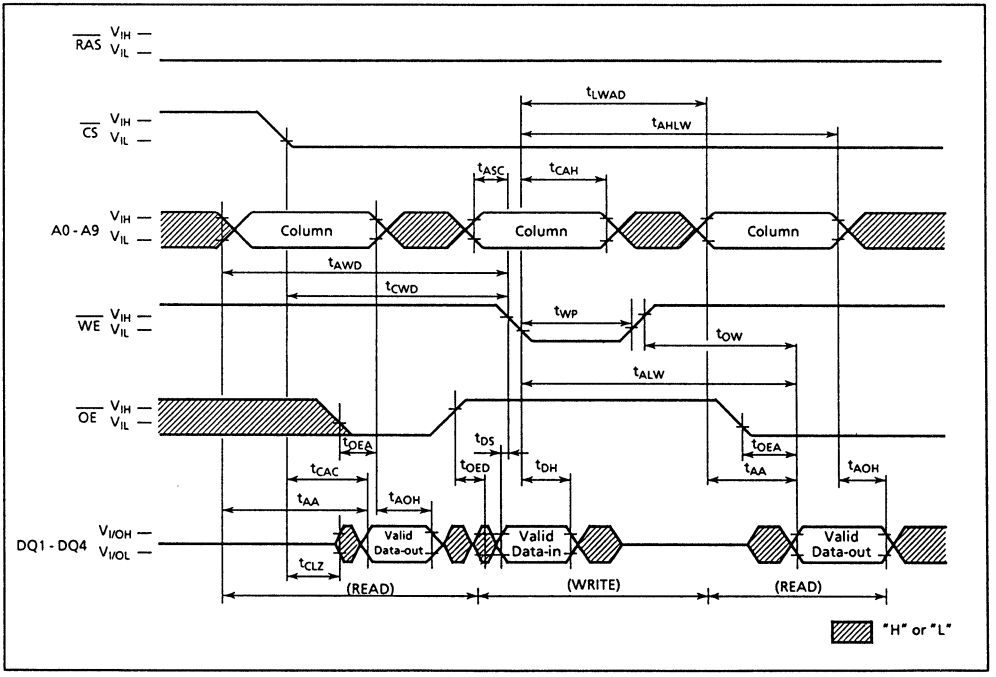
STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)



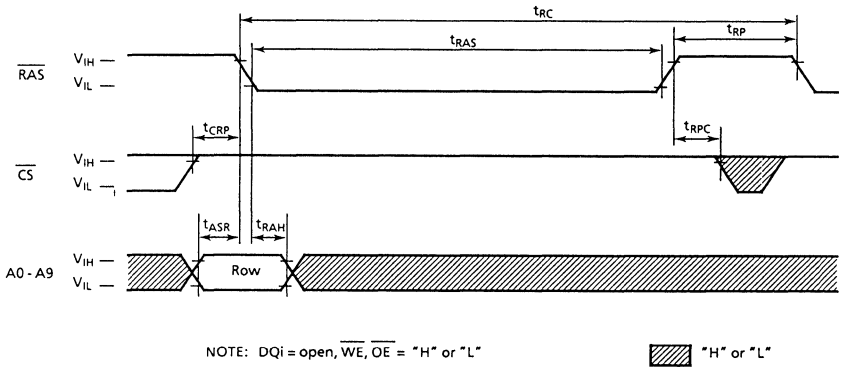
STATIC COLUMN MODE READ/WRITE CYCLE



STATIC COLUMN MODE READ/WRITE MIXED CYCLE



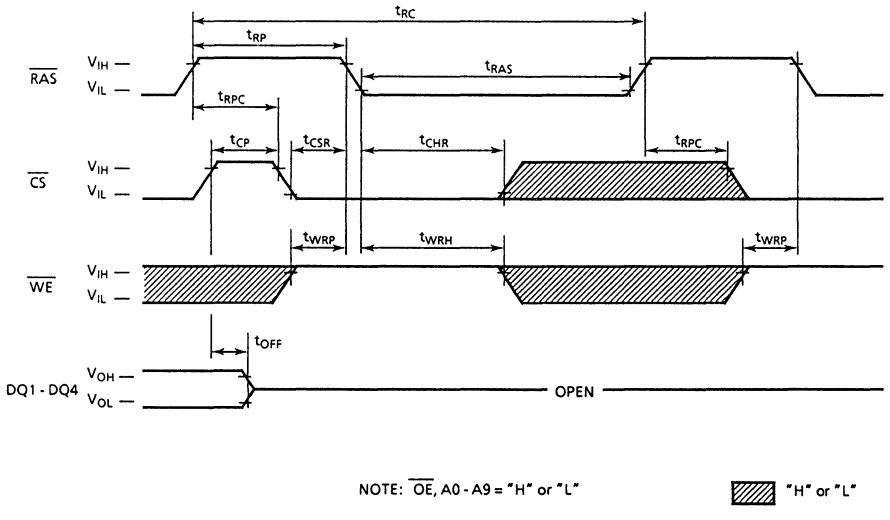
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



NOTE: DQi = open, $\overline{\text{WE}}$, $\overline{\text{OE}}$ = "H" or "L"

"H" or "L"

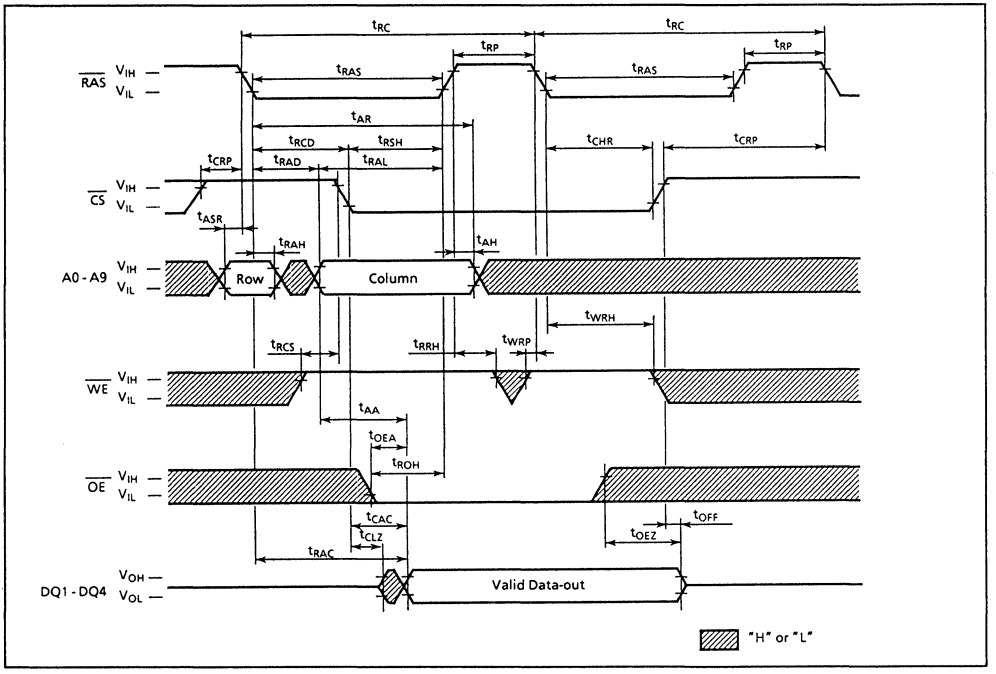
$\overline{\text{CS}}$ BEFORE $\overline{\text{RAS}}$ AUTO REFRESH CYCLE



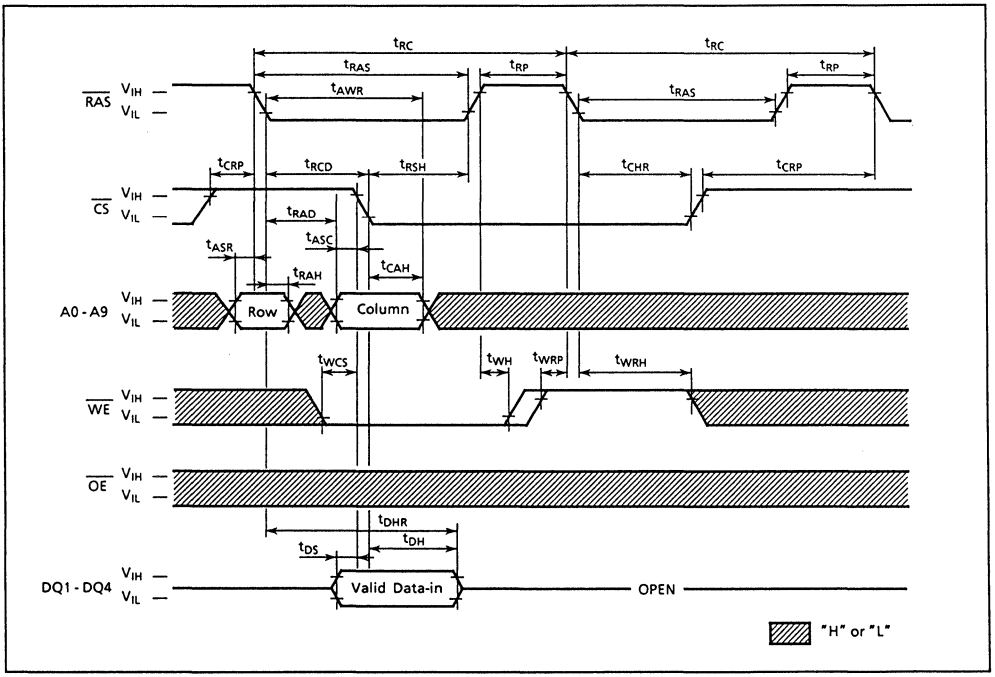
NOTE: $\overline{\text{OE}}$, A0 - A9 = "H" or "L"

"H" or "L"

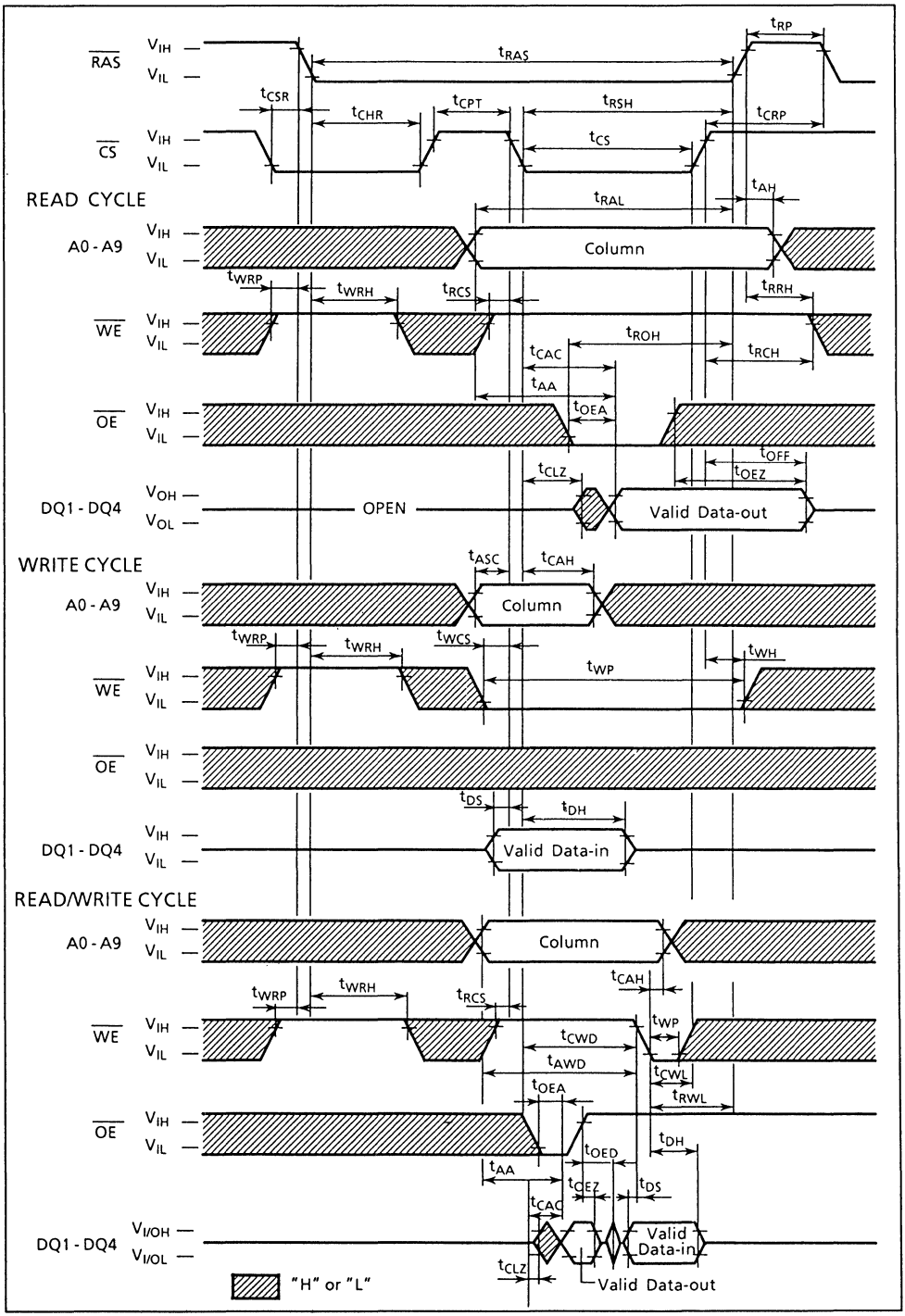
HIDDEN REFRESH READ CYCLE



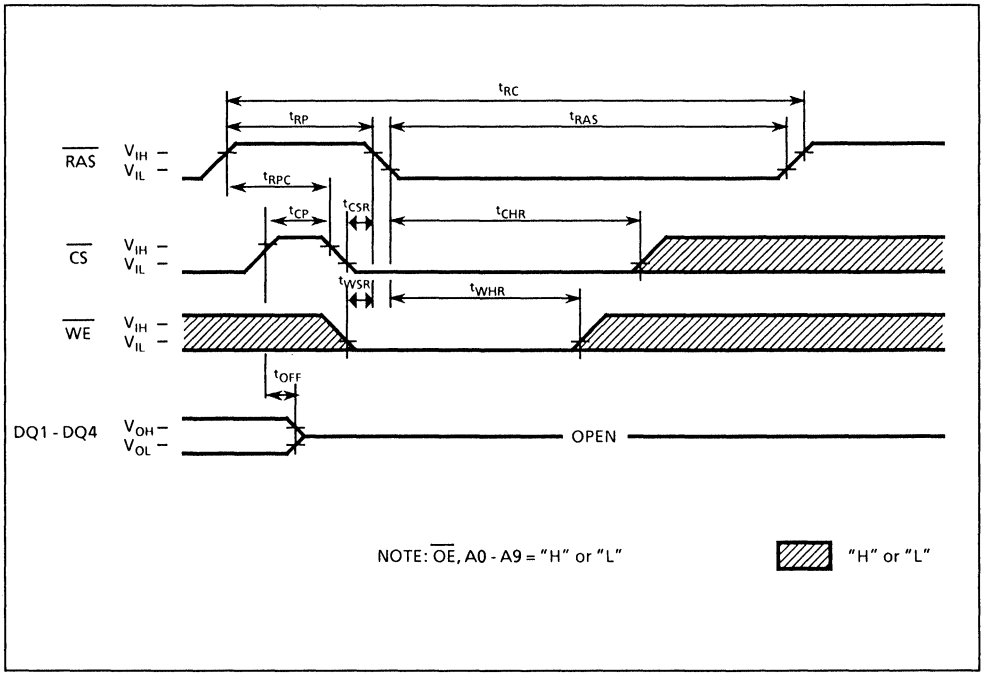
HIDDEN REFRESH WRITE CYCLE



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



TEST MODE INITIATE CYCLE



MSC2304YS8/KS8

262,144 BY 8 BIT DYNAMIC RAM MODULE <Page Mode Type>

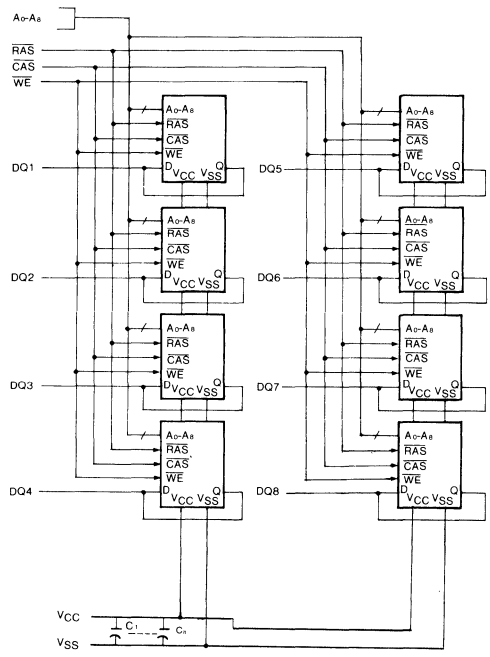
GENERAL DESCRIPTION

The Oki MSC2304YS8/KS8 is a fully decoded, 262,144 words × 8 bit NMOS dynamic random access memory composed of eight 256K DRAMs in plastic leaded chip carrier (MSM41256AJS). The mounting of eight PLCCs together with eight 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2304YS8/KS8 are quite same as the original MSM41256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

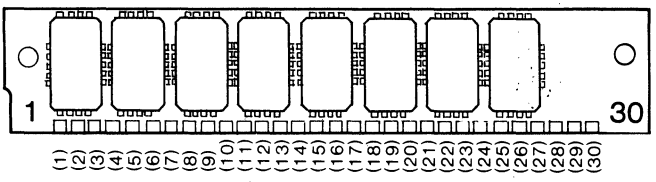
- 262,144 word × 8 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 4ms (256 cycles)
- All Inputs, Outputs, Clocks
  Fully TTL compatible
- 3-States Outputs
- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Row Access Time;
  100ns max. (MSC2304-10YS8/KS8)
  120ns max. (MSC2304-12YS8/KS8)
  150ns max. (MSC2304-15YS8/KS8)
- Low Power Dissipation;
  2640mW max. (MSC2304-10YS8/KS8)
  2420mW max. (MSC2304-12YS8/KS8)
  2200mW max. (MSC2304-15YS8/KS8)
- Operating Temperature ... 0°C to 70°C
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Page Mode" capability

FUNCTIONAL BLOCK DIAGRAM

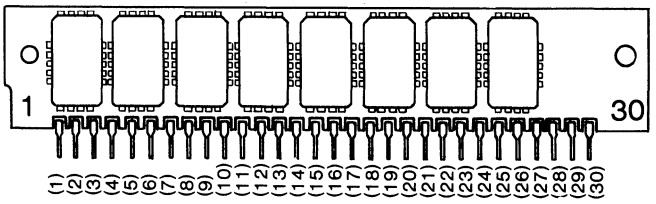


PIN ASSIGNMENT

MSC2304YS8



MSC2304KS8



PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	16	DQ5
2	$\overline{CAS}$	17	A8
3	DQ1	18	NC
4	A0	19	NC
5	A1	20	DQ6
6	DQ2	21	$\overline{WE}$
7	A2	22	VSS
8	A3	23	DQ7
9	VSS	24	NC
10	DQ3	25	DQ8
11	A4	26	NC
12	A5	27	$\overline{RAS}$
13	DQ4	28	NC
14	A6	29	NC
15	A7	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	8	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

4

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	100ns MODULE		120ns MODULE		150ns MODULE		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		480		440		400	mA
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		40		40		40	mA
Refresh Current 1 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		440		400		360	mA
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, CAS cycling; t_{PC} = min.)	I_{CC4}		320		280		240	mA
Refresh Current 2 Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	I_{CC5}		440		400		360	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−80	80	−80	80	−80	80	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_8$)	C_{IN1}	37	60	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	35	65	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF

Capacitance measured with Boonton Meter.

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AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSC2304-10 YS8/KS8		MSC2304-12 YS8/KS8		MSC2304-15 YS8/KS8		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	30	0	30	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		0		
Write command set-up time	t_{WCS}	ns	0		0		0		

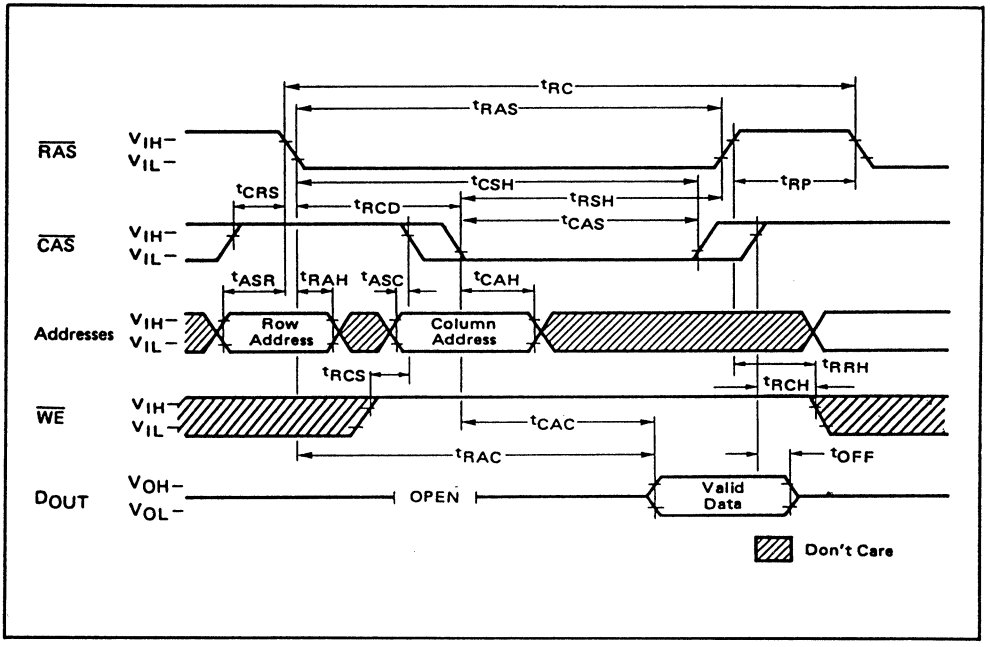
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSC2304-10 YS8/KS8		MSC2304-12 YS8/KS8		MSC2304-15 YS8/KS8		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	15		20		25		
Write command hold time	t_{WCH}	ns	15		20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		20		25		
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		30		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		20		
Page mode cycle time	t_{PC}	ns	100		120		145		8
Page mode $\overline{CAS}$ precharge time	t_{CP}	ns	40		50		60		8

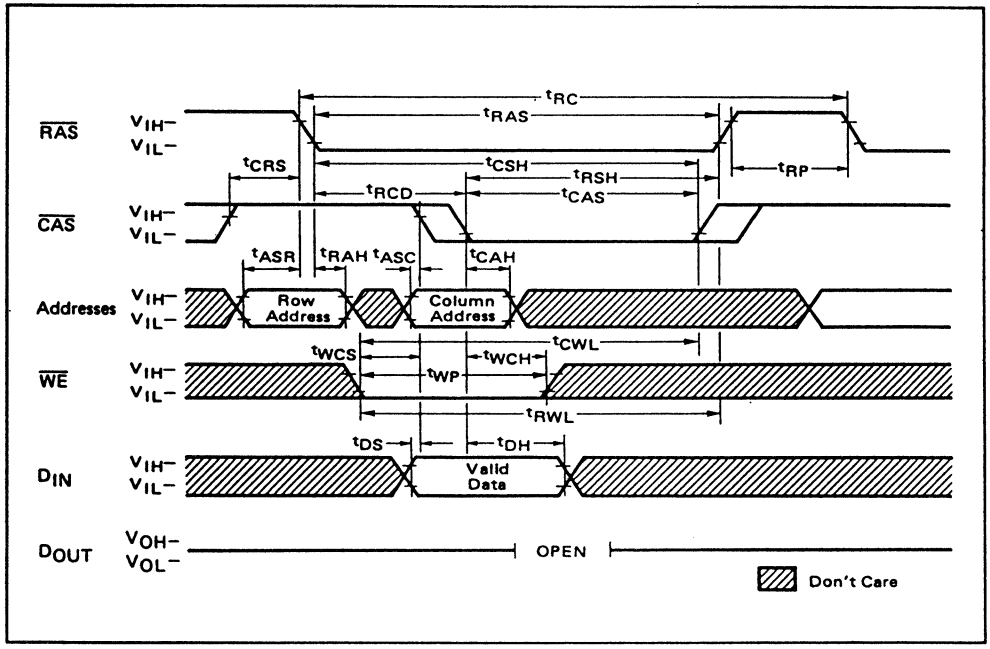
Notes:

1. An initial pause of 100μs is required after power-up followed by any 8 RAS cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC measurements assume $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; If t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Page mode cycle.

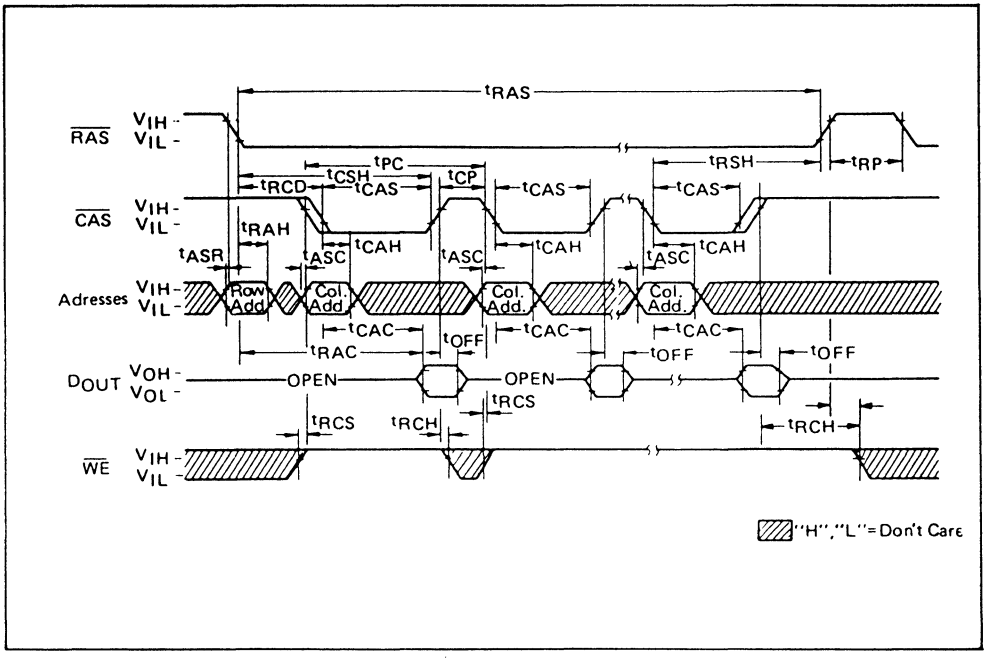
READ CYCLE



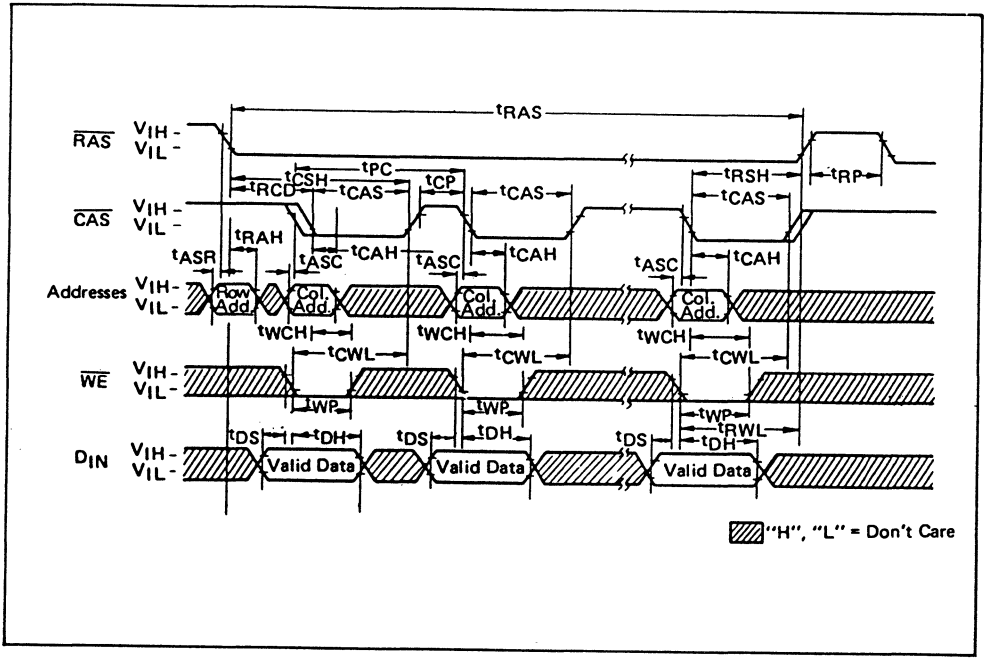
WRITE CYCLE



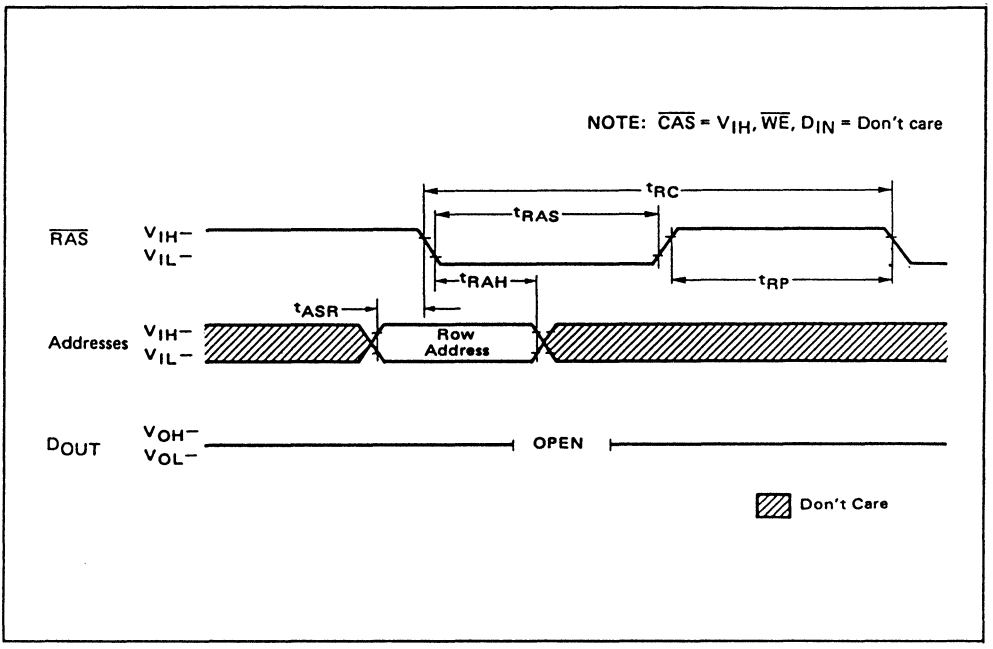
PAGE MODE READ CYCLE



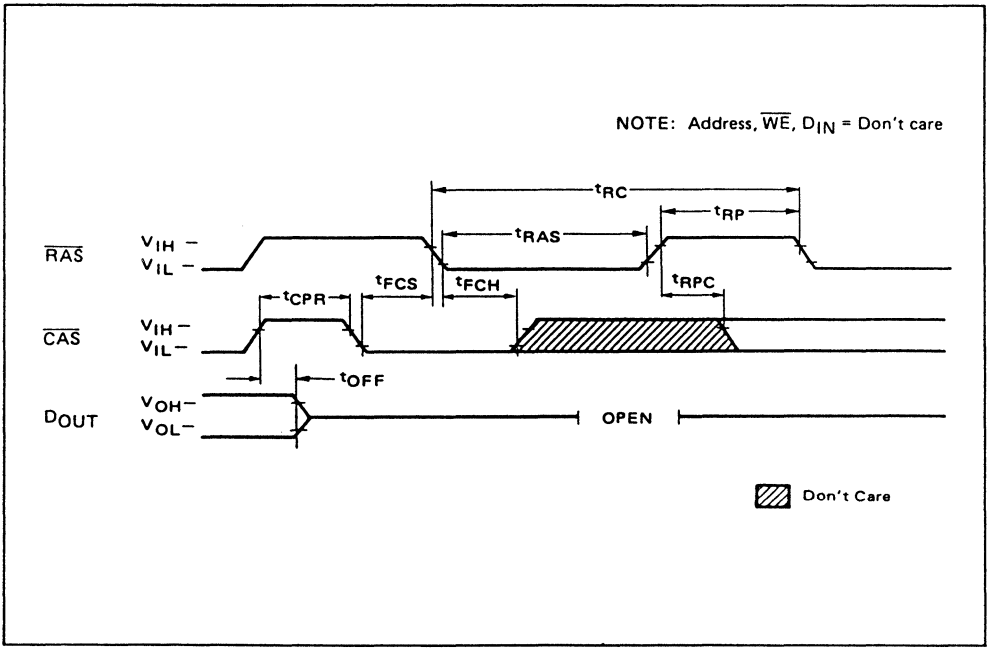
PAGE MODE WRITE CYCLE



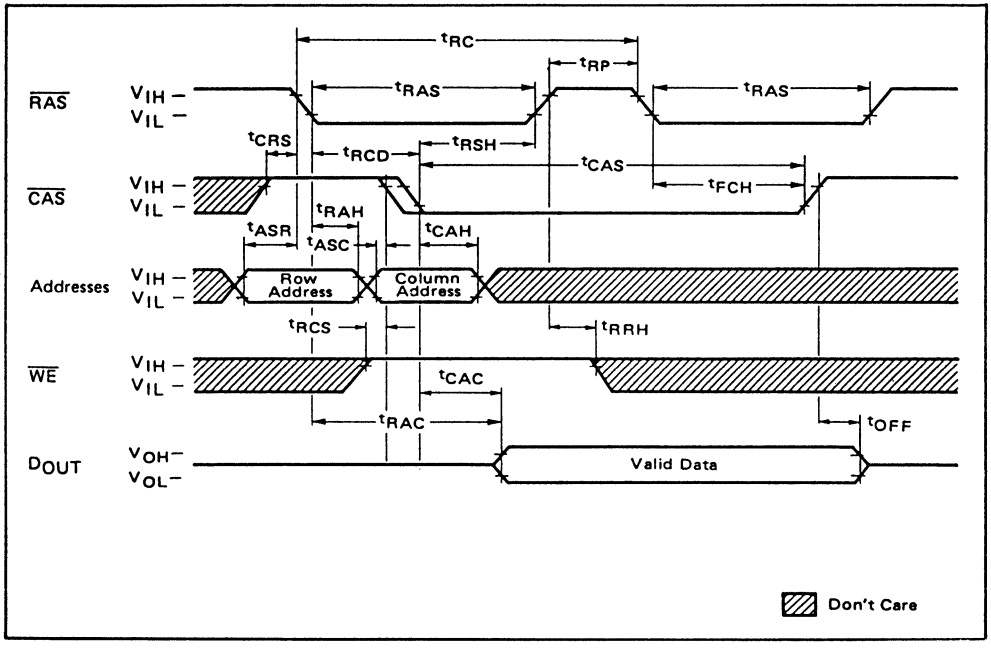
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



FUNCTIONAL DESCRIPTION

Simple Timing Requirements:

The MSC2304 has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSC2304 can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address minimam hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and DIN (t_{DH}). And the MSC2304 can commit better memory system through-put during operations in an interleaved system.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSC2304. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input addresses must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSCA2304 during a write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data In (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought low (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

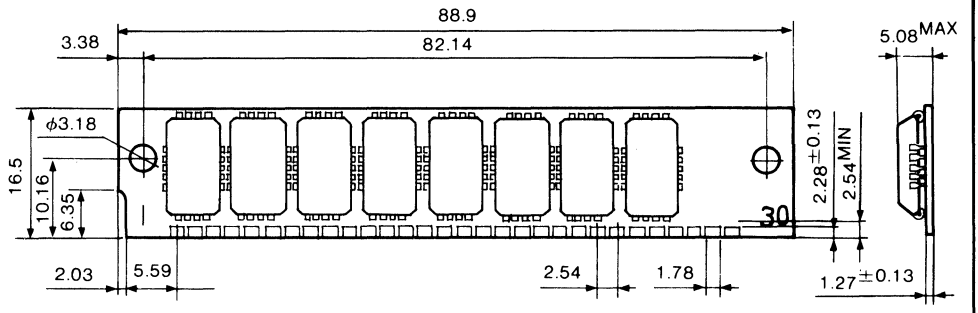
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSC2304 offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

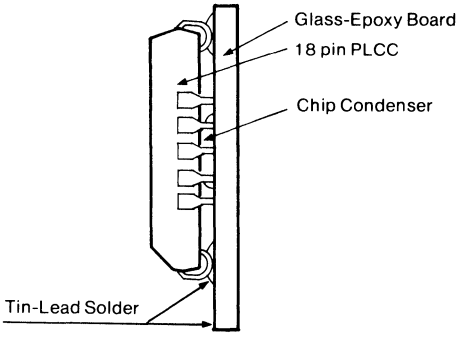
Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSC2304 hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

4

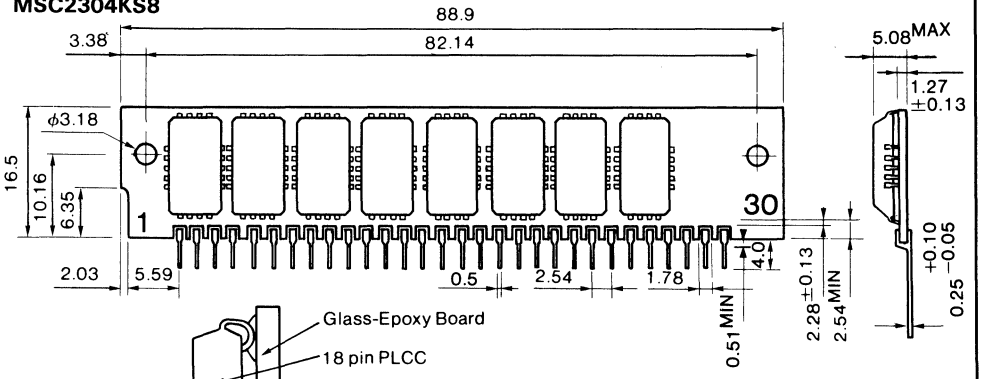
MSC2304YS8

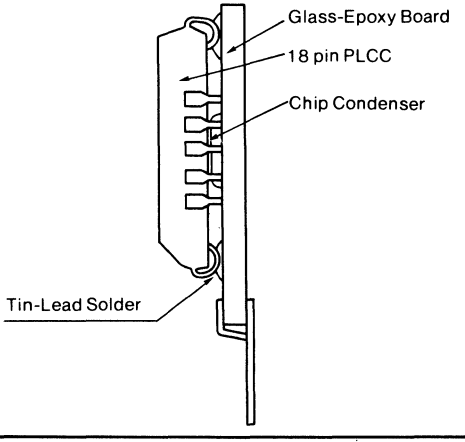




1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

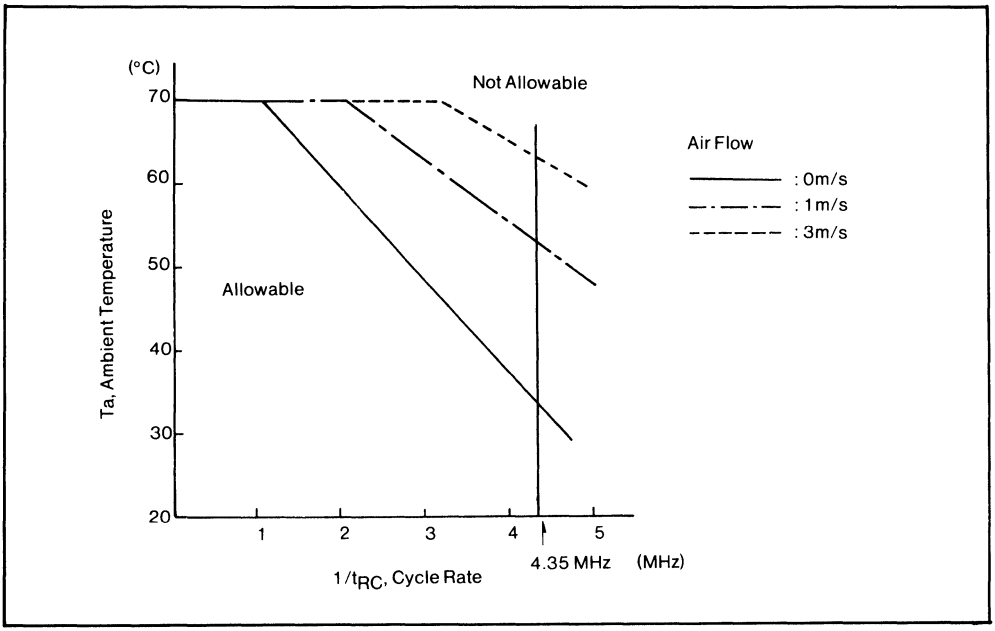
MSC2304KS8





1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

MSC2304YS8/KS8 (SIP/SIM) DERATING CURVE



MSC2304YS9/KS9

262,144 BY 9 BIT DYNAMIC RAM MODULE <Page Mode Type>

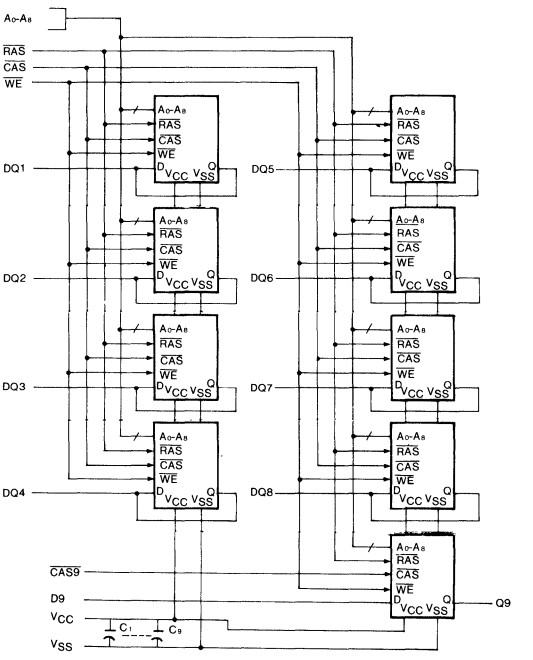
GENERAL DESCRIPTION

The Oki MSC2304YS9/KS9 is a fully decoded, 262,144 words × 9 bit NMOS dynamic random access memory composed of nine 256K DRAMs in plastic leaded chip carrier (MSM41256AJS). The mounting of nine PLCCs together with nine 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2304YS9/KS9 are quite same as the original MSM41256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

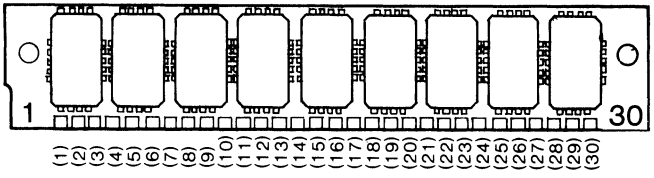
- 262,144 word × 9 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 4ms (256 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Lines
- Row Access Time;
  100ns max. (MSC2304-10YS9/KS9)
  120ns max. (MSC2304-12YS9/KS9)
  150ns max. (MSC2304-15YS9/KS9)
- Low Power Dissipation;
  2970mW max. (MSC2304-10YS9/KS9)
  2723mW max. (MSC2304-12YS9/KS9)
  2475mW max. (MSC2304-15YS9/KS9)
- Operating Temperature ... 0°C to 70°C
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- "Page Mode" capability

FUNCTIONAL BLOCK DIAGRAM

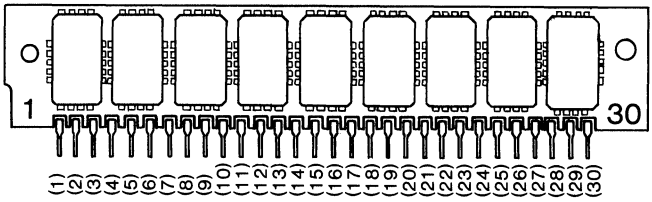


PIN ASSIGNMENT

MSC2304YS9



MSC2304KS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	Q9
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	NC	28	$\overline{CAS9}$
9	VSS	19	NC	29	D9
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	9	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4		6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0		0.8	V	

4

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	100ns MODULE		120ns MODULE		150ns MODULE		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}		540		495		450	mA
Standby Current Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2}		45		45		45	mA
Refresh Current 1 Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} = min.)	I_{CC3}		495		450		405	mA
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = min.)	I_{CC4}		360		315		270	mA
Refresh Current 2 Average power supply current ($\overline{CAS}$ before $\overline{RAS}$; t_{RC} = min.)	I_{CC5}		495		450		405	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−90	90	−90	90	−90	90	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4		2.4		2.4		V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}		0.4		0.4		0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_8$)	C_{IN1}	40	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	75	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF
Input Capacitance ($\overline{CAS9}$)	C_{IN3}	5	10	pF
Input Capacitance (D9)	C_{IN4}	4	10	pF
Output Capacitance (Q9)	C_{OUT}	4	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.) Note 1, 2, 3

Parameter	Symbol	Unit	MSC2304-10 YS9/KS9		MSC2304-12 YS9/KS9		MSC2304-15 YS9/KS9		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Refresh period	t_{REF}	ms		4		4		4	
Random read or write cycle time	t_{RC}	ns	200		220		260		
Access time from $\overline{RAS}$	t_{RAC}	ns		100		120		150	4, 6
Access time from $\overline{CAS}$	t_{CAC}	ns		50		60		75	5, 6
Output buffer turn-off delay	t_{OFF}	ns	0	30	0	30	0	30	
Transition time	t_T	ns	3	50	3	50	3	50	
$\overline{RAS}$ precharge time	t_{RP}	ns	90		90		100		
$\overline{RAS}$ pulse width	t_{RAS}	ns	100	10μs	120	10μs	150	10μs	
$\overline{RAS}$ hold time	t_{RSH}	ns	50		60		75		
$\overline{CAS}$ pulse width	t_{CAS}	ns	50	10μs	60	10μs	75	10μs	
$\overline{CAS}$ hold time	t_{CSH}	ns	100		120		150		
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	ns	25	50	25	60	25	75	7
$\overline{CAS}$ to $\overline{RAS}$ set-up time	t_{CRS}	ns	20		25		30		
Row address set-up time	t_{ASR}	ns	0		0		0		
Row address hold time	t_{RAH}	ns	15		15		15		
Column address set-up time	t_{ASC}	ns	0		0		0		
Column address hold time	t_{CAH}	ns	20		20		25		
Read command set-up time	t_{RCS}	ns	0		0		0		
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	ns	0		0		0		
Write command set-up time	t_{WCS}	ns	0		0		0		8

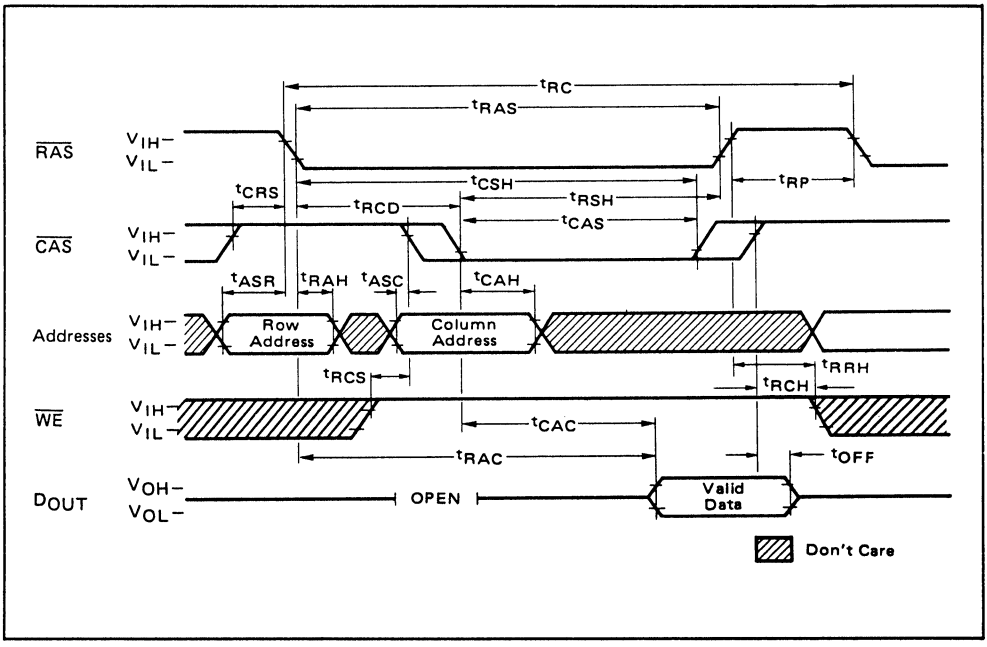
AC CHARACTERISTICS (Continued)
(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	Unit	MSC2304-10 YS9/KS9		MSC2304-12 YS9/KS9		MSC2304-15 YS9/KS9		Notes
			Min.	Max.	Min.	Max.	Min.	Max.	
Write command pulse width	t_{WP}	ns	15		20		25		
Write command hold time	t_{WCH}	ns	15		20		25		
Write command to $\overline{RAS}$ lead time	t_{RWL}	ns	35		40		45		
Write command to $\overline{CAS}$ lead time	t_{CWL}	ns	35		40		45		
Data-in set-up time	t_{DS}	ns	0		0		0		
Data-in hold time	t_{DH}	ns	20		20		25		
Refresh set-up time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCS}	ns	20		25		30		
Refresh hold time for $\overline{CAS}$ referenced to $\overline{RAS}$	t_{FCH}	ns	20		25		30		
$\overline{CAS}$ precharge time (C before R cycle)	t_{CPR}	ns	20		25		30		
$\overline{RAS}$ precharge to $\overline{CAS}$ active time	t_{RPC}	ns	20		20		20		
Page mode cycle time	t_{PC}	ns	100		120		145		8
Page mode $\overline{CAS}$ precharge time	t_{CP}	ns	40		50		60		8

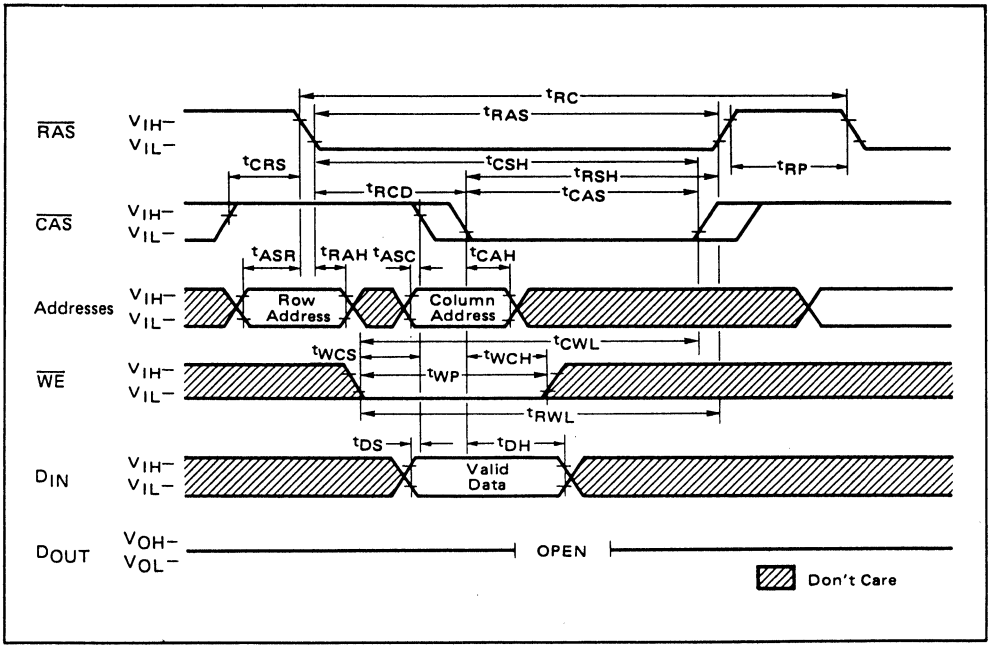
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 RAS cycles (Example: RAS only) before proper device operation is achieved.
2. The AC measurements assume $t_T = 5$ ns
3. V_{IH} (Min.) and V_{IL} (Max.) are reference levels for measuring of input signals. Also transition times are measured between V_{IH} and V_{IL}.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (Max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (Max.).
6. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
7. Operation within the t_{RCD} (Max.) limit insures that t_{RAC} (Max.) can be met. t_{RCD} (Max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (Max.) limit, then access time is controlled exclusively by t_{CAC}.
8. Page mode cycle.

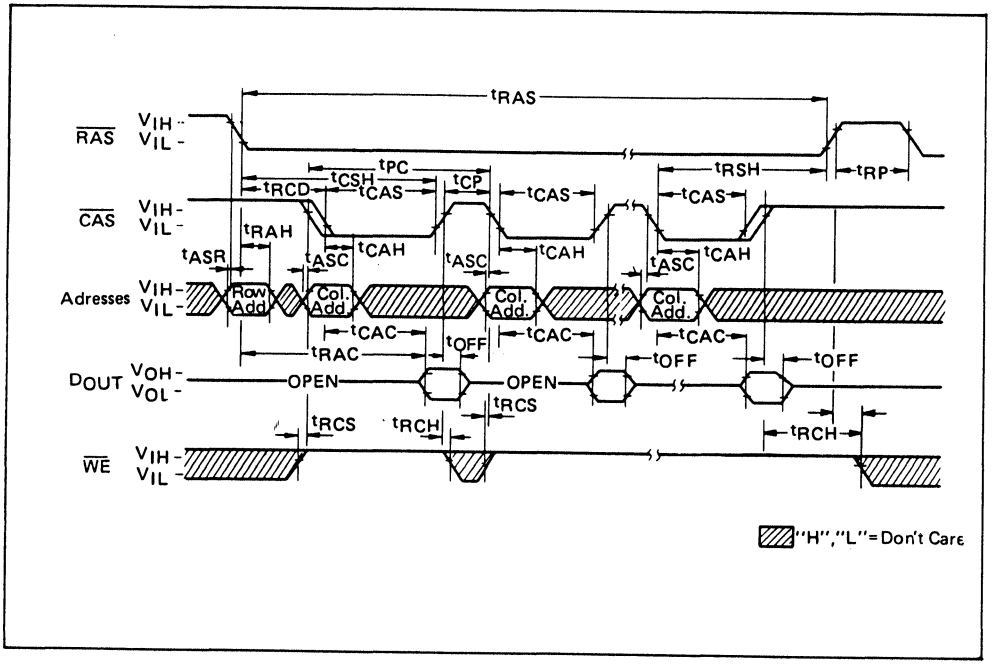
READ CYCLE



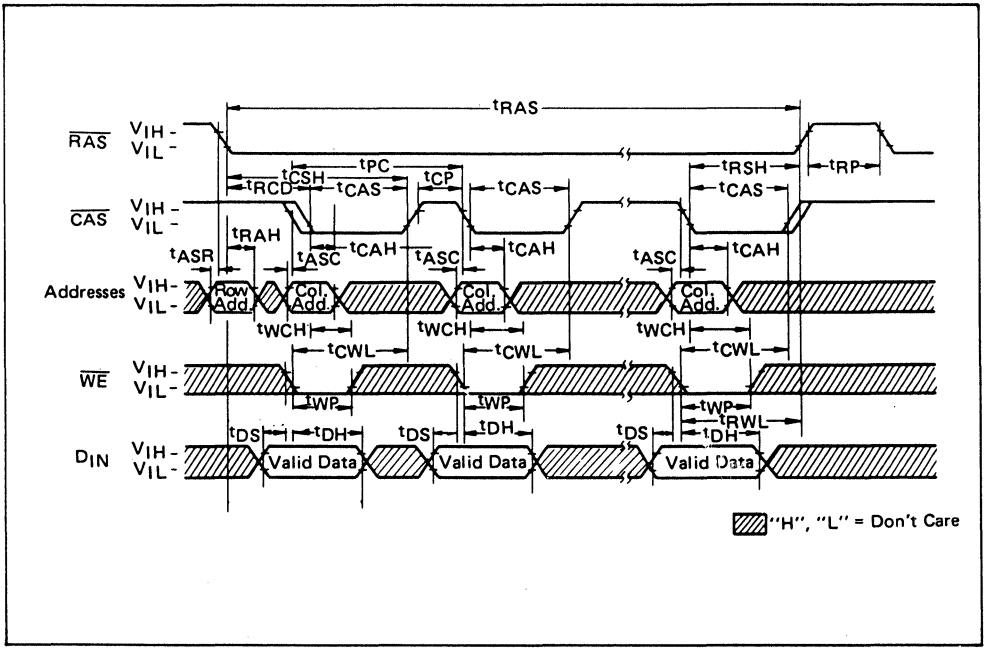
WRITE CYCLE



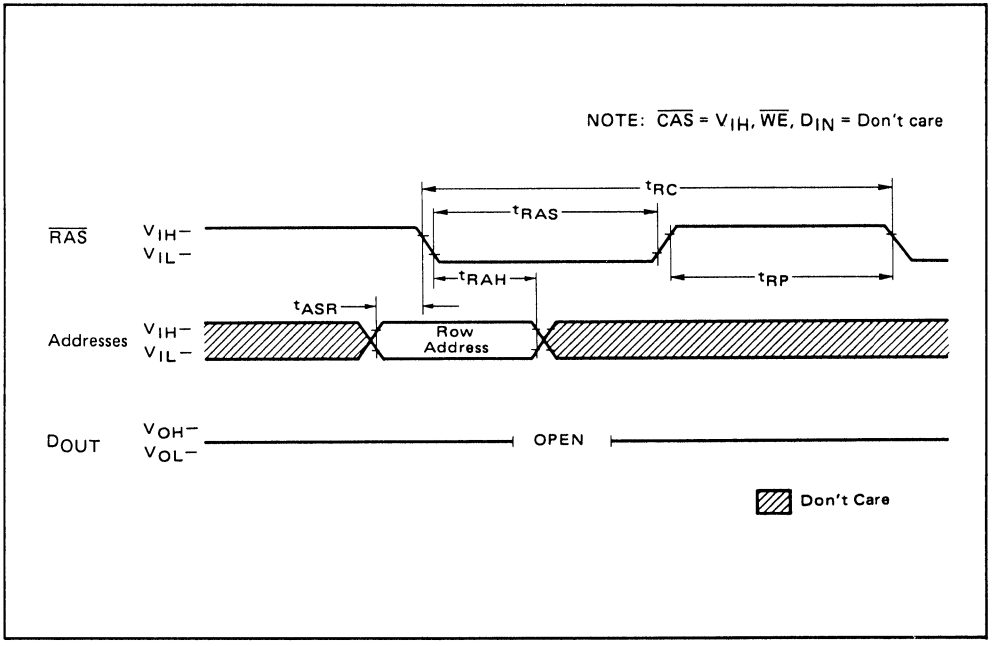
PAGE MODE READ CYCLE



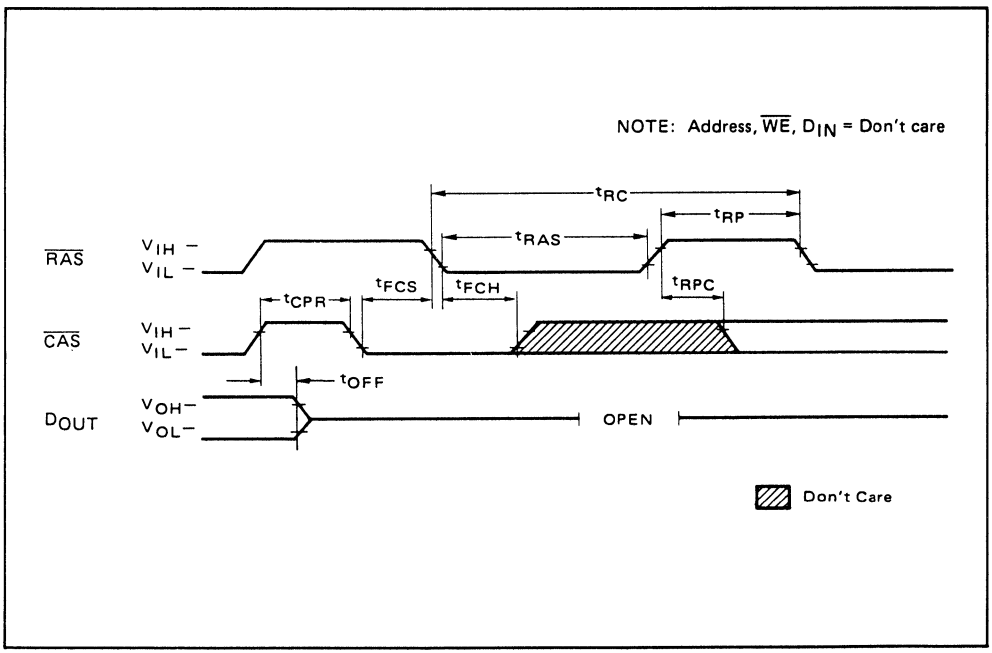
PAGE MODE WRITE CYCLE



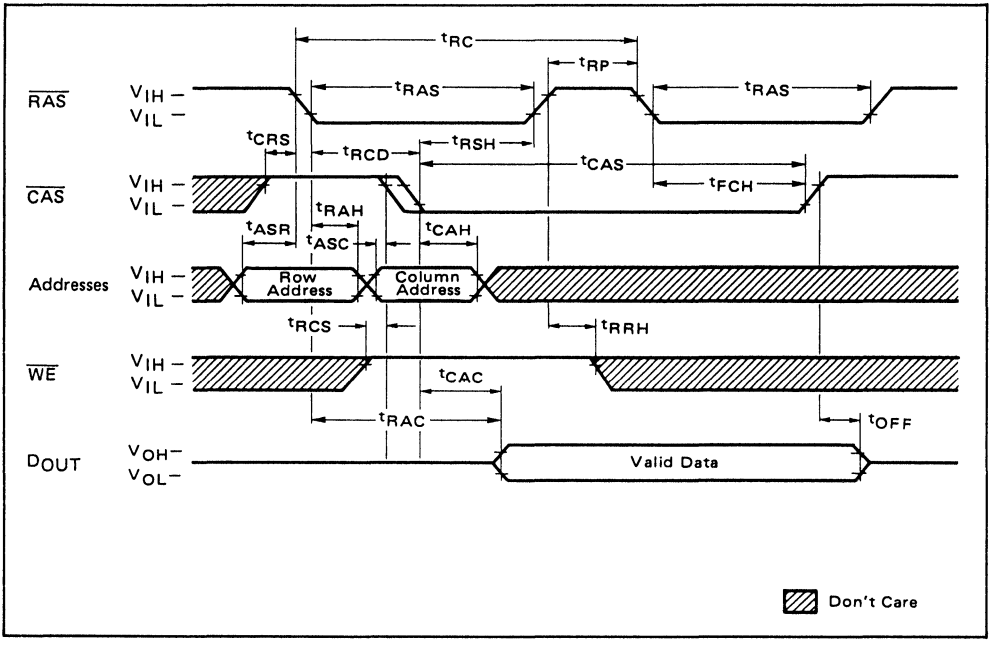
$\overline{RAS}$ ONLY REFRESH CYCLE



$\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



FUNCTIONAL DESCRIPTION

Simple Timing Requirements:

The MSC2304 has the circuit considerations for easy operational timing requirements for high speed access time operations. The MSC2304 can operate under the condition of t_{RCD} (max) = t_{CAC} which provides an optimal time space for address multiplexing. In addition, the MSC2304 has the minimal hold time of Address (t_{CAH}), $\overline{WE}$ (t_{WCH}) and D_{IN} (t_{DH}). And the MSC2304 can commit better memory system through-put during operations in an interleaved system.

Address Inputs:

A total of eighteen binary input address bits are required to decode any 1 of 262,144 storage cell location within the MSC2304. Nine row-address bits are established on the input pins (A_0 through A_8) and latched with the Row Address Strobe ($\overline{RAS}$). Then nine column address bits are established on the input pins and latched with the Column Address Strobe ($\overline{CAS}$). All input address must be stable on or before the falling edge of $\overline{RAS}$. $\overline{CAS}$ is internally inhibited (or "gated") by $\overline{RAS}$ to permit triggering of $\overline{CAS}$ as soon as the Row Address Hold Time (t_{RAH}) specification has been satisfied and the address inputs have been changed from row-addresses to column-addresses.

Write Enable:

The read or write mode is selected with the $\overline{WE}$ input. A logic "high" on $\overline{WE}$ dictates read mode, logic "low" dictates write mode. Data input is disabled when read mode is selected.

Data Input:

Data is written into the MSC2304 during a write cycle. The last falling edge of $\overline{WE}$ or $\overline{CAS}$ is a strobe for the Data in (D_{IN}) register. In a write cycle, if $\overline{WE}$ is brought "low" (write mode) before $\overline{CAS}$, D_{IN} is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$.

Data Output:

The output buffer is three-state TTL compatible with a fan-out of two standard TTL loads. Data out is the same polarity as data in. The output is in a high impedance state until $\overline{CAS}$ is brought "low". In a read cycle, or a read-write cycle, the output is valid after t_{RAC} from transition of $\overline{RAS}$ when t_{RCD} (max) is satisfied, or after t_{CAC} from transition of $\overline{CAS}$ when the transition occurs after t_{RCD} (max). Data remain valid until $\overline{CAS}$ is returned to "high". In a write cycle, the identical sequence occurs, but data is not valid.

Page Mode:

Page-mode operation permits strobing the row-address while maintaining $\overline{RAS}$ at a logic low (0) throughout all successive memory operations in which the row-address doesn't change. Thus the power dissipated by the negative going edge of $\overline{RAS}$ is saved. Further, access and cycle times are decreased because the time normally required to strobe a new row-address is eliminated.

$\overline{RAS}$ Only Refresh:

Refresh of the dynamic memory cells is accomplished by performing a memory cycle at each of the 256 row-addresses (A_0 to A_7) at least every 4 milliseconds. $\overline{RAS}$ only refresh avoids any output during refresh because the output buffer is in the high impedance state unless $\overline{CAS}$ is brought low. Strobing each of the 256 row-addresses (A_0 to A_7) with $\overline{RAS}$ will cause all bits in each row to be refreshed. Further $\overline{RAS}$ only refresh results in a substantial reduction in power dissipation.

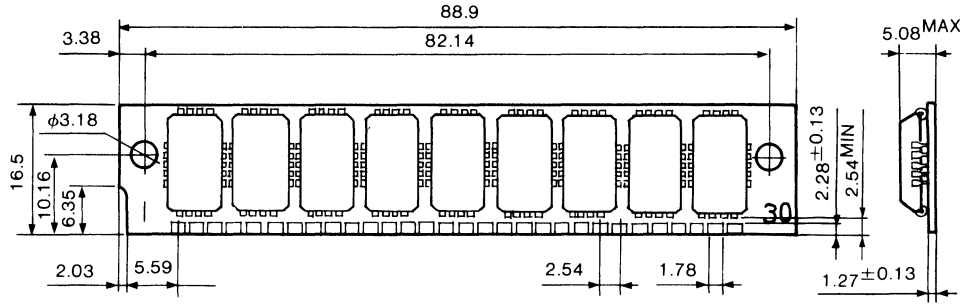
$\overline{CAS}$ Before $\overline{RAS}$ Refresh:

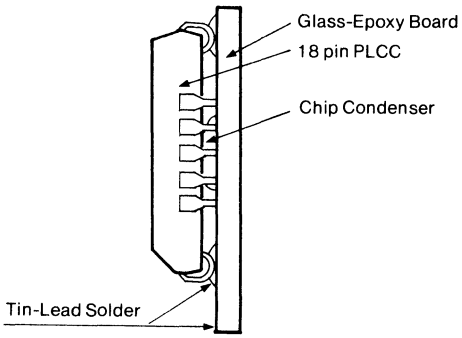
$\overline{CAS}$ before $\overline{RAS}$ refreshing available on the MSC2304 offers an alternate refresh method. If $\overline{CAS}$ is held on low for the specified period (t_{FCS}) before $\overline{RAS}$ goes to low, on chip refresh control clock generators and the refresh address counter are enabled, and an internal refresh operation takes place. After the refresh operation is performed, the refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$ before $\overline{RAS}$ refresh operation.

Hidden Refresh:

Hidden refresh cycle may take place while maintaining latest valid data at the output by extending $\overline{CAS}$ active time from the previous memory read cycle. In MSC2304 hidden refresh means $\overline{CAS}$ before $\overline{RAS}$ refresh and the internal refresh addresses from the counter are used to refresh addresses, because $\overline{CAS}$ is always low when $\overline{RAS}$ goes to low in this mode.

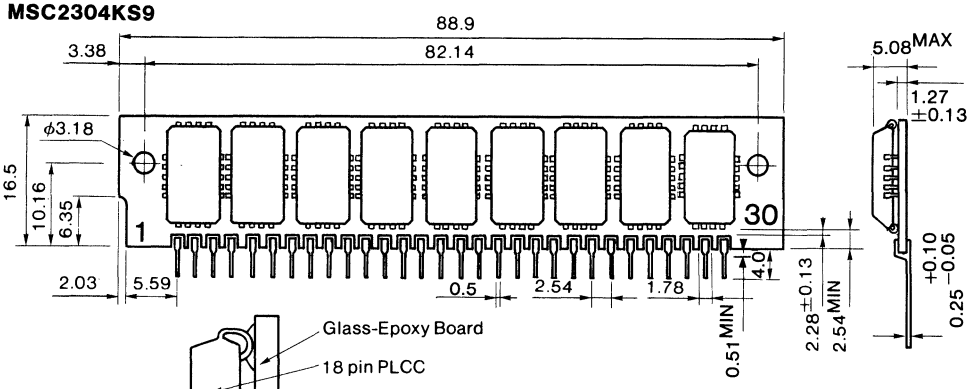
MSC2304YS9

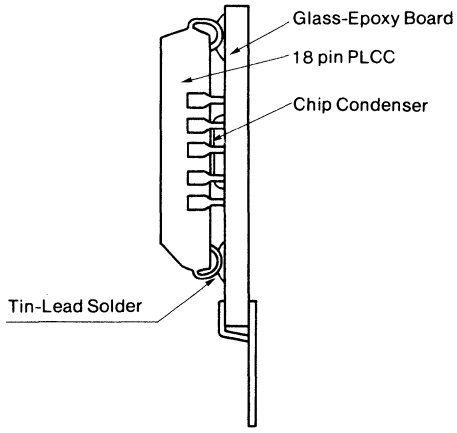




1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

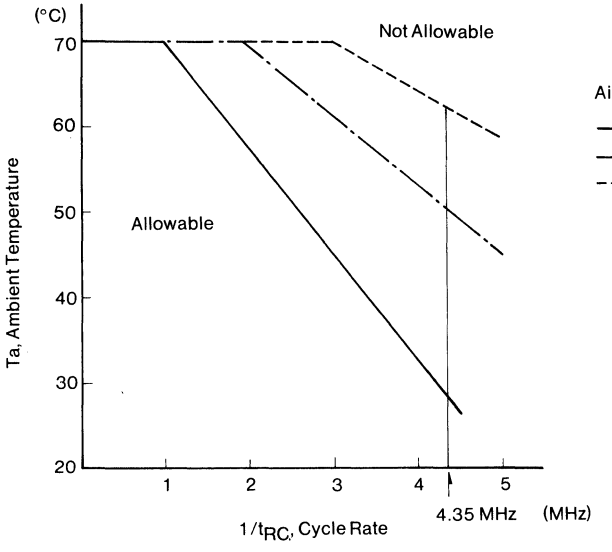
MSC2304KS9





1. Substrate: GLASS-EPOXY
2. Through Hole: Copper Plating Followed by Sn/Pb Plating
3. Contact Pads: Copper Plating Followed by Sn/Pb Plating on Copper Film (18μm^t)
4. Surface Coating: Photo Film Resist

MSC2304YS9/KS9 (SIP/SIM) DERATING CURVE



MSC2331A-XX YS3/KS3

262, 144 BY 9 BIT DYNAMIC RAM MODULE

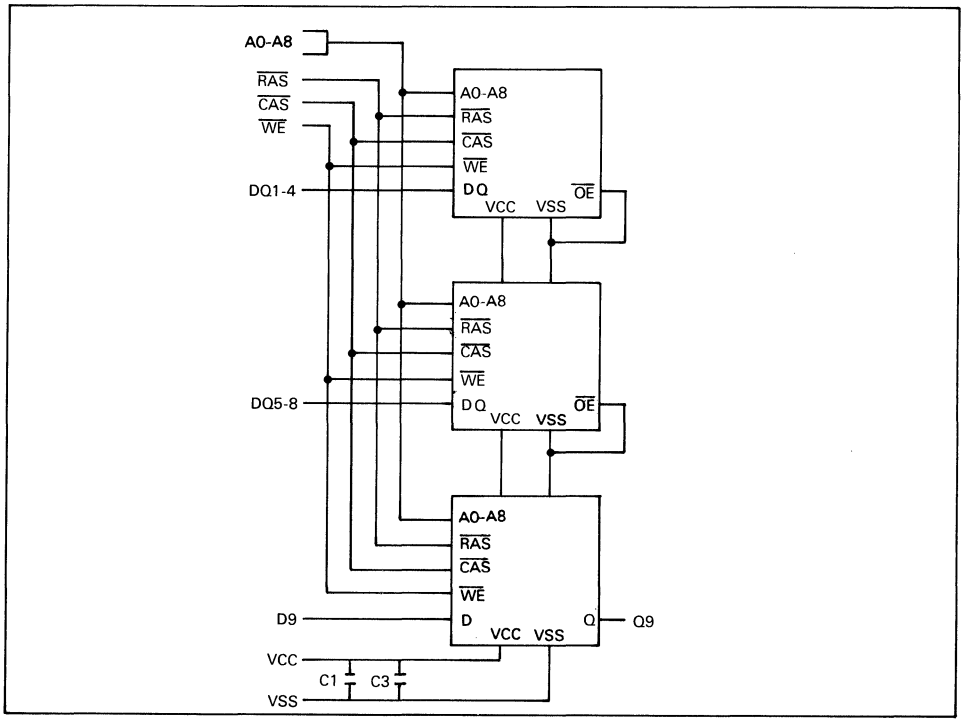
GENERAL DESCRIPTION

The Oki MSC2331A-XX YS3/KS3 is a fully decoded, 262,144 words × 9 bit CMOS dynamic random access memory composed of two 1 Mb DRAMs in SOJ (MSM514256AJS) and one 256Kb DRAM in PLCC (MSM51C256JS). The mounting of two SOJs and one PLCC together with three 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2331A-XX YS3/KS3 are quite same as the original MSM514256AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

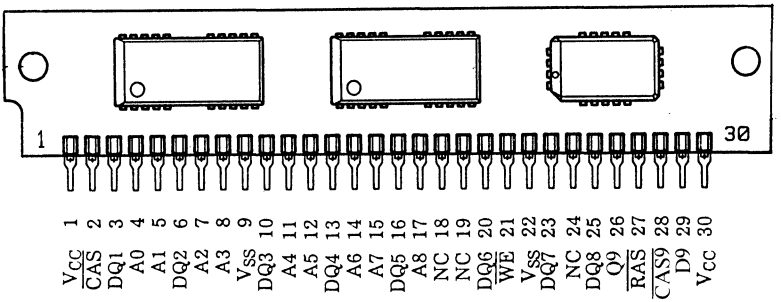
FEATURES

- 262,144 word × 9 bit Organization
- Single +5V Supply (10% Tolerance)
- Refresh Period ... 8ms (512 cycles)
- All Inputs, Outputs, Clocks
  Fully TTL compatible
- 3-States Outputs
- Common $\overline{CAS}$ Control for two Common Data-In and Data-Out Lines.
- Separate $\overline{CAS}$ Control for one Separate Pair of Data-In and Data-Out Lines.
- Row Access Time;
  80ns max. (MSC2331A-8A/80 YS3/KS3)
  100ns max. (MSC2331A-1A/10 YS3/KS3)
- Low Power Dissipation;
  1155mW max. (MSC2331A-8A/80 YS3/KS3)
  990mW max. (MSC2331A-1A/10YS3/KS3)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	Q9
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	NC	28	$\overline{CAS9}$
9	VSS	19	NC	29	D9
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	3	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

4

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSC2331A-8AYS3/KS3		MSC2331A-1AYS3/KS3		MSC2331A-80YS3/KS3		MSC2331A-10YS3/KS3		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current* average power supply (RAS, CAS cycling: t_{RC} = min.)	I_{CC1}	—	210	—	180	—	210	—	180	mA
Standby Current* power supply current (RAS = CAS = V_{IH})	I_{CC2} (TTL)	—	7.5	—	7.5	—	7.5	—	7.5	mA
	I_{CC2} (MOS)	—	4.5	—	4.5	—	4.5	—	4.5	mA
Refresh Current 1* Avarage power supply current (RAS cycling, CAS = V_{IH}: t_{RC} =min.)	I_{CC3}	—	210	—	180	—	210	—	180	mA
Refresh Current 2* Average power supply current (CAS before RAS; t_{RC} = min.)	I_{CC6}	—	210	—	180	—	210	—	180	mA
Refresh Current* Average power supply current (RAS = V_{IL}, CAS cyling: tPC =min.)	I_{CC7}	—	160	—	155	—	170	—	155	mA
Input Leakage Current Input leakage current, any input ($OV \leq V_{IN} \leq 5.5V$, all other pins not under test = OV)	I_{LI}	−20	20	−20	20	−20	20	−20	20	μA
Output Leakage Current (Data out is disabled, $OV \leq V_{OUT} \leq 5.5V$)	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA
Output Levets Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance ($A_0 \sim A_8$)	C_{I1}	40	pF
Input Capacitance (RAS, CAS, WE)	C_{I2}	40	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	20	pF
Input Capacitance ($\overline{CAS9}$)	C_{I3}	10	pF
Input Capacitance (D9)	C_{I4}	10	pF
Output Capacitance (Q9)	C_O	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSC2331A 8A YS3/KS3		MSC2331A 1A YS3/KS3		MSC2331A 80 YS3/KS3		MSC2331A 10 YS3/KS3		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
Random read or write cycle time	t_{RC}	160	—	190	—	160	—	190	—	ns	
Fast page mode cycle time	t_{PC}	55	—	55	—	50	—	55	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	80	—	100	ns	4,5,6
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	30	—	20	—	25	ns	4,5
Access time from column address	t_{AA}	—	40	—	50	—	40	—	50	ns	4,6
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	50	—	50	—	45	—	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	0	—	n_s	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100000	100	100000	80	100000	100	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25	—	30	—	20	—	25	—	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	30	10000	20	10000	25	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	80	—	100	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	55	25	70	25	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Row address set-up time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	15	—	15	—	12	—	15	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	15	—	20	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	—	75	—	60	—	75	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	50	—	40	—	50	—	ns	

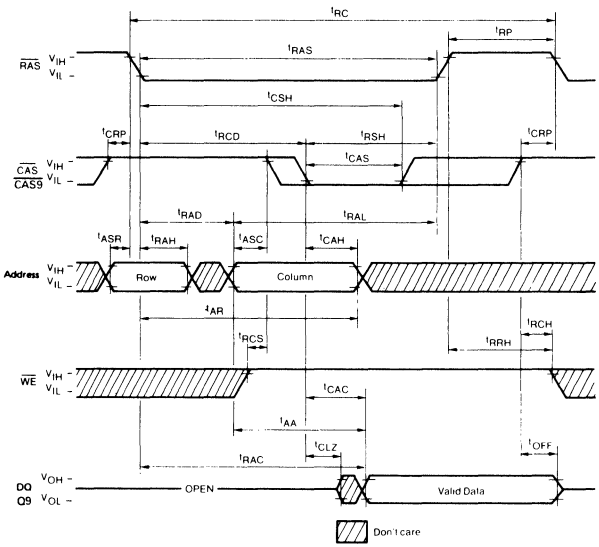
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSC2331A 8A YS3/KS3		MSC2331A 1A YS3/KS3		MSC2331A 80 YS3/KS3		MSC2331A 10 YS3/KS3		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	7
Write command hold time from $\overline{RAS}$	t_{WCR}	60	—	75	—	60	—	75	—	ns	
Write command set-up time	t_{WCS}	0	—	0	—	0	—	0	—	ns	
Write command hold time	t_{WCH}	15	—	20	—	15	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	15	—	20	—	ns	
Data-in set-up time	t_{DS}	0	—	0	—	0	—	0	—	ns	
Data-in hold time	t_{DH}	15	—	20	—	15	—	20	—	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	—	75	—	60	—	75	—	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	7
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	—	30	—	30	—	30	—	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	—	15	—	10	—	15	—	ns	

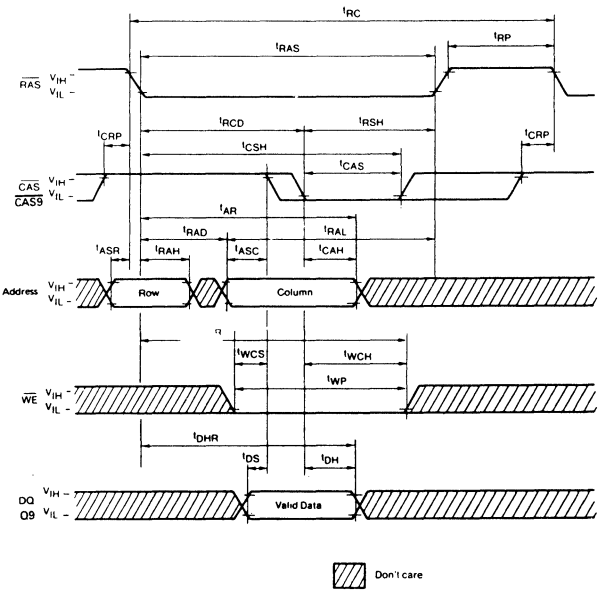
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

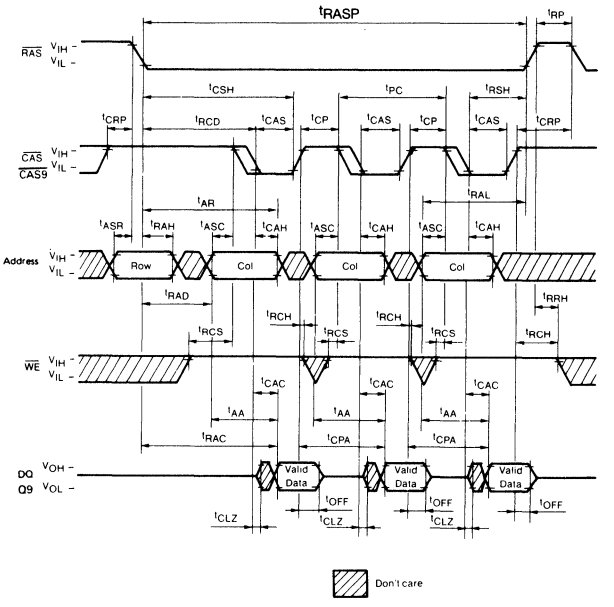
READ CYCLE



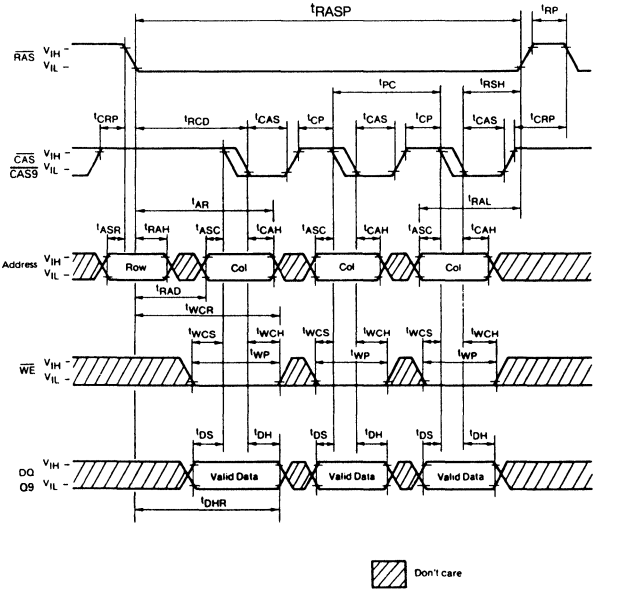
WRITE CYCLE(EARLY WRITE)



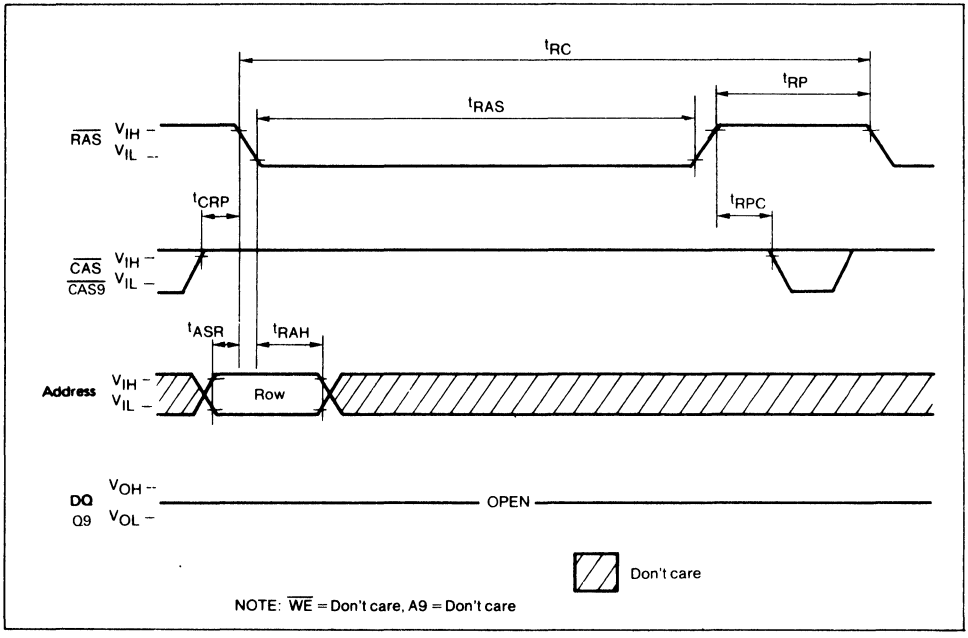
FAST PAGE MODE READ CYCLE



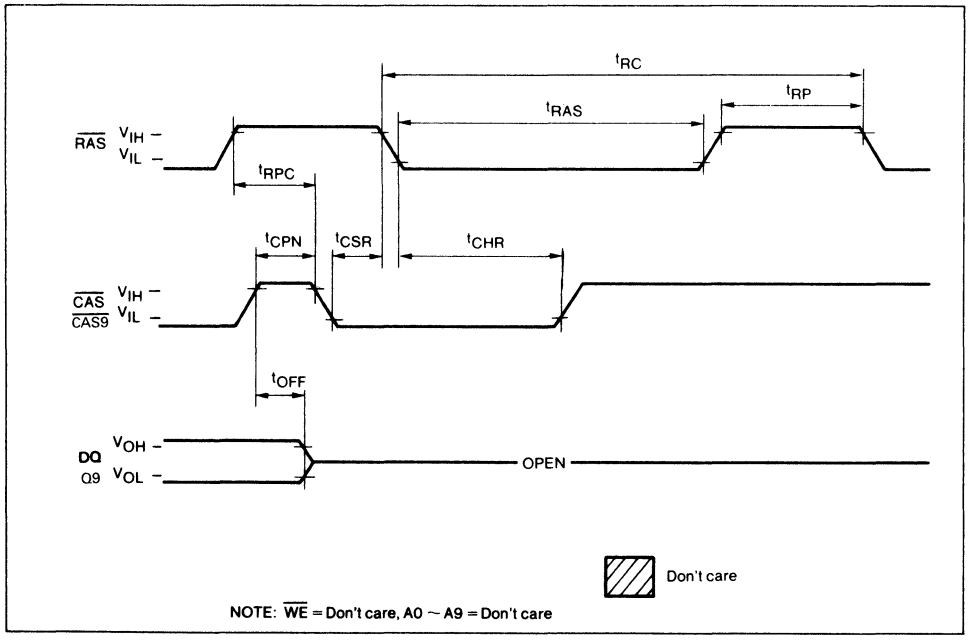
FAST PAGE MODE CYCLE (EARLY WRITE)



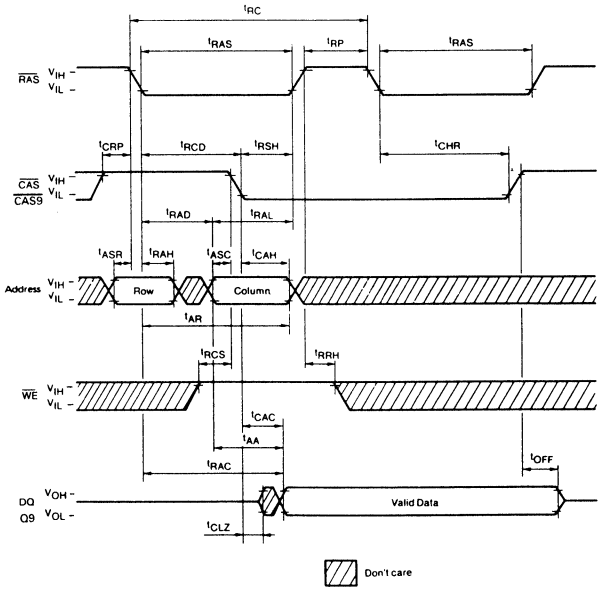
RAS ONLY REFRESH CYCLE



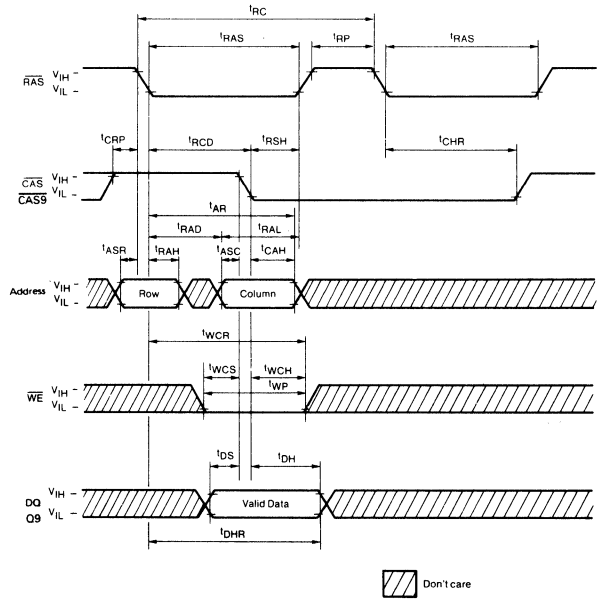
CAS BEFORE RAS AUTO REFRESH CYCLE



HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



MEMO

MEMO

MEMO

MEMO

MSC2312A-XXYS9/KS9

1,048,576 BY 9 BIT DYNAMIC RAM MODULE

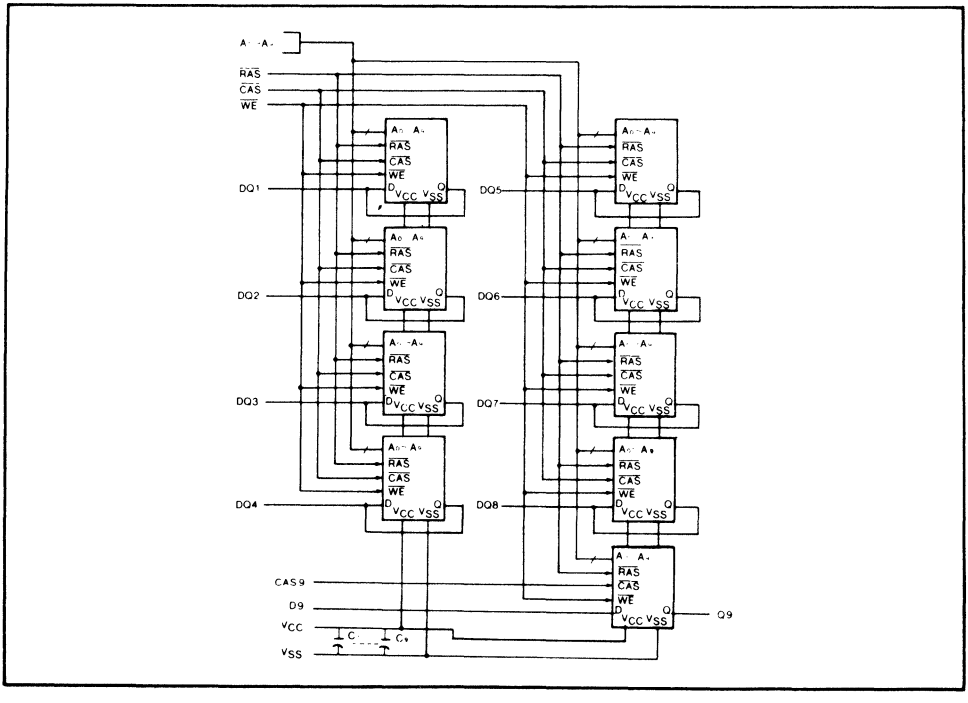
GENERAL DESCRIPTION

The Oki MSC2312A-XX YS9/KS9 is a fully decoded, 1,048,576 words × 9 bit CMOS dynamic random access memory composed of nine 1 Mb DRAMs in SOJ (MSM511000AJS). The mounting of nine SOJs together with nine 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2312A-XX YS9/KS9 are quite same as the original MSM511000A JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

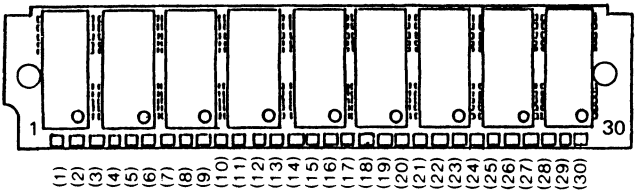
- 1,048,576 word × 9 bit Organization
- Single +5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 8ms (512 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Separate $\overline{CAS}$ Control for One Separate Pair of Data-In and Data-Out Linens
- Access Time;
  80ns max. (MSC2312A-8A/80 YS9/KS9)
  100ns max. (MSC2312A-1A/10 YS9/KS/9)
- Low Power Dissipation;
  3713mW max. (MSC2312A-8A/80 YS9/KS9)
  3218mW max. (MSC2312A-1A/10 YS9/KS9)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM

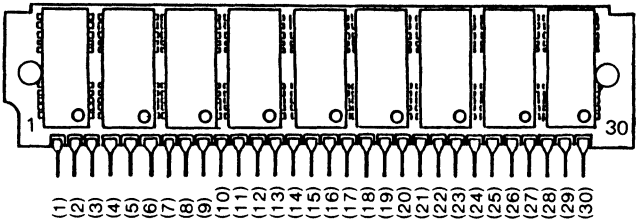


PIN ASSIGNMENT

MSC2312AYS9



MSC2312AKS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	Q9
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	$\overline{CAS9}$
9	VSS	19	NC	29	D9
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to 150	°C
Power dissipation	P_D	9	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSC2312A-8AYS9/KS9		MSC2312A-1AYS9/KS9		MSC2312A-80YS9/KS9		MSC2312A-10YS9/KS9		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}	—	675	—	585	—	675	—	585	mA
Standby Current* Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2} (TTL)	—	18	—	18	—	18	—	18	mA
	I_{CC2} (MOS)	—	9	—	9	—	9	—	9	mA
Refresh Current 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} =min.)	I_{CC3}	—	675	—	585	—	675	—	585	mA
Refresh Current 2* Average power supply current (CAS before RAS; t_{RC}=min)	I_{CC6}	—	675	—	585	—	675	—	585	mA
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} =min.)	I_{CC7}	—	495	—	495	—	540	—	495	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−90	90	−90	90	−90	90	−90	90	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_9$)	C_{IN1}	40	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	40	75	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF
Input Capacitance ($\overline{CAS9}$)	C_{IN3}	5	10	pF
Input Capacitance (D9)	C_{IN4}	4	10	pF
Output Capacitance (Q9)	C_{OUT}	4	15	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSC2312A -8AYS9/KS9		MSC2312A -1AYS9/KS9		MSC2312A -80YS9/KS9		MSC2312A -10YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
Random read or write cycle time	t_{RC}	160	—	190	—	160	—	190	—	ns	
Fast page mode cycle time	t_{PC}	55	—	55	—	50	—	55	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	80	—	100	ns	4,5,6
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	30	—	20	—	25	ns	4,5
Access time from column address	t_{AA}	—	40	—	50	—	40	—	50	ns	4,6
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	50	—	50	—	45	—	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	0	—	n_s	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100000	100	100000	80	100000	100	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25	—	30	—	20	—	25	—	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	30	10000	20	10000	25	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	80	—	100	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	70	25	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Row address set-up time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	15	—	15	—	12	—	15	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	15	—	20	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	—	75	—	60	—	75	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	50	—	40	—	50	—	ns	

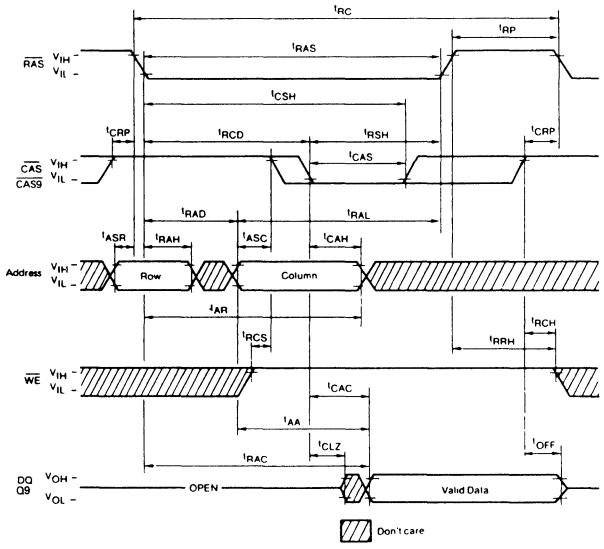
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSC2312A -8AYS9/KS9		MSC2312A -1AYS9/KS9		MSC2312A -80YS9/KS9		MSC2312A -10YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	7
Write command hold time from $\overline{RAS}$	t_{WCR}	60	—	75	—	60	—	75	—	ns	
Write command set-up time	t_{WCS}	0	—	0	—	0	—	0	—	ns	
Write command hold time	t_{WCH}	15	—	20	—	15	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	15	—	20	—	ns	
Data-in set-up time	t_{DS}	0	—	0	—	0	—	0	—	ns	
Data-in hold time	t_{DH}	15	—	20	—	15	—	20	—	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	—	75	—	60	—	75	—	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	7
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	—	30	—	30	—	30	—	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	—	15	—	10	—	15	—	ns	

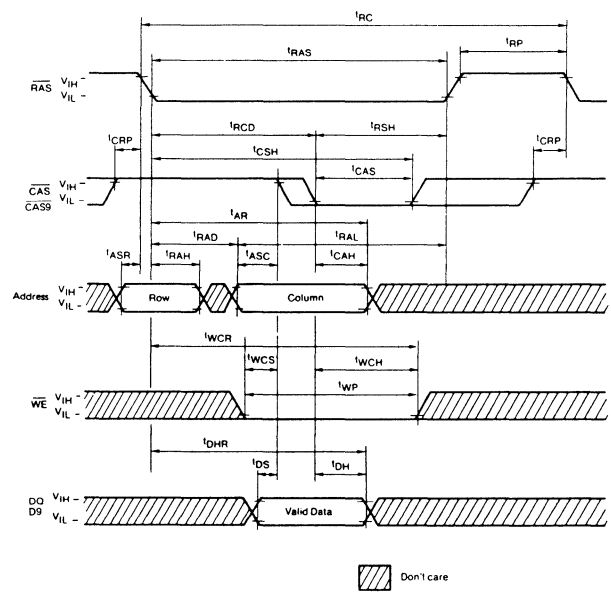
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at $t_T = 5$ ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

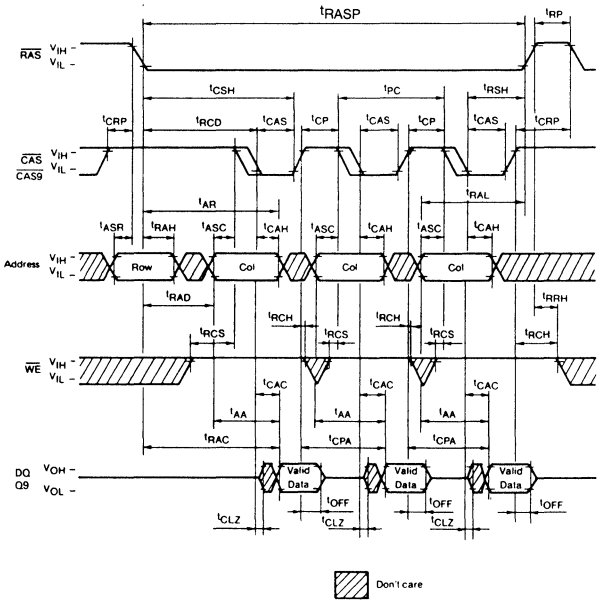
READ CYCLE



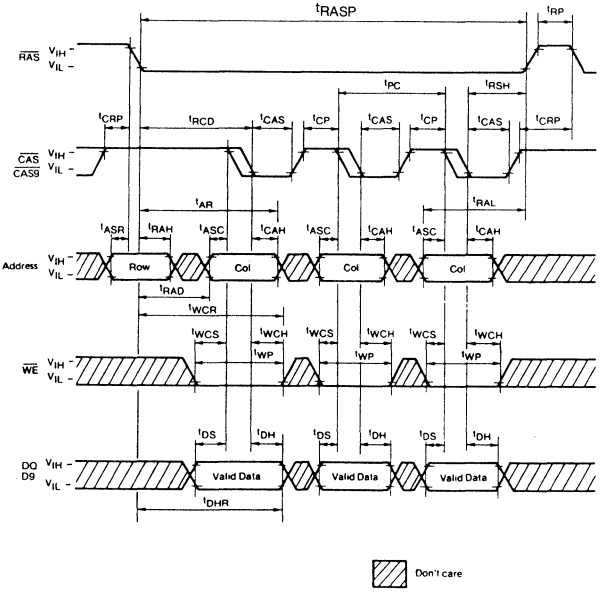
WRITE CYCLE(EARLY WRITE)



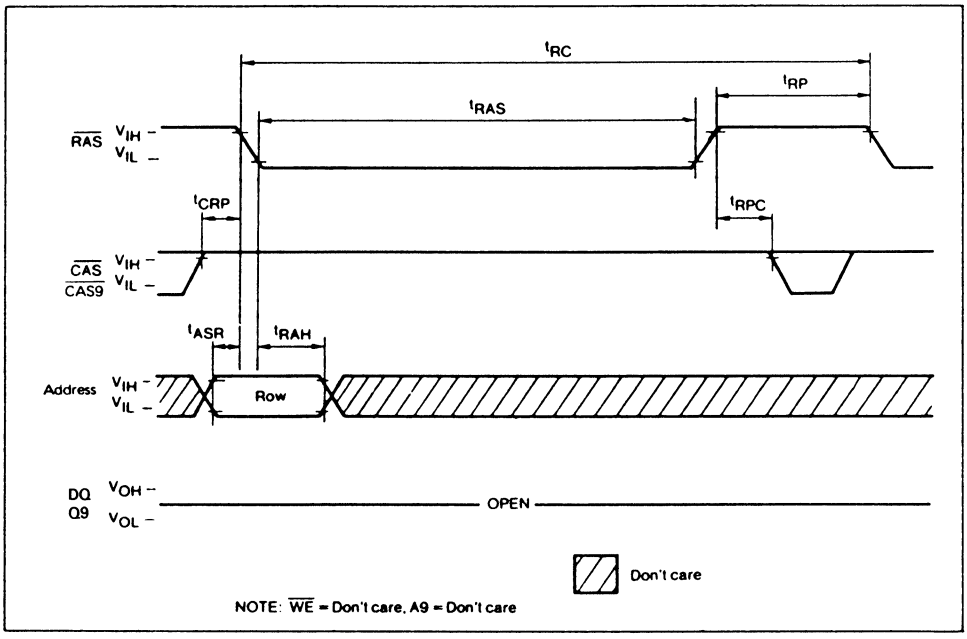
FAST PAGE MODE READ CYCLE



FAST PAGE MODE CYCLE (EARLY WRITE)

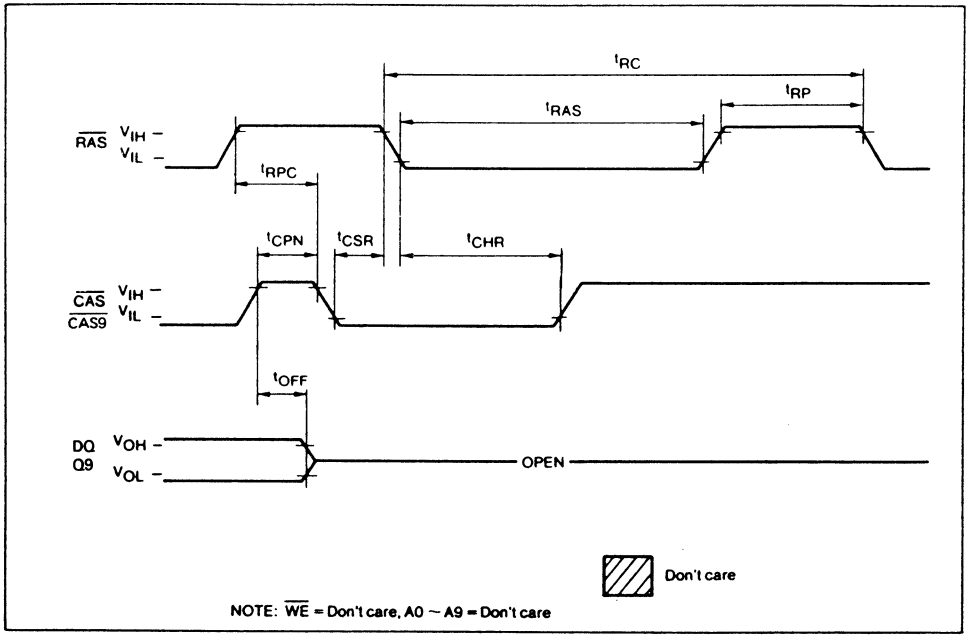


RAS ONLY REFRESH CYCLE



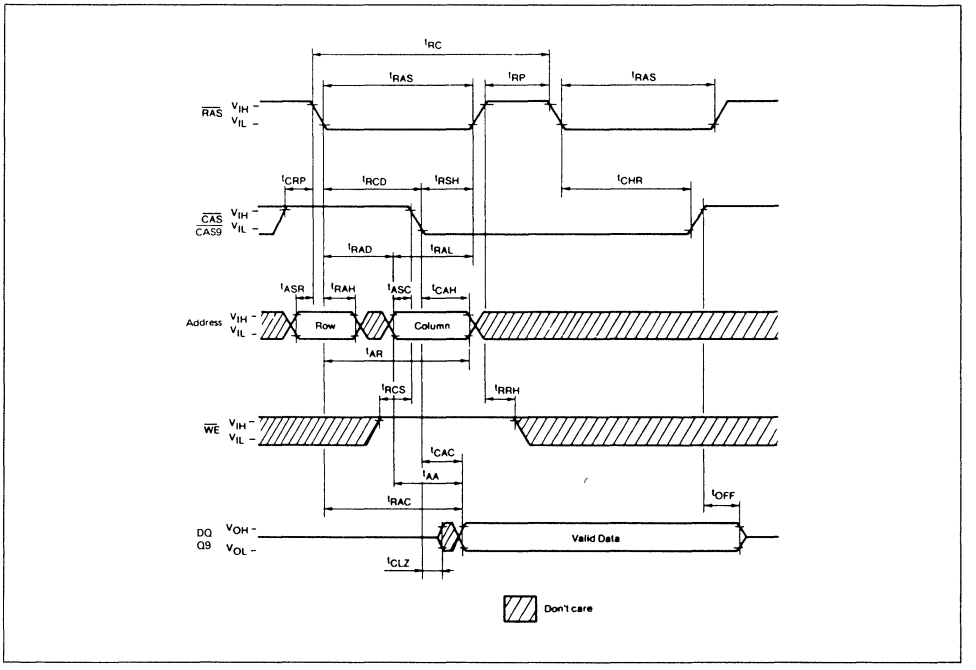
NOTE: $\overline{WE}$ = Don't care, A9 = Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE

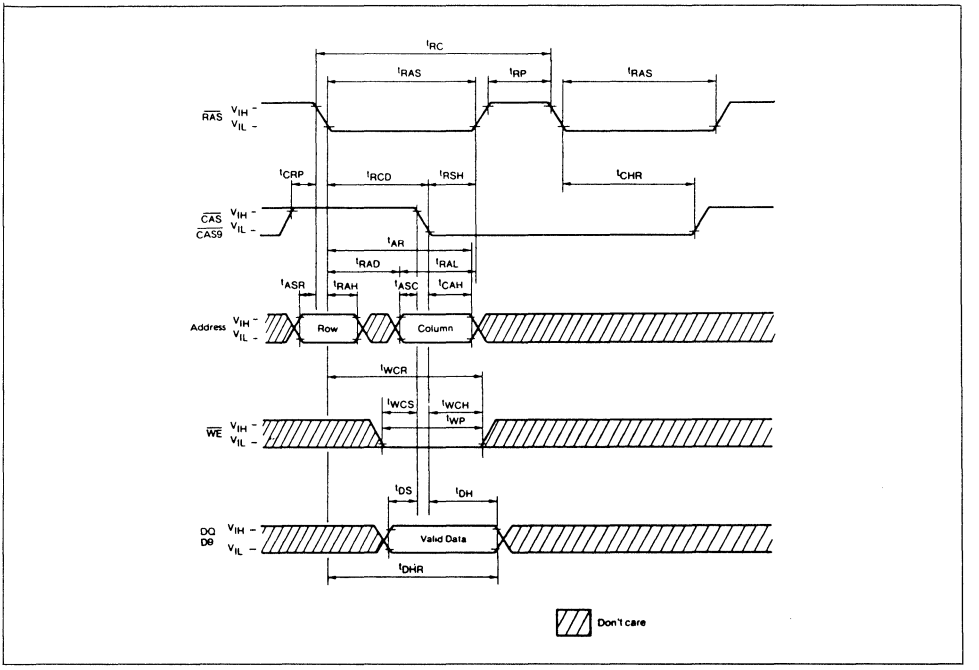


NOTE: $\overline{WE}$ = Don't care, A0 ~ A9 = Don't care

HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



MSC2313A-XX YS8/KS8

1,048,576 BY 8 BIT DYNAMIC RAM MODULE

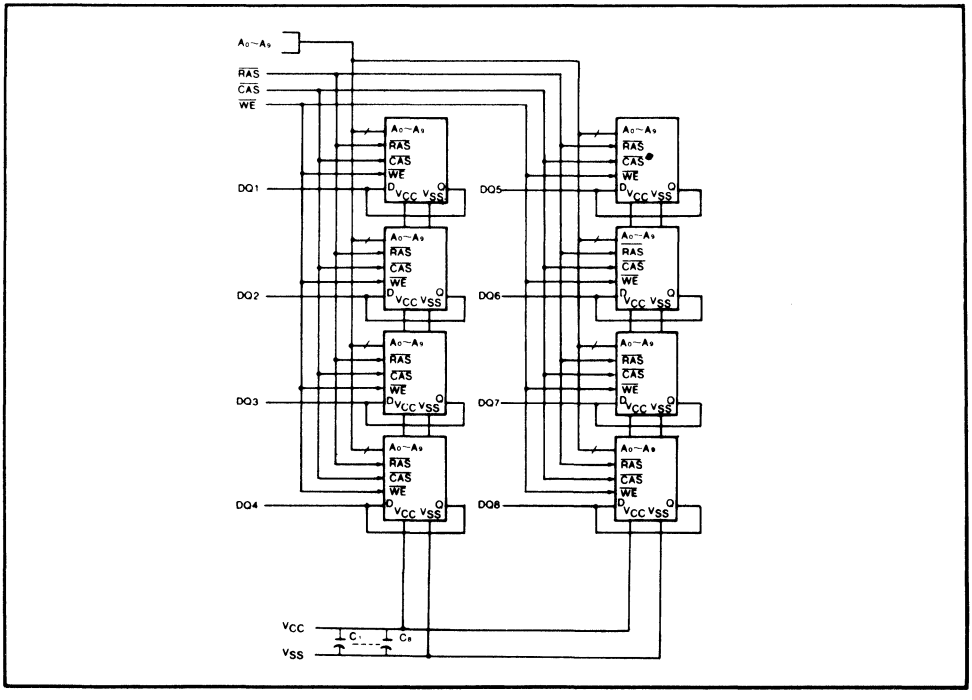
GENERAL DESCRIPTION

The Oki MSC2313A-XX YS8/KS8 is a fully decoded, 1,048,576 words×8 bit CMOS dynamic random access memory composed of nine 1Mb DRAMs in SOJ (MSM511000AJS). The mounting of nine SOJs together with nine 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2313A-XX YS8/KS8 are quite same as the original MSM511000A JS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

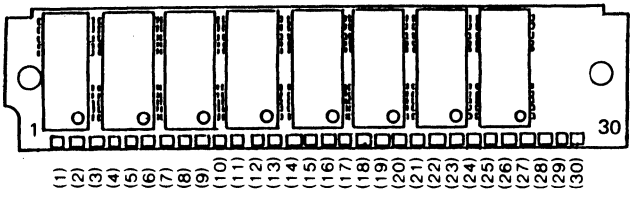
- 1,048,576 word × 8 bit Organization
- Single =5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 8ms (512 cycles)
- All Inputs, Outputs, Clocks Fully TTL compatible
- 3-States Outputs
- Common $\overline{CAS}$ Control for Eight Common Data-In and Data-Out Lines
- Row Access Time;
  80ns max. (MSC2313A-8A/80 YS8/KS8)
  100ns max. (MSC2313A-1A/10 YS8/KS8)
- Low Power Dissipation;
  3300mW max. (MSC2313A-8A/80 YS8/KS8)
  2860mW max. (MSC2313A-1A/10 YS8/KS8)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM

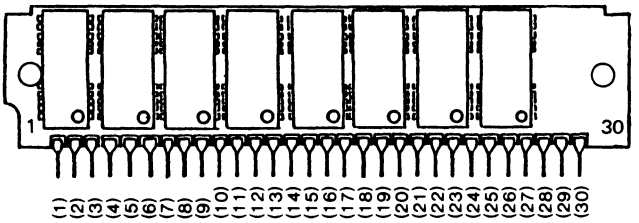


PIN ASSIGNMENT

MSC2313AYS8



MSC2313AKS8



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	NC
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	NC
9	VSS	19	NC	29	NC
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to 150	°C
Power dissipation	P_D	8	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSC2313A-8AYS8/KS8		MSC2313A-1AYS8/KS8		MSC2313A-80YS8/KS8		MSC2313A-10YS8/KS8		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}	—	600	—	520	—	600	—	520	mA
Standby Current* Power supply current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	I_{CC2} (TTL)	—	16	—	16	—	16	—	16	mA
	I_{CC2} (MOS)	—	8	—	8	—	8	—	8	mA
REfresh Current 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}; t_{RC} =min.)	I_{CC3}	—	600	—	520	—	600	—	520	mA
Refresh Current 2* Average power supply current (CAS before RAS; t_{RC} = min)	I_{CC6}	—	600	—	520	—	600	—	520	mA
Page Mode Current* Average power supply current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} =min.)	I_{CC7}	—	440	—	440	—	480	—	440	mA
Input Leakage Current Input leakage current, any input (0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V)	I_{LI}	−80	80	−80	80	−80	80	−80	80	μA
Output Leakage Current (Data out is disabled, 0V ≤ V_{OUT} ≤ 5.5V)	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ.	Max.	Unit
Input Capacitance ($A_0 \sim A_9$)	C_{IN1}	37	60	pF
Input Capacitance (RAS, CAS, WE)	C_{IN2}	35	65	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	7	20	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C)

Note 1, 2, 3

Parameter	Symbol	MSC2313A-8AYS8/KS8		MSC2313A-1AYS8/KS8		MSC2313A-80YS8/KS8		MSC2313A-10YS8/KS8		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
Random read or write cycle time	t_{RC}	160	—	190	—	160	—	190	—	ns	
Fast page mode cycle time	t_{PC}	55	—	55	—	50	—	55	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	80	—	100	ns	4,5,6
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	30	—	20	—	25	ns	4,5
Access time from column address	t_{AA}	—	40	—	50	—	40	—	50	ns	4,6
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	50	—	50	—	45	—	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	0	—	ns	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100000	100	100000	80	100000	100	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25	—	30	—	20	—	25	—	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	30	10000	20	10000	25	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	80	—	100	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	55	25	70	25	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Row address set-up time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	15	—	15	—	12	—	20	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	15	—	25	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	—	75	—	60	—	75	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	50	—	40	—	50	—	ns	

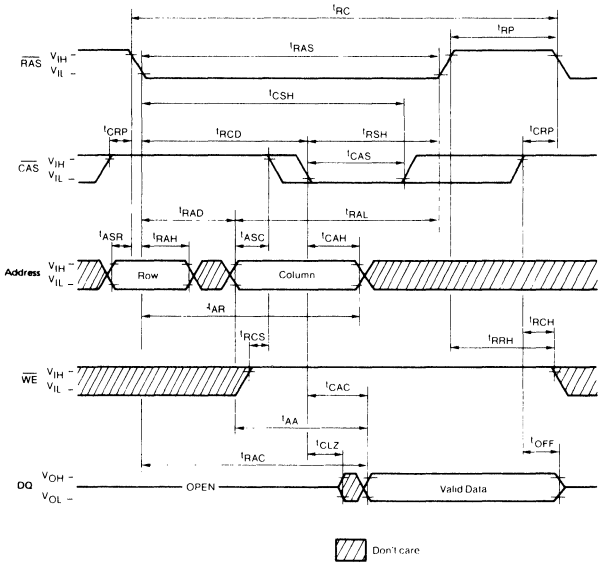
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSC2313A-8AYS8/KS8		MSC2313A-1AYS8/KS8		MSC2313A-80YS8/KS8		MSC2313A-10YS8/KS8		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	7
Write command hold time from $\overline{RAS}$	t_{WCR}	60	—	75	—	60	—	75	—	ns	
Write command set-up time	t_{WCS}	0	—	0	—	0	—	0	—	ns	
Write command hold time	t_{WCH}	15	—	20	—	15	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	15	—	20	—	ns	
Data-in set-up time	t_{DS}	0	—	0	—	0	—	0	—	ns	
Data-in hold time	t_{DH}	15	—	20	—	15	—	20	—	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	—	75	—	60	—	75	—	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	7
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	—	30	—	30	—	30	—	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	—	15	—	10	—	15	—	ns	

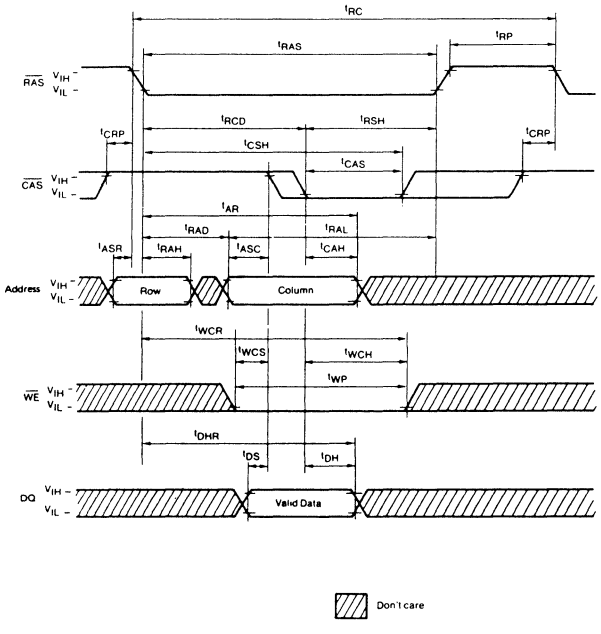
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

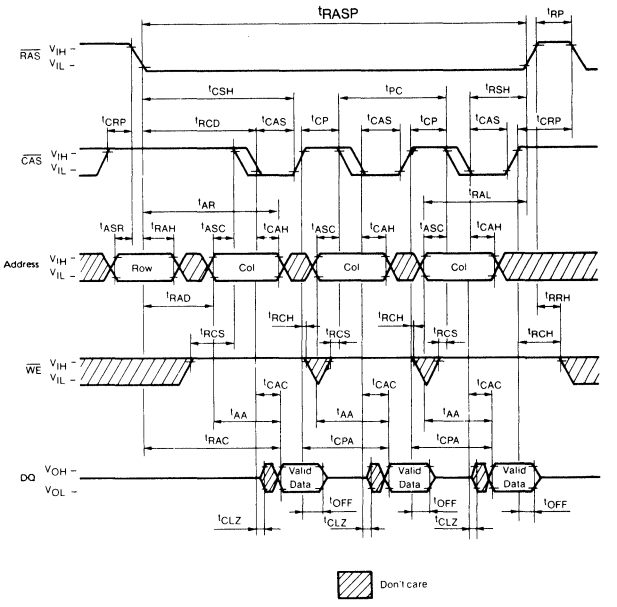
READ CYCLE



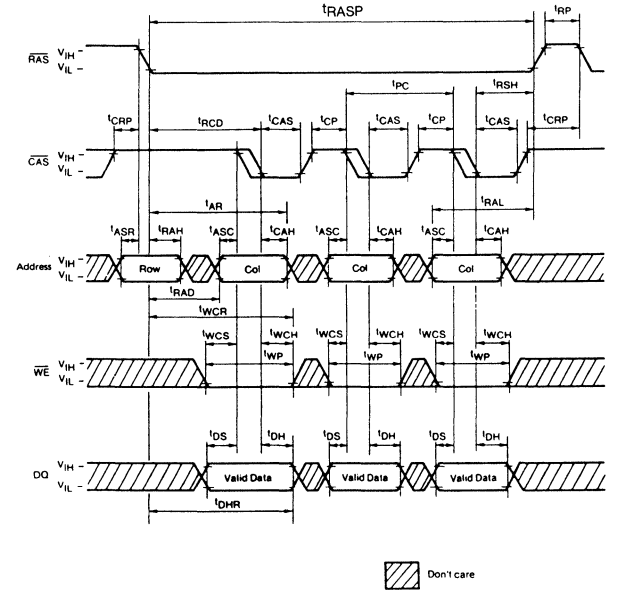
WRITE CYCLE(EARLY WRITE)



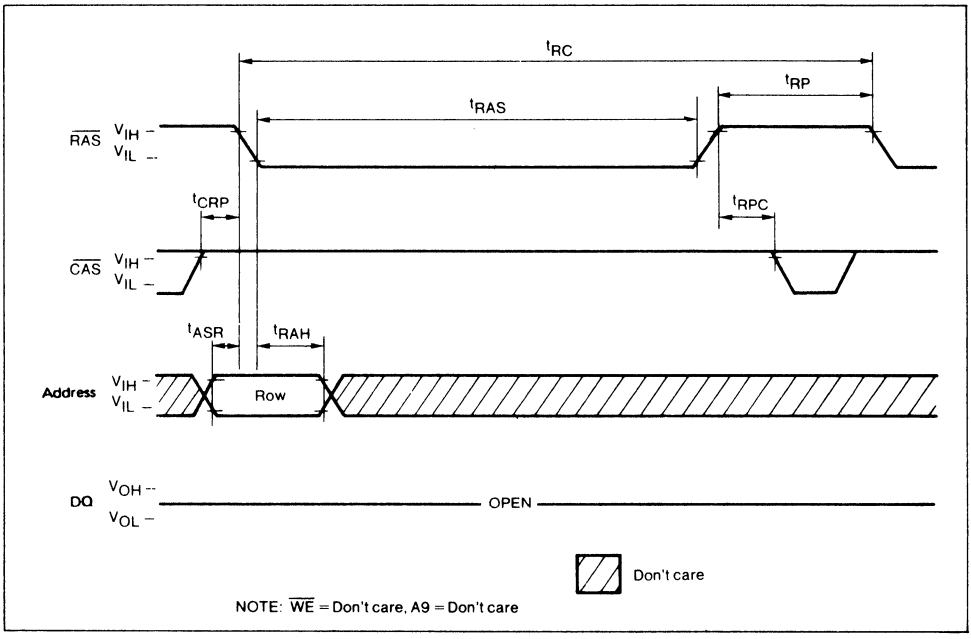
FAST PAGE MODE READ CYCLE



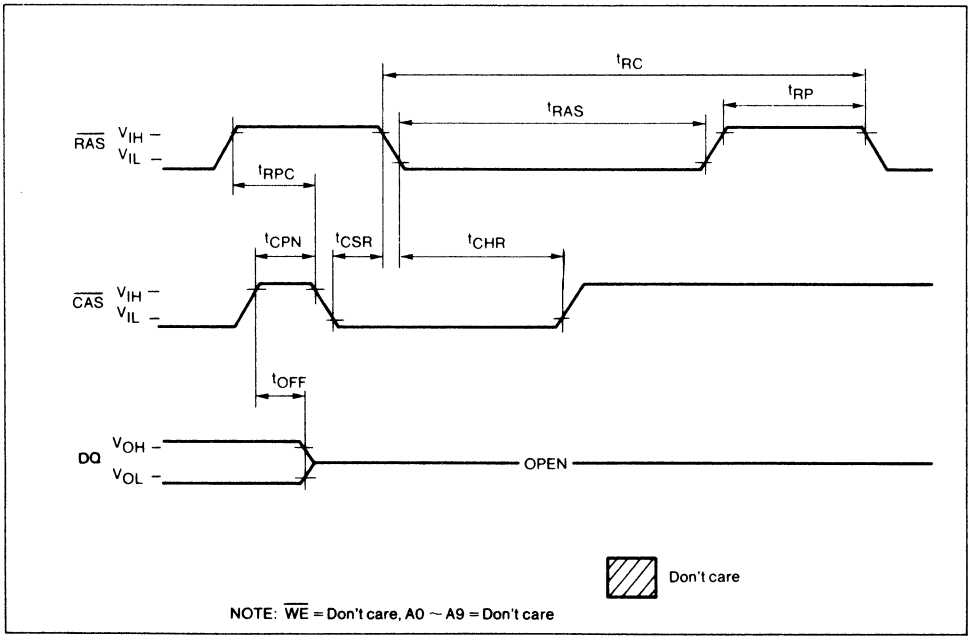
FAST PAGE MODE CYCLE (EARLY WRITE)



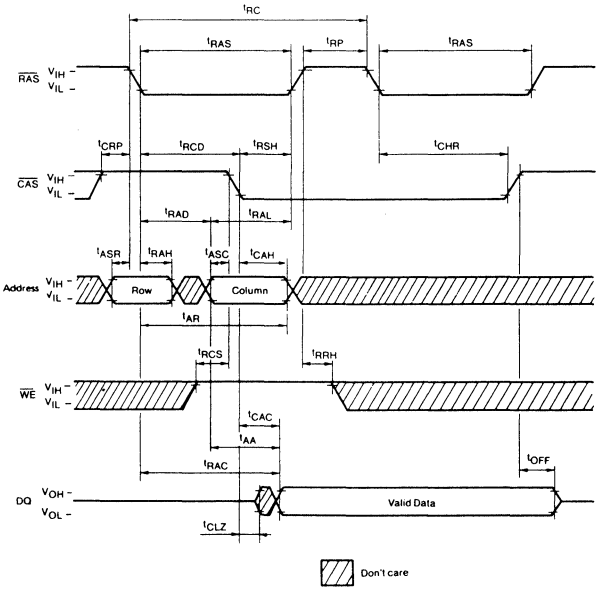
RAS ONLY REFRESH CYCLE



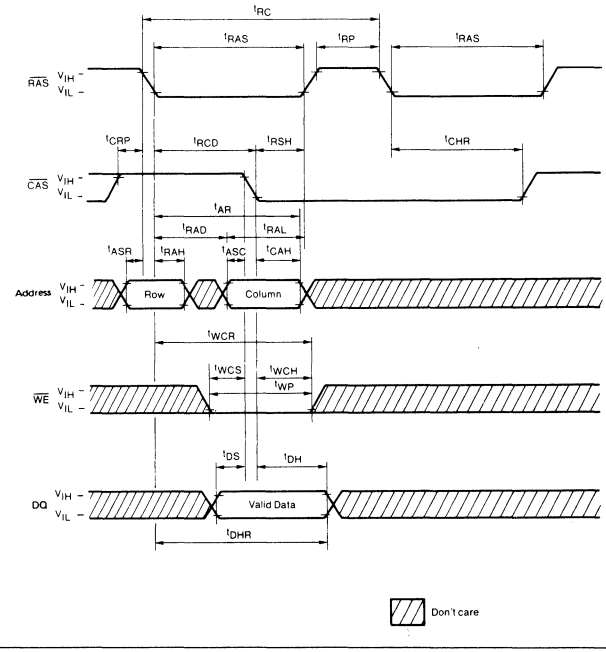
CAS BEFORE RAS AUTO REFRESH CYCLE



HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



MSC2320A-XXYS9

262, 144 BY 36BIT DYNAMIC RAM MODULE

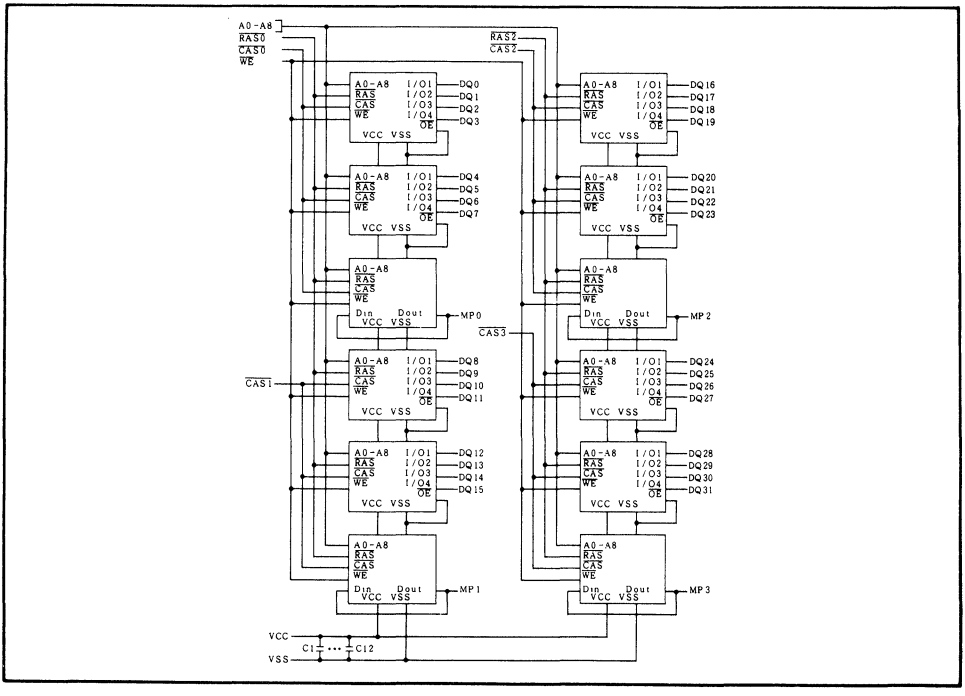
GENERAL DESCRIPTION

The Oki MSC2320A-XXYS9 is a fully decoded, 262,144 words × 36 bit CMOS dynamic random access memory composed of eight 1 Mb DRAMs in SOJ (MSM514256AJS) and four 256 Kb drams in SOJ (MSM51256JS). The mounting of twelve SOJs together with twelve 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2320A-XXYS9 are quite same as the original MSM511000AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

FEATURES

- 262,144 word × 36 bit Organization
- Single +5V Supply (5 % Tolerance)
- Refresh Period ... 8ms (512 cycles)
- All Inputs, Outputs, Clocks
  Fully TTL compatible
- JEDEC Compatible Dimensioning
- $\overline{CAS}$ before $\overline{RAS}$ refresh, RAS only refresh, hidden refresh, and fast page mode capability
- Access Time;
  80ns max. (MSC2320A-8A/80 YS9)
  100ns max. (MSC2320A-1A/10YS9)
- Low Power Dissipation;
  4410mW max. (MSC2320A-8A/80 YS9)
  3780mW max. (MSC2320A-1A/10YS9)
- Operating Temperature ... 0°C to 70°C
- Fast access and cycle times

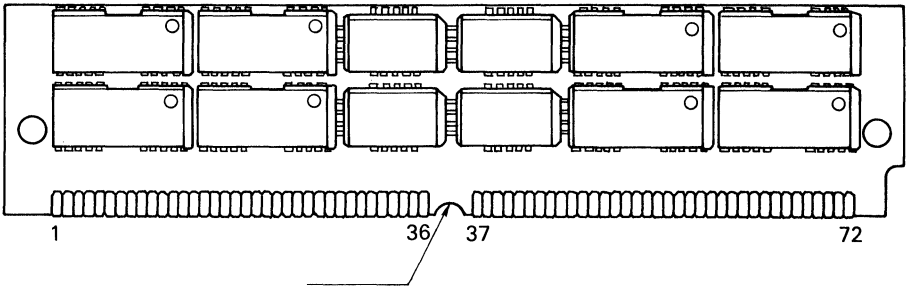
FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT

MSC2320A-XXYS9

BOTTOM



Pinout Assignments

Pin No.	Assign	Pin No.	Assign	Pin No.	Assign	Pin No.	Assign	Pin No.	Assign	Pin No.	Assign	
											100 ns	80 ns
1	V_{SS}	13	A1	25	DQ22	37	MP1	49	DQ8	61	DQ13	–
2	DQ0	14	A2	26	DQ7	38	MP3	50	DQ24	62	DQ30	–
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14	–
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ31	–
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15	–
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC	–
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ11	67	V_{SS}	V_{SS}
8	DQ3	20	DQ4	32	NC	44	$\overline{RAS0}$	56	DQ27	68	NC	NC
9	DQ19	21	DQ20	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ12	69	V_{SS}	NC
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	V_{SS}	V_{SS}
11	NC	23	DQ21	35	MP2	47	WE	59	V_{CC}	71	NC	–
12	A0	24	DQ6	36	MP0	48	NC	60	DQ29	72	V_{SS}	–

Note: V_{CC} is the source, V_{SS} is ground and NC is no connection.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	12	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSC2320A-8AYS9		MSC2320A-1AYS9		MSC2320A-80YS9		MSC2320A-10YS9		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current average power supply ($\overline{RAS}$, $\overline{CAS}$ Address cycling)	ICC1	—	840	—	720	—	840	—	720	mA
Standby current power supply standby current	ICC2	—	30	—	30	—	30	—	30	mA
$\overline{RAS}$ only refresh current ($\overline{RAS}$ only mode, $\overline{RAS}$ cycling)	ICC3	—	840	—	720	—	840	—	720	mA
Fast page mode current	ICC4	—	640	—	620	—	680	—	620	mA
Standby current	ICC5	—	18	—	18	—	18	—	18	mA
$\overline{CAS}$ before $\overline{RAS}$ refresh current	ICC6	—	840	—	720	—	840	—	720	mA
Input leakage current	II(L)	-120	120	-120	120	-120	120	-120	120	μA
Output leakage current dout disagled	IO(L)	—10	10	—10	10	—10	10	—10	10	μA
Output high level	IOH	2.4	—	2.4	—	2.4	—	2.4	—	mA
Output low level	VOL	—	0.4	—	0.4	—	0.4	—	0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(V_{CC} = 5 Volts ± 5%, f = 1MHz, Tc = 0 ~ 70°C)

Symbol	Parameter	Min.	Max.	Unit
C_{I_1}	Input Capacitance (A_0 ~A_8)	—	88	pF
C_{I_2}	Input Capacitance ($\overline{W}$)	—	104	pF
C_{I_3}	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	—	57	pF
C_{I_4}	Input Capacitance ($\overline{CAS0}$ — $\overline{RAS3}$)	—	36	pF
CDQ_1	I/O Cap (DQ0 — DQ31)	—	17	pF
CDQ_2	I/O Cap (MP0 — MP3)	—	22	pF

Capacitance measured with Boonton Meter.

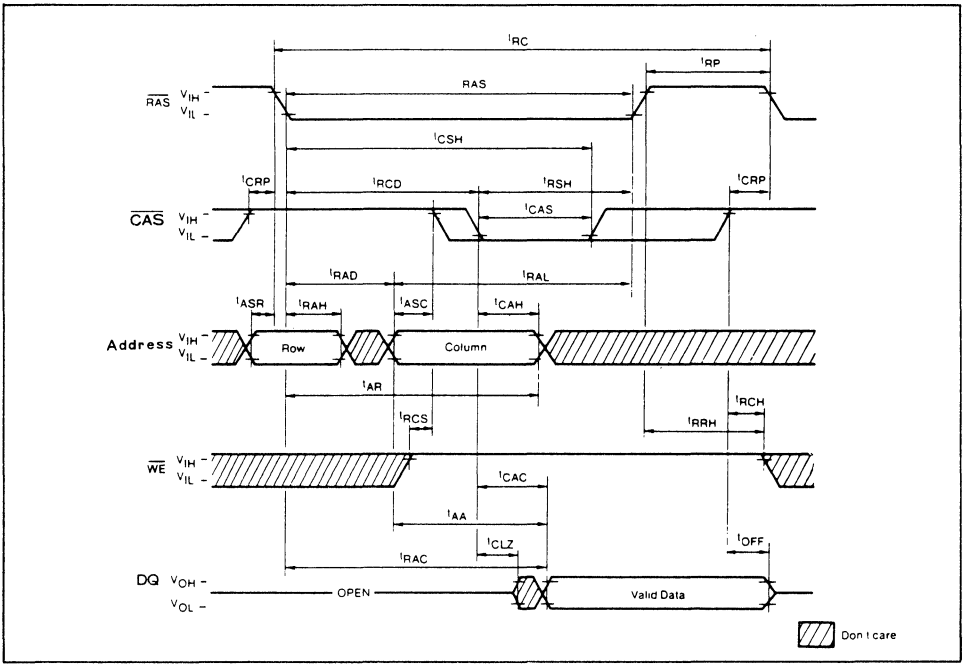
Electrical Characteristics and Recommended AC Operating Conditions

Symbol	Parameter	MSC2320A-8AYS9		MSC2320A-1AYS9		MSC2320A-80YS9		MSC2320A-10YS9		Units	Notes
		MIN.	MAX	MIN.	MAX	MIN.	MAX	MIN.	MAX		
tRC	Random read or write cycle time	160	—	190	—	160	—	190	—	ns	
tPC	Fast page mode cycle time	55	—	55	—	50	—	55	—	ns	
tRAC	Access time from $\overline{RAS}$	—	80	—	100	—	80	—	100	ns	2, 7
tCAC	Access time from $\overline{CAS}$	—	25	—	30	—	20	—	25	ns	2, 7
tAA	Access time from Column address	—	40	—	50	—	40	—	50	ns	2, 8
tCPA	Access time from $\overline{CAS}$ procharge	—	50	—	50	—	45	—	50	ns	2
tCLZ	$\overline{CAS}$ to output in Lo-Z	—	0	—	0	—	0	—	0	ns	2
tOFF	Output buffer turn-off delay	0	20	0	20	0	20	0	20	ns	3
tT	Transition time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	1
tRP	$\overline{RAS}$ procharge time	70	—	80	—	70	—	80	—	ns	
tRAS	$\overline{RAS}$ pulse width	80	10,000	100	10,000	80	10,000	100	10,000	ns	
tRASP	$\overline{RAS}$ pulse width (Fast page mode)	80	100,000	100	100,000	80	100,000	100	100,000	ns	
tRSH	$\overline{RAS}$ hold time	25	—	30	—	20	—	25	—	ns	
tCSH	$\overline{CAS}$ hold time	80	—	100	—	80	—	100	—	ns	
tCAS	$\overline{CAS}$ pulse width	25	10,000	30	10,000	20	10,000	25	10,000	ns	
tRCD	$\overline{RAS}$ to $\overline{CAS}$ delay time	25	55	25	70	22	60	25	75	ns	7
tRAD	$\overline{RAS}$ to column address delay time	20	40	20	50	17	40	20	50	ns	8
tCRP	$\overline{CAS}$ to $\overline{RAS}$ precharge time	10	—	10	—	10	—	10	—	ns	
tCP	$\overline{CAS}$ precharge time (Fast page mode)	10	0	10	—	10	—	10	—	ns	
tASR	Row address set-up time	0	—	0	—	0	—	0	—	ns	
tRAH	Row address hold time	15	—	15	—	12	—	15	—	ns	
tASC	Column address set-up time	0	—	0	—	0	—	0	—	ns	
tCAH	Column address hold time	15	—	20	—	15	—	20	—	ns	
tAR	Column address hold time ref to $\overline{RAS}$	60	—	75	—	60	—	75	—	ns	
tRAL	Column address to $\overline{RAS}$ lead time	40	—	50	—	40	—	50	—	ns	
tRCS	Read command set-up	0	—	0	—	0	—	0	—	ns	
tRCH	Read command hold time	0	—	0	—	0	—	0	—	ns	4
tRRH	Read command hold time refer to $\overline{RAS}$	10	—	10	—	10	—	10	—	ns	4
tWCH	Write command hold time	15	—	20	—	15	—	20	—	ns	
tWCR	Write command hold time ref to $\overline{RAS}$	60	—	75	—	60	—	75	—	ns	
tWP	Write command pulse width	15	—	20	—	15	—	20	—	ns	
tRWL	Write command to $\overline{RAS}$ lead time	20	—	25	—	20	—	25	—	ns	
tCWL	Write command to $\overline{CAS}$ lead time	20	—	25	—	20	—	25	—	ns	
tDS	Date set-up time	0	—	0	—	0	—	0	—	ns	5
tDH	Date hold time	15	—	20	—	15	—	20	—	ns	5
tDHR	Date hold time referenced to $\overline{RAS}$	60	—	75	—	60	—	75	—	ns	
tREF	Refresh time	—	8	—	8	—	8	—	8	ns	
tWCS	Write command set-up time	0	—	0	—	0	—	0	—	ns	6
tCSR	$\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	10	—	10	—	10	—	10	—	ns	
tCHR	$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	30	—	30	—	30	—	30	—	ns	
tRPC	$\overline{RAS}$ to $\overline{CAS}$ precharge time	10	—	10	—	10	—	10	—	ns	
tCPN	$\overline{CAS}$ precharger time	10	—	15	—	10	—	15	—	ns	

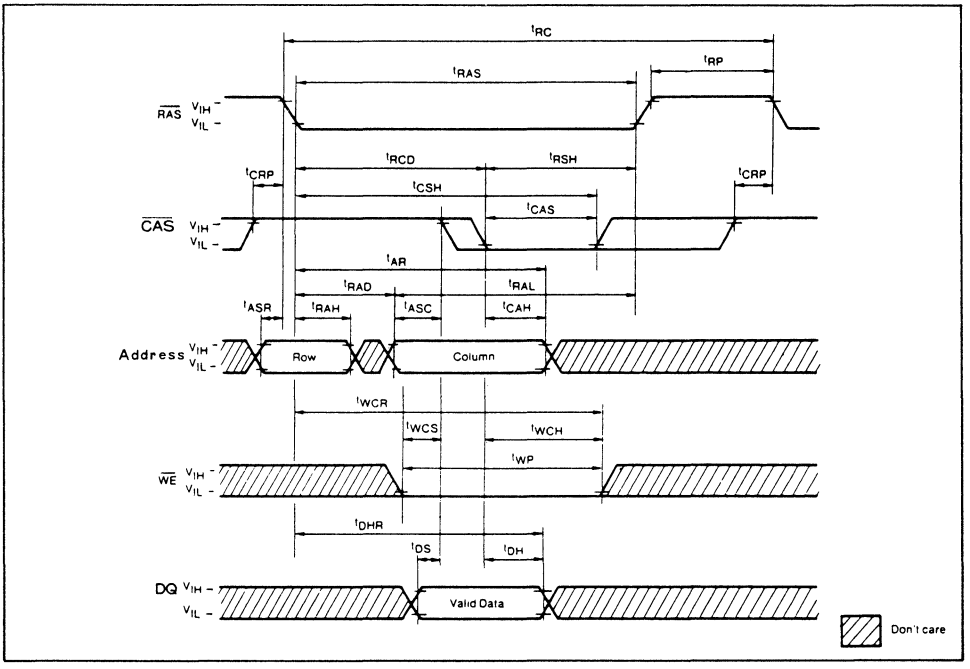
NOTES:

1) AC measurements assume tT = 5ns.
2) Measured with a load equivalent to 2 TTL loads and 100pf.
3) tOFF (max defines the time at which the output achieves an open circuit condition.
4) Either tRCH or tRRH must be satisfied for a read cycle.
5) These parameters are referenced to $\overline{CAS}$ leading edge.
6) tWCS is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If tWCS > tWACS (min), the cycle is an early write cycle and the data out pun will remain an open circuit (Hi-Z)
7) Operation within the tRCS (max) limit, insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only: if tRCD is greater than the specified tRCD (max) limit, them access time is controlled by tCAC.
8) Operation within the tRAD (max) limit, insures that tRAC (max) can be met. tRAD (max) is specified as a reference point only: if tRAD is greater than the specified tRAD (max) limit, them access time is controlled by tAA.

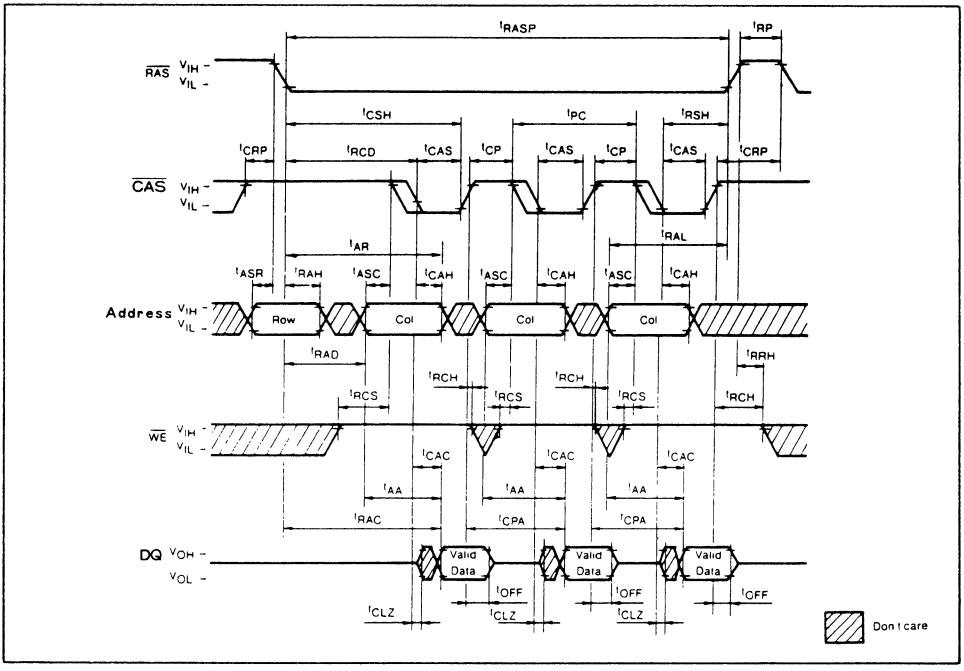
● READ CYCLE



● WRITE CYCLE (EARLY WRITE)



● FAST PAGE MODE READ CYCLE



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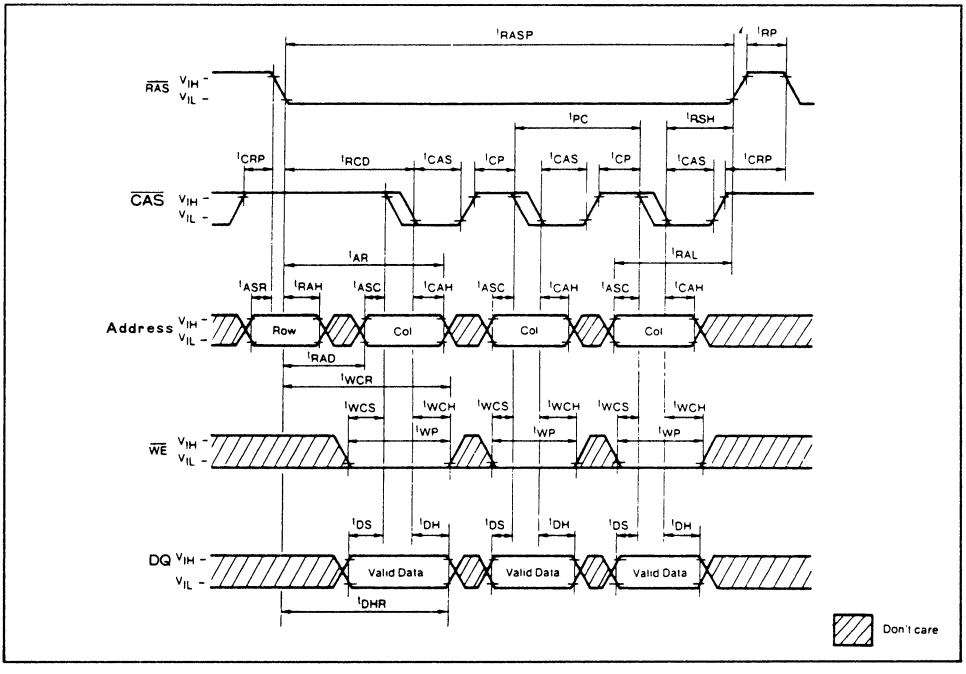
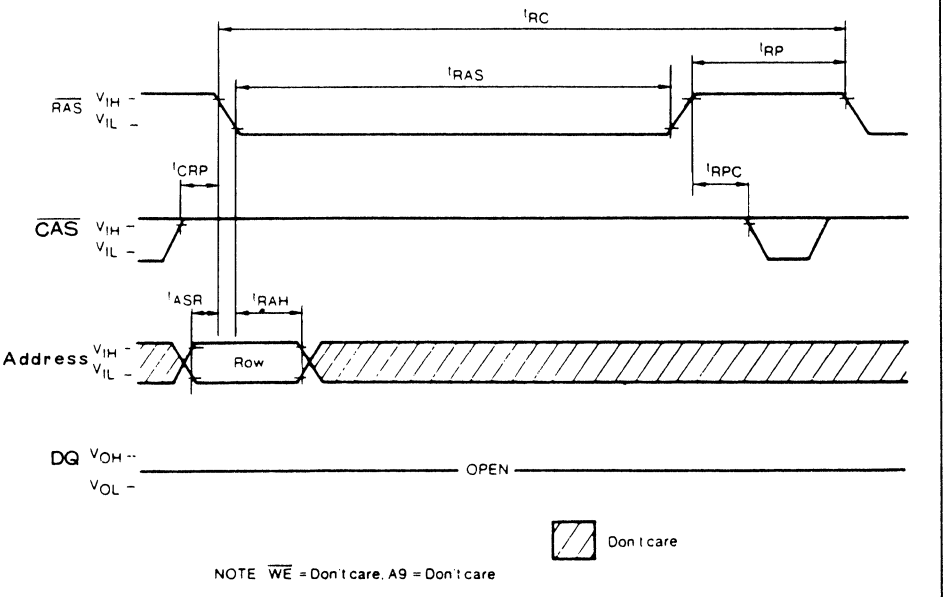
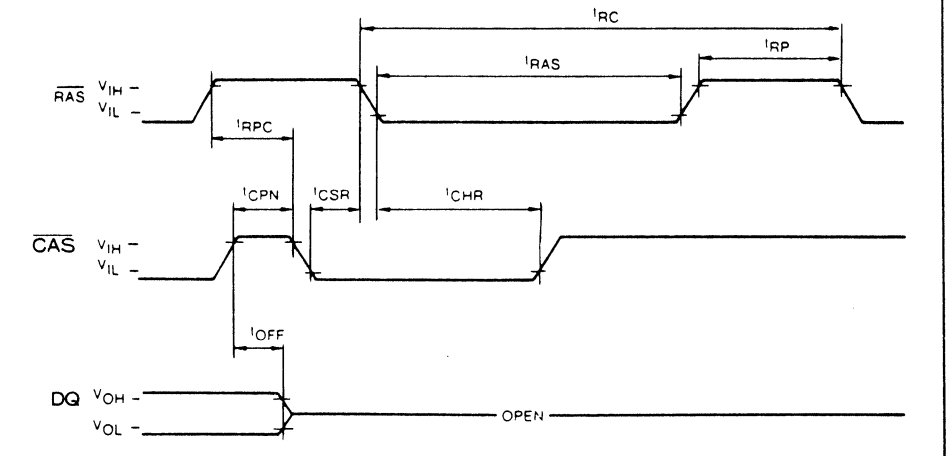


● $\overline{RAS}$ ONLY REFRESH CYCLE



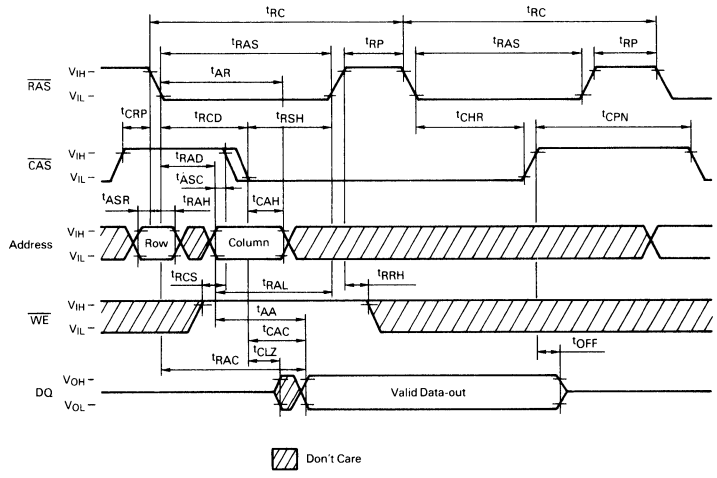
NOTE $\overline{WE}$ = Don't care, A9 = Don't care

● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

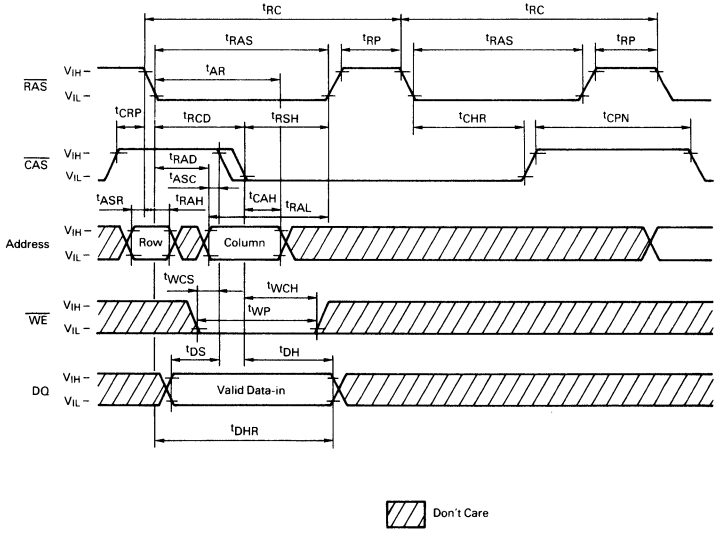


NOTE: $\overline{WE}$ = Don't care, A0 ~ A9 = Don't care

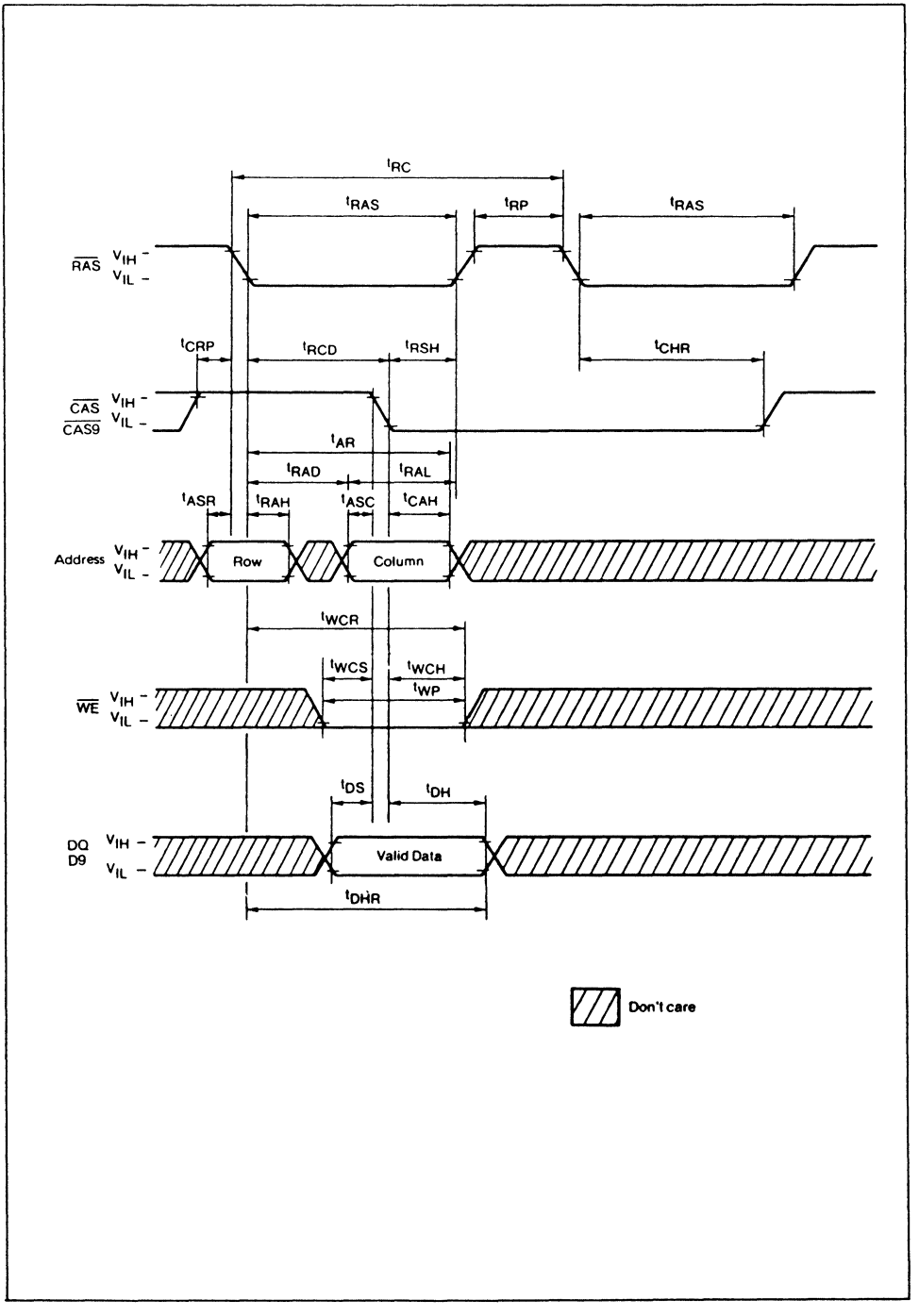
● HIDDEN REFRESH READ CYCLE



● HIDDEN REFRESH WRITE CYCLE



HIDDEN REFRESH WRITE CYCLE



MSC2321A-XXYS18

524, 288 WORD BY 36 BIT DYNAMIC RAM MODULE

GENERAL DESCRIPTION

The Oki MSC2321A-XXYS18 is a fully decoded, 524,288 words × 32 bit CMOS dynamic random access memory composed of sixteen 1 Mb DRAMs in SOJ (MSM514256AJS) and eight 256 Kb drams in SOJ (MSM51256JS). The mounting of twenty-four SOJs together with twenty-four 0.2 μF decoupling capacitors on a 72 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2321A-XXYS18 are quite same as the original MSM511000AJS; each timing requirements are noncritical, and power supply tolerance is very wide.

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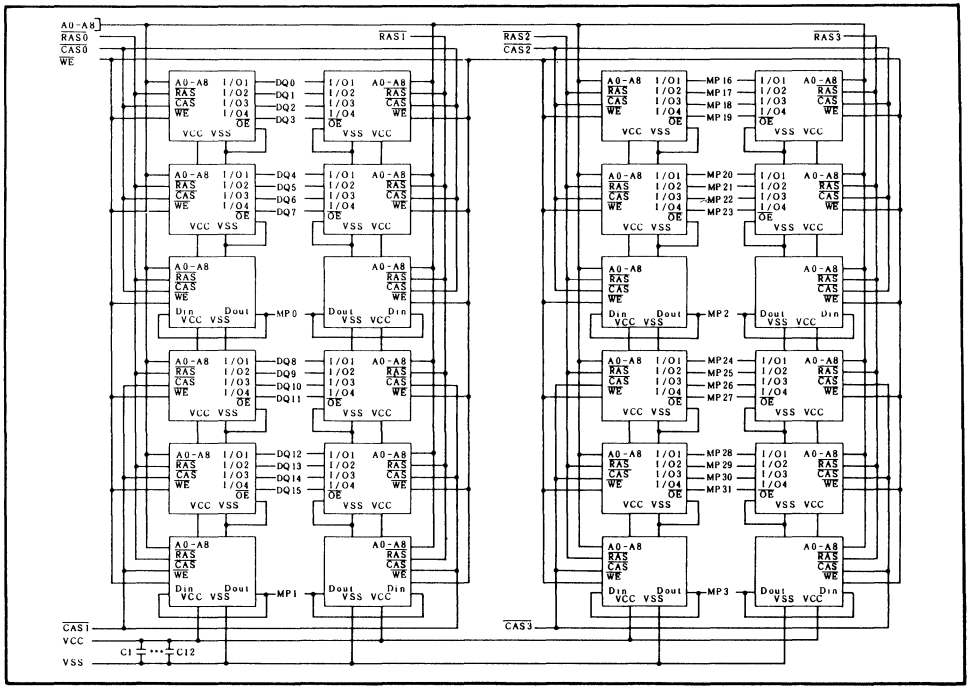
FEATURES

- 524,288 word × 36 bit Organization
- Single +5V Supply (5 % Tolerance)
- Refresh Period ... 8ms (512 cycles)
- All Inputs, Outputs, Clocks
  Fully TTL compatible
- JEDEC Compatible Dimensions and pinout.
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, hidden refresh, and fast page mode capability
- Access Time;
  80ns max. (MSC2321A-8A/80 YS18)
  100ns max. (MSC2321A-1A/10YS18)
- Low Power Dissipation;
  4568mW max. (MSC2321A-8A/80 YS18)
  3938mW max. (MSC2321A-1A/10YS18)
- Operating Temperature ... 0°C to 70°C
- Fast access and cycle times

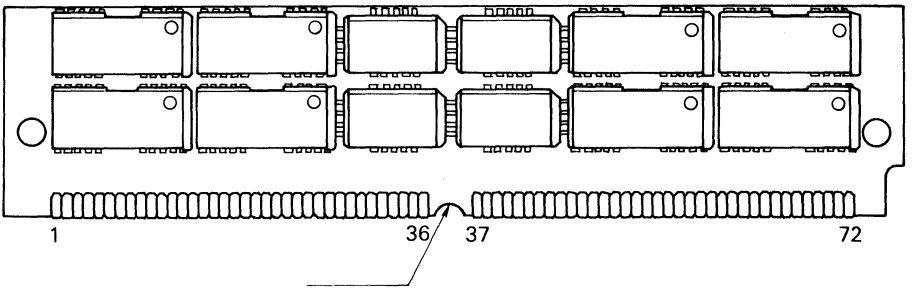
FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT

MSC2321A-XXYS18

BOTTOM



Pinout Assignments

Pin No.	Assign	Pin No.	Assign	Pin No.	Assign	Pin No.	Assign	Pin No.	Assign	Pin No.	Assign		
											100 ns	80 ns	70 ns
1	V_{SS}	13	A1	25	DQ22	37	MP1	49	DQ8	61	DQ13	–	–
2	DQ0	14	A2	26	DQ7	38	MP3	50	DQ24	62	DQ30	–	–
3	DQ16	15	A3	27	DQ23	39	V_{SS}	51	DQ9	63	DQ14	–	–
4	DQ1	16	A4	28	A7	40	$\overline{CAS0}$	52	DQ25	64	DQ31	–	–
5	DQ17	17	A5	29	NC	41	$\overline{CAS2}$	53	DQ10	65	DQ15	–	–
6	DQ2	18	A6	30	V_{CC}	42	$\overline{CAS3}$	54	DQ26	66	NC	–	–
7	DQ18	19	NC	31	A8	43	$\overline{CAS1}$	55	DQ11	67	NC	NC	NC
8	DQ3	20	DQ4	32	NC	44	$\overline{RAS0}$	56	DQ27	68	V_{SS}	V_{SS}	V_{SS}
9	DQ19	21	DQ20	33	$\overline{RAS3}$	45	$\overline{RAS1}$	57	DQ12	69	NC	V_{SS}	NC
10	V_{CC}	22	DQ5	34	$\overline{RAS2}$	46	NC	58	DQ28	70	NC	V_{SS}	V_{SS}
11	NC	23	DQ21	35	MP2	47	WE	59	V_{CC}	71	NC	–	–
12	A0	24	DQ6	36	MPO	48	NC	60	DQ29	72	V_{SS}	–	–

Note: V_{CC} is source, V_{SS} is ground and NC is no connection.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−40 to +125	°C
Power dissipation	P_D	24	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.75	5.0	5.25	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSC2321A-8AYS18		MSC2321A-1AYS18		MSC2321A-80YS18		MSC2321A-10YS18		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current average power supply ($\overline{RAS}$, $\overline{CAS}$ Address cycling)	ICC1	—	870	—	750	—	870	—	750	mA
Standby current power supply standby current	ICC2	—	60	—	60	—	60	—	60	mA
$\overline{RAS}$ only refresh current ($\overline{RAS}$ only mode, $\overline{RAS}$ cycling)	ICC3	—	870	—	750	—	870	—	750	mA
Fast page mode current	ICC4	—	670	—	650	—	710	—	650	mA
Standby current	ICC5	—	36	—	36	—	36	—	36	mA
$\overline{CAS}$ before $\overline{RAS}$ refresh current	ICC6	—	870	—	750	—	870	—	750	mA
Input leakage current	II(L)	-240	240	-240	240	-240	240	-240	240	μA
Output leakage current dout disagled	IO(L)	-20	20	-20	20	-20	20	-20	20	μA
Output high level	IOH	2.4	—	2.4	—	2.4	—	2.4	—	mA
Output low level	VOL	—	0.4	—	0.4	—	0.4	—	0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(V_{CC} = 5 Volts ± 5%, f = 1MHz, Tc = 0 ~ 70°C)

Symbol	Parameter	Min.	Max.	Unit
C_{I_1}	Input Capacitance (A_0 ~A_8)	—	161	pF
C_{I_2}	Input Capacitance ($\overline{W}$)	—	193	pF
C_{I_3}	Input Capacitance ($\overline{RAS0}$, $\overline{RAS3}$)	—	62	pF
C_{I_4}	Input Capacitance ($\overline{CAS0}$ — $\overline{CAS3}$)	—	62	pF
CDQ_1	I/O Cap (DQ0 — DQ31)	—	29	pF
CDQ_2	I/O Cap (MP0 — MP3)	—	39	pF

NOTES:

1) AC measurements assume tT = 5ns.

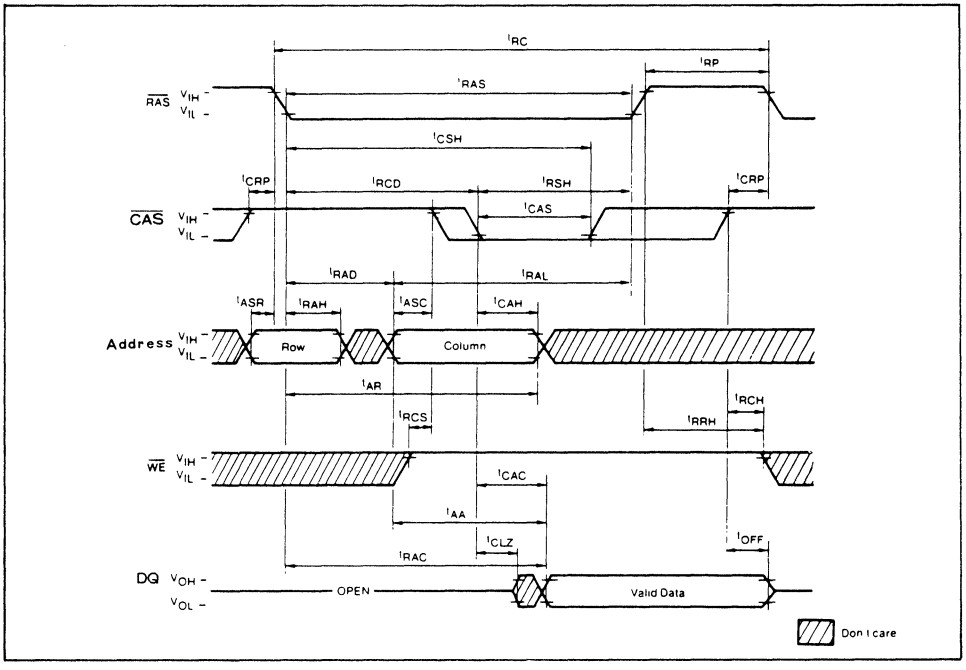
Electrical Characteristics and Recommended AC Operating Conditions

Symbol	Parameter	MSC2321A-8AYS18		MSC2321A-1AYS18		MSC2321A-80YS18		MSC2321A-10YS18		Units	Notes
		MIN.	MAX	MIN.	MAX	MIN.	MAX	MIN.	MAX		
tRC	Random read or write cycle time	160	—	190	—	160	—	190	—	ns	
tPC	Fast page mode cycle time	55	—	55	—	50	—	55	—	ns	
tRAC	Access time from $\overline{RAS}$	—	80	—	100	—	60	—	100	ns	2, 7
tCAC	Access time from $\overline{CAS}$	—	25	—	30	—	20	—	25	ns	2, 7
tAA	Access time from Column address	—	40	—	50	—	40	—	50	ns	2, 8
tCPA	Access time from $\overline{CAS}$ procharge	—	50	—	50	—	45	—	50	ns	2
tCLZ	$\overline{CAS}$ to output in Lo-Z	—	0	—	0	—	0	—	0	ns	2
tOFF	Output buffer turn-off delay	0	20	0	20	0	20	0	20	ns	3
tT	Transition time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	1
tRP	$\overline{RAS}$ procharge time	70	—	80	—	70	—	80	—	ns	
tRAS	$\overline{RAS}$ pulse width	80	10,000	100	10,000	80	10,000	100	10,000	ns	
tRASP	$\overline{RAS}$ pulse width (Fast page mode)	80	100,000	100	100,000	80	100,000	100	100,000	ns	
tRSH	$\overline{RAS}$ hold time	25	—	30	—	20	—	25	—	ns	
tCSH	$\overline{CAS}$ hold time	80	—	100	—	80	—	100	—	ns	
tCAS	$\overline{CAS}$ pulse width	25	10,000	30	10,000	20	10,000	25	10,000	ns	
tRCD	$\overline{RAS}$ to $\overline{CAS}$ delay time	25	55	25	70	22	60	25	75	ns	7
tRAD	$\overline{RAS}$ to column address delay time	20	40	20	50	17	40	20	50	ns	8
tCRP	$\overline{CAS}$ to $\overline{RAS}$ precharge time	10	—	10	—	10	—	10	—	ns	
tCP	$\overline{CAS}$ precharge time (Fast page mode)	10	—	10	—	10	—	10	—	ns	
tASR	Row address set-up time	0	—	0	—	0	—	0	—	ns	
tRAH	Row address hold time	15	—	15	—	12	—	15	—	ns	
tASC	Column address set-up time	0	—	0	—	0	—	0	—	ns	
tCAH	Column address hold time	15	—	20	—	15	—	20	—	ns	
tAR	Column address hold time ref to $\overline{RAS}$	60	—	75	—	60	—	75	—	ns	
tRAL	Column address to $\overline{RAS}$ lead time	40	—	50	—	40	—	50	—	ns	
tRCS	Read command set-up	0	—	0	—	0	—	0	—	ns	
tRCH	Read command hold time	0	—	0	—	0	—	0	—	ns	4
tRRH	Read command hold time refer to $\overline{RAS}$	10	—	10	—	10	—	10	—	ns	4
tWCH	Write command hold time	15	—	20	—	15	—	20	—	ns	
tWCR	Write command hold time ref to $\overline{RAS}$	60	—	75	—	60	—	75	—	ns	
tWP	Write command pulse width	15	—	20	—	15	—	20	—	ns	
tRWL	Write command to $\overline{RAS}$ lead time	20	—	25	—	20	—	25	—	ns	
tCWL	Write command to $\overline{CAS}$ lead time	20	—	25	—	20	—	25	—	ns	
tDS	Date set-up time	0	—	0	—	0	—	0	—	ns	5
tDH	Date hold time	15	—	20	—	15	—	20	—	ns	5
tDHR	Date hold time referenced to $\overline{RAS}$	60	—	75	—	60	—	75	—	ns	
tREF	Refresh time	—	8	—	8	—	8	—	8	ns	
tWCS	Write command set-up time	0	—	0	—	0	—	0	—	ns	6
tCSR	$\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	10	—	10	—	10	—	10	—	ns	
tCHR	$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$ cycle)	30	—	30	—	30	—	30	—	ns	
tRPC	$\overline{RAS}$ to $\overline{CAS}$ precharge time	10	—	10	—	10	—	10	—	ns	
tCPN	$\overline{CAS}$ precharger time	10	—	15	—	10	—	15	—	ns	

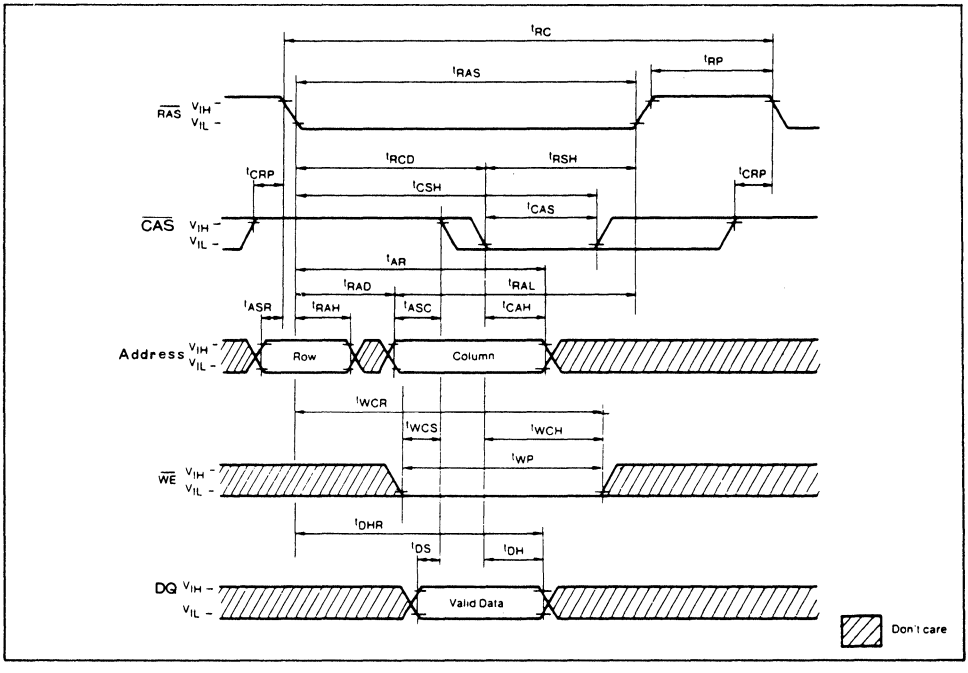
NOTES:

1) AC measurements assume tT = 5ns.
2) Measured with a load equivalent to 2 TTL loads and 100pf.
3) tOFF (max defines the time at which the output achieves an open circuit condition.
4) Either tRCH or tRRH must be satisfied for a read cycle.
5) These parameters are referenced to $\overline{CAS}$ leading edge.
6) tWCS is not a restrictive operating parameter. This is included in the data sheet as electrical characteristic only. If tWCS > tWACS (min), the cycle is an early write cycle and the data out pun will remain an open circuit (Hi-Z)
7) Operation within the tRCS (max) limit, insures that tRAC (max) can be met. tRCD (max) is specified as a reference point only: if tRCD is greater than the specified tRCD (max) limit, them access time is controlled by tCAC.
8) Operation within the tRAD (max) limit, insures that tRAC (max) can be met. tRAD (max) is specified as a reference point only: if tRAD is greater than the specified tRAD (max) limit, them access time is controlled by tAA.

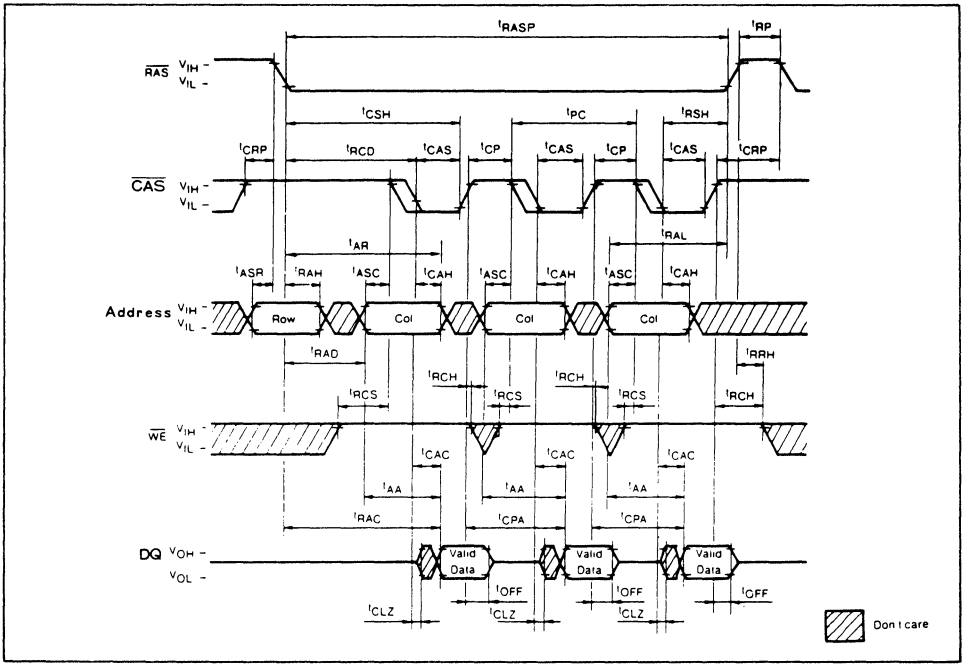
● READ CYCLE



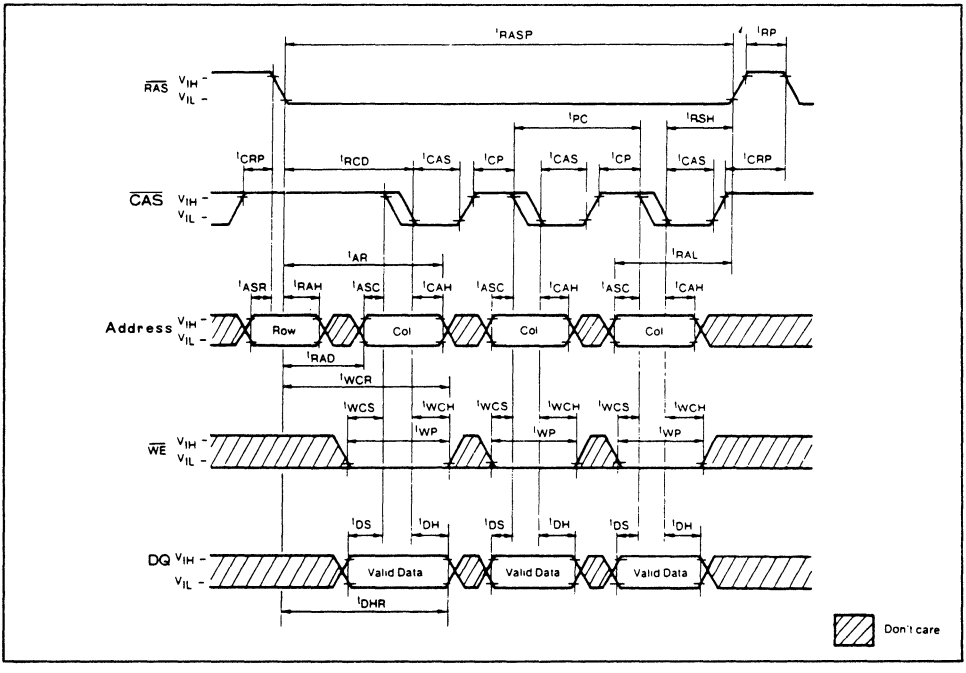
● WRITE CYCLE (EARLY WRITE)



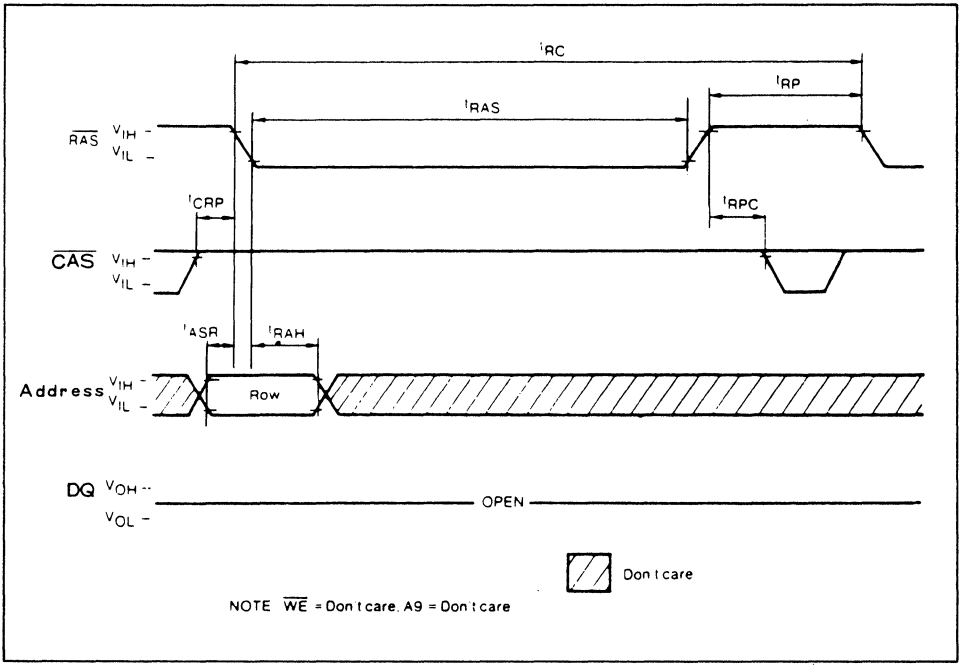
● FAST PAGE MODE READ CYCLE



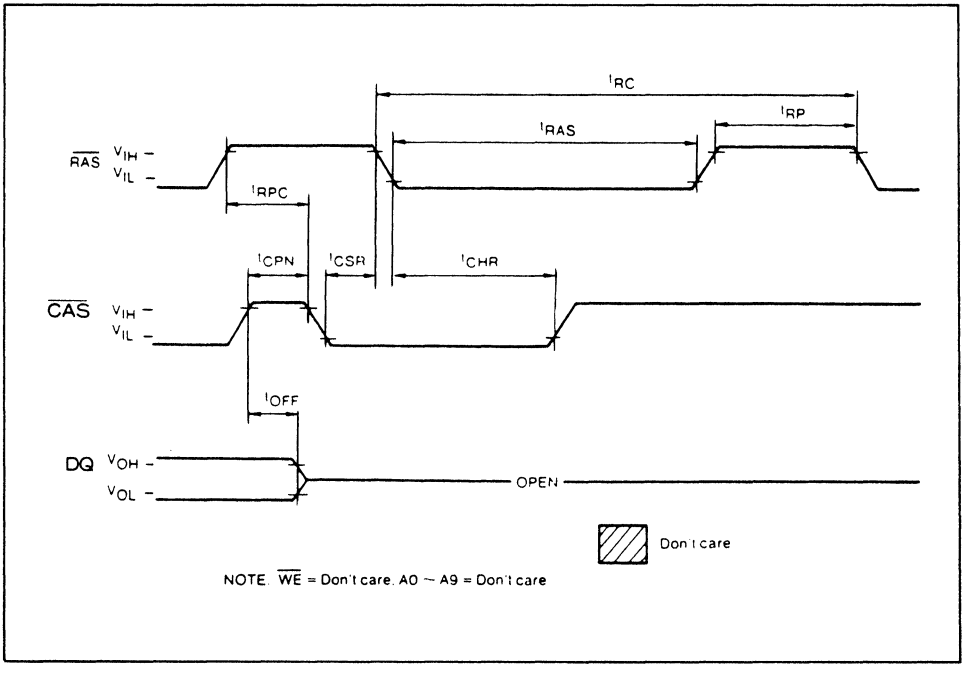
● FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



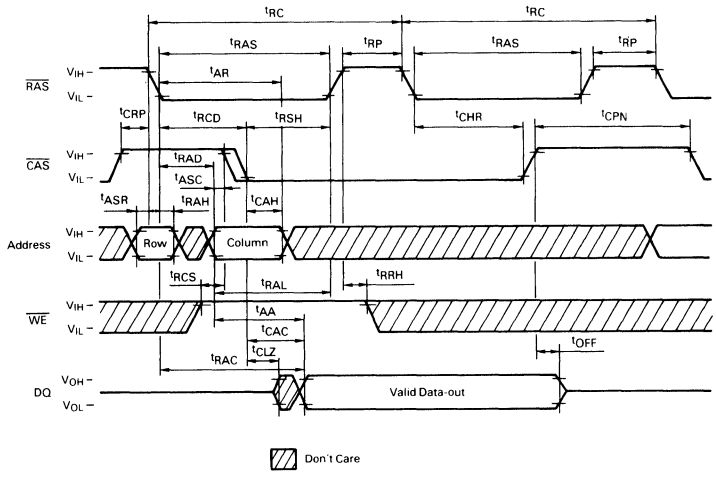
● $\overline{RAS}$ ONLY REFRESH CYCLE



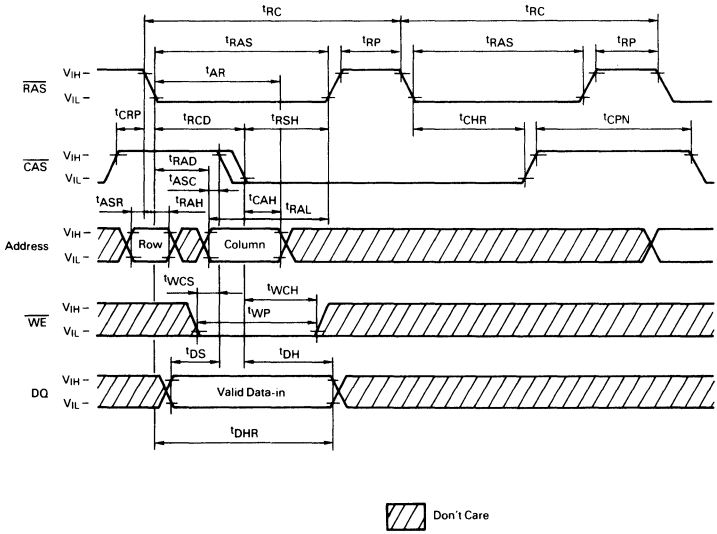
● $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



● HIDDEN REFRESH READ CYCLE



● HIDDEN REFRESH WRITE CYCLE



MSC2328A-XX YS2/KS2

262,144 BY 8 BIT DYNAMIC RAM MODULE

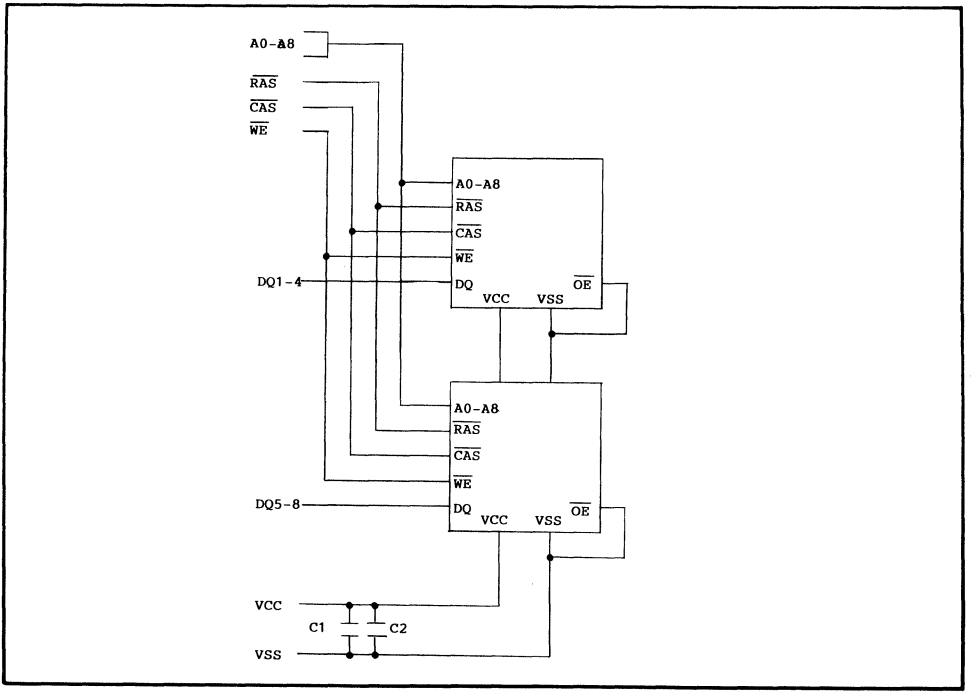
GENERAL DESCRIPTION

The Oki MSC2328A-XX YS2/KS2 is a fully decoded, 262,144 words×8 bit CMOS dynamic random access memory composed of two 1Mb DRAMs in SOJ (MSM514256AJS). The mounting of two SOJs together with two 0.2 μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2328A-XX YS2/KS2are quite same as the original MSM514256A JS; each timing requirements are noncritical, and power supply tolerance is very wide.

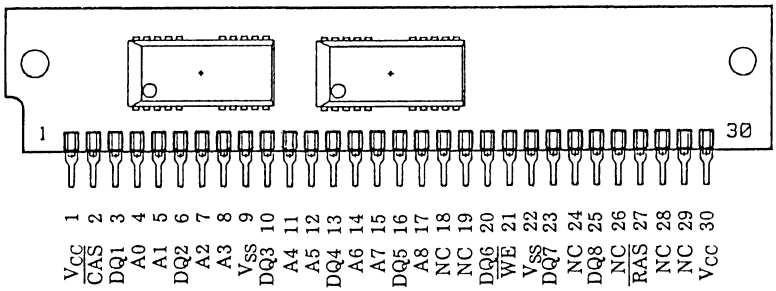
FEATURES

- 262,144 word × 8 bit Organization
- Single =5V Supply (10% Tolerance)
- 30-Pin Socket Insertable Module
- Refresh Period ... 8ms (512 cycles)
- All Inputs, Outputs, Clocks
  Fully TTL compatible
- 3-States Outputs
- Common $\overline{CAS}$ Control for two Common Data-In and Data-Out Lines
- Row Access Time;
  80ns max. (MSC2328A-8A/80 YS2/KS2)
  100ns max. (MSC2328A-1A/10 YS2/KS2)
- Low Power Dissipation;
  825mW max. (MSC2328A-8A/80 YS2/KS2)
  715mW max. (MSC2328A-1A/10 YS2/KS2)
- Operating Temperature ... 0°C to 70°C

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	NC
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	NC	28	NC
9	VSS	19	NC	29	NC
10	DQ3	20	DQ6	30	V_{CC}

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	−1 to +7	V
Voltage on V_{CC} supply relative to V_{SS}	V_{CC}	−1 to +7	V
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	−55 to 150	°C
Power dissipation	P_D	2	W
Short circuit output current		50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0°C to +70°C
	V_{SS}	0	0	0	V	
Input High Voltage, all inputs	V_{IH}	2.4	—	6.5	V	
Input Low Voltage, all inputs	V_{IL}	−1.0	—	0.8	V	

4

DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Symbol	MSC2328A-8AYS2/KS2		MSC2328A-1AYS2/KS2		MSC2328A-80YS2/KS2		MSC2328A-10YS2/KS2		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Operating Current* Average power supply current ($\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = min.)	I_{CC1}	—	150	—	130	—	150	—	130	mA
Standby Current* Power supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2} (TTL)	—	4	—	4	—	4	—	4	mA
	I_{CC2} (MOS)	—	2	—	2	—	2	—	2	mA
REfresh Current 1* Average power supply current ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$; t_{RC} =min.)	I_{CC3}	—	150	—	130	—	150	—	130	mA
Refresh Current 2* Average power supply current (CAS before RAS; t_{RC} = min)	I_{CC6}	—	150	—	130	—	150	—	130	mA
Page Mode Current* Average power supply current ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling; t_{PC} =min.)	I_{CC7}	—	120	—	120	—	130	—	120	mA
Input Leakage Current Input leakage current, any input ($0V \leq V_{IN} \leq 5.5V$, all other pins not under test = 0V)	I_{LI}	−20	20	−20	20	−20	20	−20	20	μA
Output Leakage Current (Data out is disabled, $0V \leq V_{OUT} \leq 5.5V$)	I_{LO}	−10	10	−10	10	−10	10	−10	10	μA
Output Levels Output high voltage (I_{OH} = −5mA)	V_{OH}	2.4	—	2.4	—	2.4	—	2.4	—	V
Output low voltage (I_{OL} = 4.2mA)	V_{OL}	—	0.4	—	0.4	—	0.4	—	0.4	V

Note*: I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance ($A_0 \sim A_8$)	C_{IN1}	30	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	30	pF
Data Input/Output Capacitance (DQ)	C_{DQ}	20	pF

Capacitance measured with Boonton Meter.

AC CHARACTERISTICS

(V_{CC} = 5V ±10%, Ta = 0 to +70°C) Note 1, 2, 3

Parameter	Symbol	MSC2328A-8AYS2/KS2		MSC2328A-1AYS2/ KS2		MSC2328A-80YS2/KS2		MSC2328A-10YS2/KS2		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Refresh period	t_{REF}	—	8	—	8	—	8	—	8	ms	
Random read or write cycle time	t_{RC}	160	—	190	—	160	—	190	—	ns	
Fast page mode cycle time	t_{PC}	55	—	55	—	50	—	55	—	ns	
Access time from $\overline{RAS}$	t_{RAC}	—	80	—	100	—	80	—	100	ns	4,5,6
Access time from $\overline{CAS}$	t_{CAC}	—	25	—	30	—	20	—	25	ns	4,5
Access time from column address	t_{AA}	—	40	—	50	—	40	—	50	ns	4,6
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	50	—	50	—	45	—	50	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	—	0	—	0	—	0	—	n_s	4
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	20	0	20	ns	
Transition time	t_T	3	50	3	50	3	50	3	50	ns	3
$\overline{RAS}$ precharge time	t_{RP}	70	—	80	—	70	—	80	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10000	100	10000	80	10000	100	10000	ns	
$\overline{RAS}$ pulse width (Fast page mode cycle only)	t_{RASP}	80	100000	100	100000	80	100000	100	100000	ns	
$\overline{RAS}$ hold time	t_{RSH}	25	—	30	—	20	—	25	—	ns	
$\overline{CAS}$ precharge time (Fast page mode cycle only)	t_{CP}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ pulse width	t_{CAS}	25	10000	30	10000	20	10000	25	10000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	—	100	—	80	—	100	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	25	55	25	70	25	60	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	20	40	20	50	17	40	20	50	ns	6
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Row address set-up time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row address hold time	t_{RAH}	15	—	15	—	12	—	15	—	ns	
Column address set-up time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column address hold time	t_{CAH}	15	—	20	—	15	—	20	—	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	—	75	—	60	—	75	—	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	—	50	—	40	—	50	—	ns	

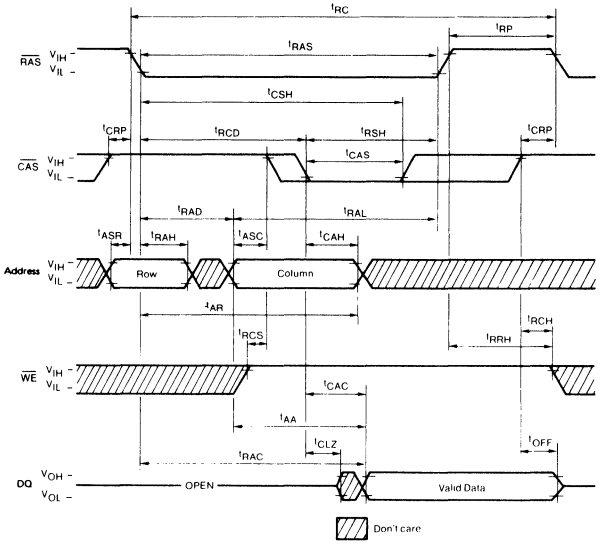
AC CHARACTERISTICS (CONT.)

Parameter	Symbol	MSC2328A-8AYS2/KS2		MSC2328A--1AYS2/ KS2		MSC2328A-80YS2/KS2		MSC2328A-10YS2/KS2		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read command hold time	t_{RCH}	0	—	0	—	0	—	0	—	ns	7
Write command hold time from $\overline{RAS}$	t_{WCR}	60	—	75	—	60	—	75	—	ns	
Write command set-up time	t_{WCS}	0	—	0	—	0	—	0	—	ns	
Write command hold time	t_{WCH}	15	—	20	—	15	—	20	—	ns	
Write command pulse width	t_{WP}	15	—	20	—	15	—	20	—	ns	
Data-in set-up time	t_{DS}	0	—	0	—	0	—	0	—	ns	
Data-in hold time	t_{DH}	15	—	20	—	15	—	20	—	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	—	75	—	60	—	75	—	ns	
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	—	10	—	10	—	10	—	ns	7
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	—	10	—	10	—	10	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	30	—	30	—	30	—	30	—	ns	
$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	t_{RPC}	10	—	10	—	10	—	10	—	ns	
$\overline{CAS}$ precharge time	t_{CPN}	10	—	15	—	10	—	15	—	ns	

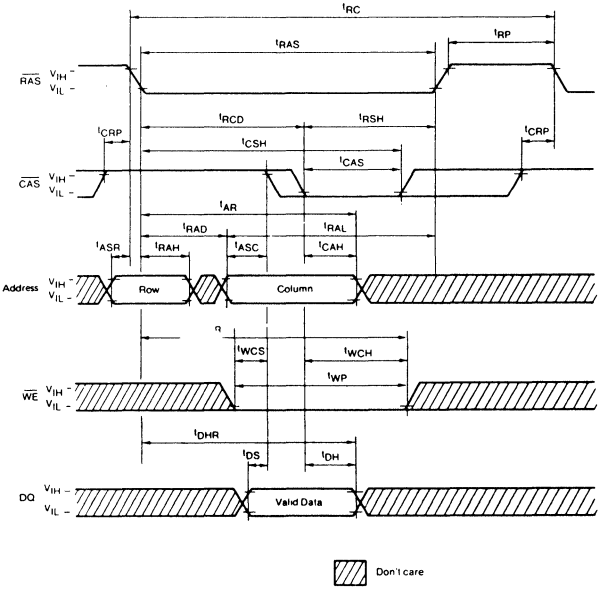
Notes:

1. An initial pause of 100 μs is required after power-up followed by any 8 $\overline{RAS}$ cycles (Example: $\overline{RAS}$ only) before proper device operation is achieved.
2. The AC characteristics assume at t_T = 5 ns.
3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Measured with a load circuit equivalent to 2TTL + 100 pF.
5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.
7. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

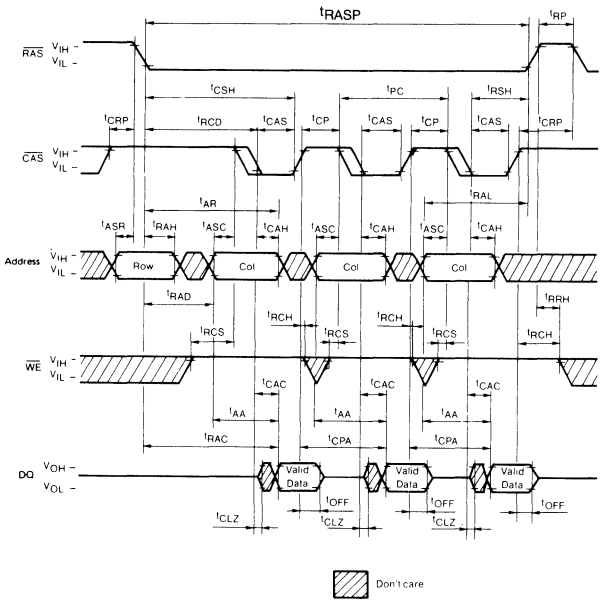
READ CYCLE



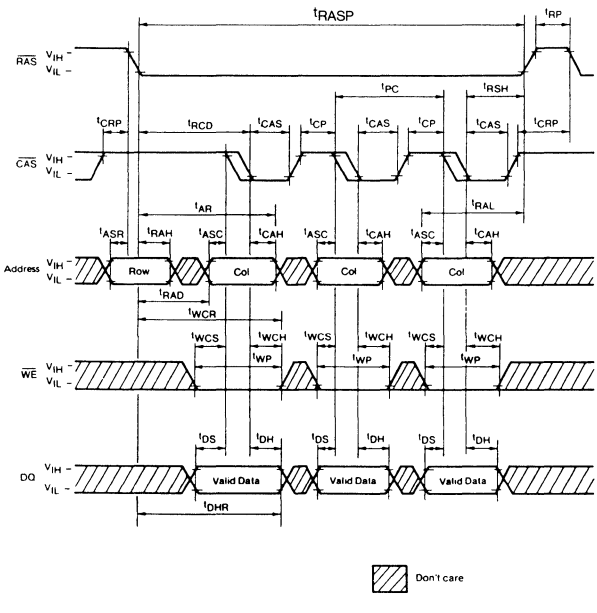
WRITE CYCLE(EARLY WRITE)



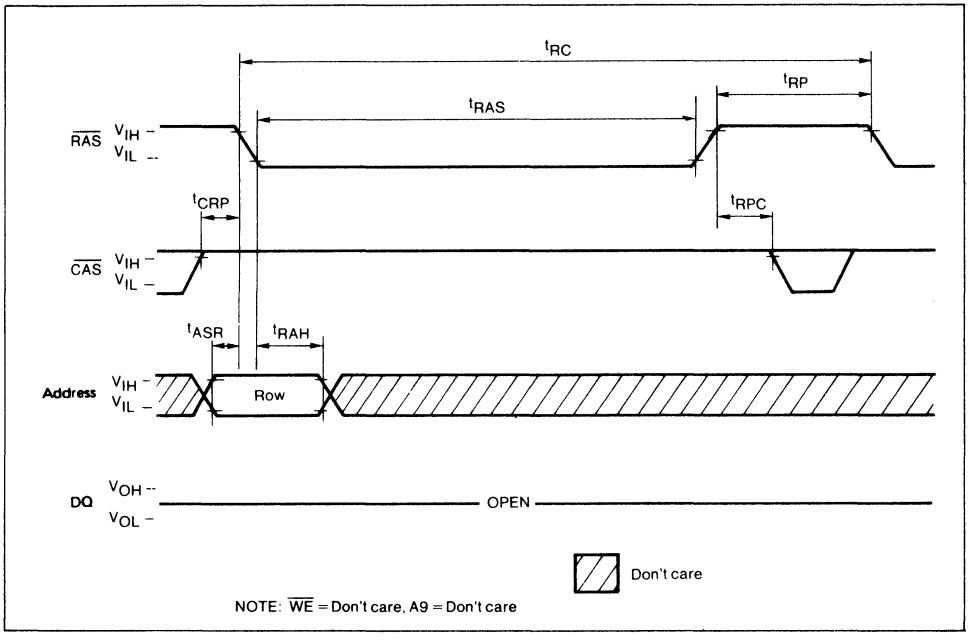
FAST PAGE MODE READ CYCLE



FAST PAGE MODE CYCLE (EARLY WRITE)

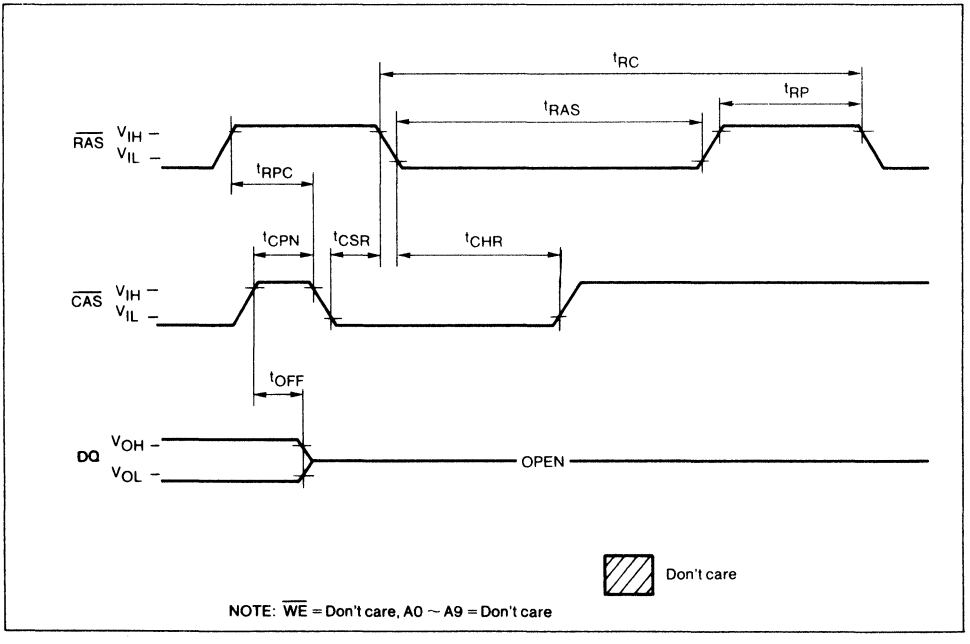


RAS ONLY REFRESH CYCLE



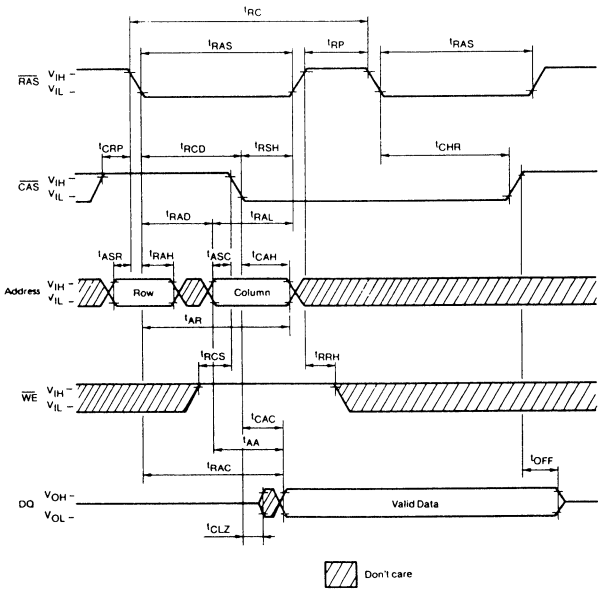
NOTE: $\overline{WE}$ = Don't care, A9 = Don't care

$\overline{CAS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE

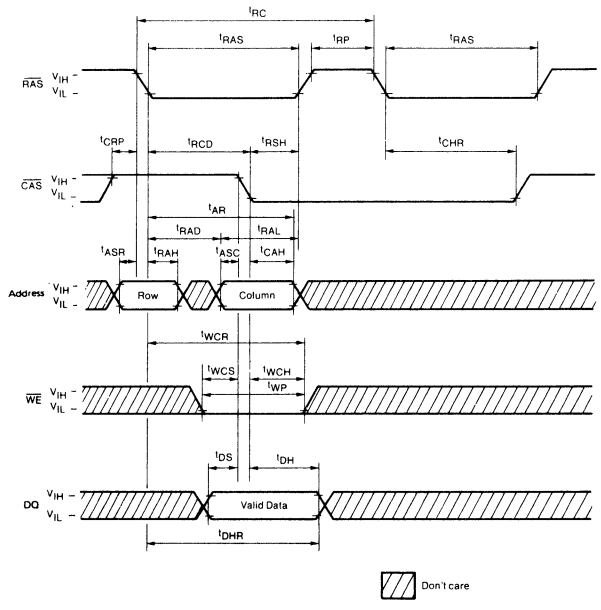


NOTE: $\overline{WE}$ = Don't care, A0 ~ A9 = Don't care

HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE



OKI semiconductor
MSC2340-XXYS9/KS9

4,194,304 Word x 9 Bit DYNAMIC RAM MODULE: FAST PAGE MODE TYPE

GENERAL DESCRIPTION

The Oki MSC2340-XXYS9/KS9 is a fully decoded, 4,194,304 word by 9 bit CMOS dynamic random access memory composed of nine 4Mb DRAMs in SOJ (MSM514100JS). The mounting of nine SOJs together with nine 0.2μF decoupling capacitors on a 30 pin glass epoxy Single-In-Line Package provides any application where high density and large capacity of storage memory are required. The electrical characteristics of the MSC2340-XXYS9/KS9 are quite same as the original MSM514100 JS; each timing requirements are noncritical, and power supply tolerance is very wide.

4

FEATURES

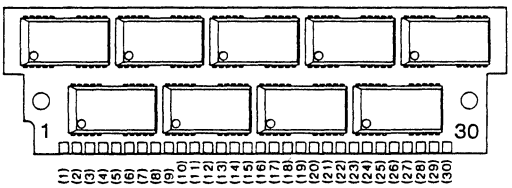
- 4,194,304 word x 9 bit organization
- 30-Pin Socket Insertable Module
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
					Operating (MAX)	Standby (MAX)
	t_{RAC}	t_{AA}	t_{CAC}			
MSC2340-8 YS9/KS9	80 ns	40 ns	20 ns	160 ns	4455 mW	49.5 mW (MOS level)
MSC2340-8A YS9/KS9	80 ns	40 ns	25 ns	160 ns	4455 mW	
MSC2340-10 YS9/KS9	100 ns	50 ns	25 ns	190 ns	3960 mW	

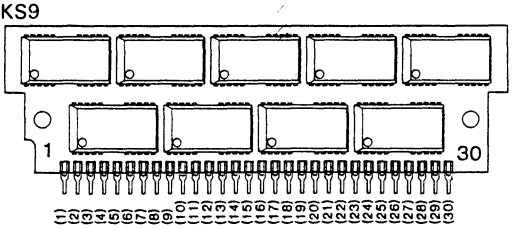
- Single + 5 V supply, ± 10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- Common $\overline{CAS}$ control for eight common Data-in and Data-out lines
- Separate $\overline{CAS}$ control for one separate pair of Data-in and Data-out lines
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Multi bit test mode capability

PIN ASSIGNMENT

MSC2340-XXYS9

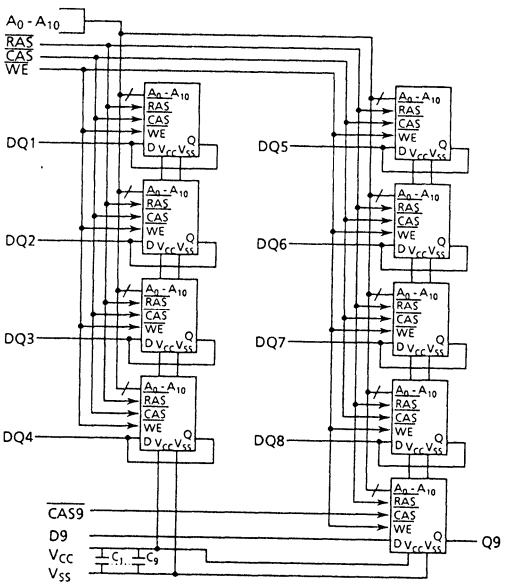


MSC2340-XXKS9



PIN No.	PIN NAME	PIN No.	PIN NAME	PIN No.	PIN NAME
1	V_{CC}	11	A4	21	$\overline{WE}$
2	$\overline{CAS}$	12	A5	22	VSS
3	DQ1	13	DQ4	23	DQ7
4	A0	14	A6	24	NC
5	A1	15	A7	25	DQ8
6	DQ2	16	DQ5	26	Q9
7	A2	17	A8	27	$\overline{RAS}$
8	A3	18	A9	28	$\overline{CAS9}$
9	VSS	19	A10	29	D9
10	DQ3	20	DQ6	30	V_{CC}

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit	Note
Voltage on any pin relative to V_{SS}	VT	Ta = 25 °C	− 1.0 to + 7.0	V	1
Short circuit output current	Ios	Ta = 25 °C	50	mA	1
Power dissipation	P_D	Ta = 25 °C	9	W	1
Operating temperature	Topr	−	0 to + 70	°C	1
Storage temperature	Tstg	−	− 40 to + 125	°C	1

RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to + 70°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	2
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	−	6.5	V	2
Input low voltage	V_{IL}	− 1.0	−	0.8	V	2

Notes: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. All voltages are referenced to V_{SS}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	TYP	MAX	Unit
Input Capacitance (A_0 to A_{10})	C_{IN1}	55	70	pF
Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	C_{IN2}	55	75	pF
Data Input/Output Capacitance (DQ1 to DQ8)	C_{DQ}	12	20	pF
Input Capacitance ($\overline{CAS9}$)	C_{IN3}	7	15	pF
Input Capacitance (D9)	C_{IN4}	7	15	pF
Output Capacitance (Q9)	C_{OUT}	8	15	pF

Capacitance measured with Boonton Meter.

DC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to + 70°C)

Parameter	Symbol	Conditions		MSC2340-8 YS9 / KS9		MSC2340-8A YS9 / KS9		MSC2340-10 YS9 / KS9		Unit	Note
				MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = − 5.0 mA		2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0 V ≤ VI ≤ 6.5V; all other pins not under test = 0 V		90	90	90	90	90	90	µA	
Output leakage current	I_{LO}	DQ1 - 8,Q9 = disable 0 V ≤ VO ≤ 5.5 V		− 10	10	− 10	10	− 10	10	µA	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$, $\overline{CAS9}$ cycling, t_{RC} = min		−	810	−	810	−	720	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$, $\overline{CAS9}$ = V_{IH} DQ1 - 8, Q9 = Hz	TTL	−	18	−	18	−	18	mA	
			MOS	−	9	−	9	−	9		
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$, $\overline{CAS9}$ = V_{IH} t_{RC} = min		−	810	−	810	−	720	mA	1, 2
Power supply current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH} $\overline{CAS}$, $\overline{CAS9}$ = V_{IL} DQ1 - 8, Q9 = enable		−	45	−	45	−	45	mA	1
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CAS}$ before $\overline{RAS}$		−	810	−	810	−	720	mA	1
Average power supply current (Fast page mode)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$, $\overline{CAS9}$ cycling t_{PC} = min		−	720	−	720	−	630	mA	1, 3

Notes: 1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

2. Address can be changed once or less while $\overline{CAS}$ = V_{IH}.

AC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to + 70°C) Note 1, 2, 3, 9, 10

Parameter	Symbol	MSC2340-8 YS9/KS9		MSC2340-8A YS9/KS9		MSC2340-10 YS9/KS9		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	160	–	160	–	190	–	ns	
Fast page mode cycle time	t_{PC}	55	–	55	–	65	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	80	–	100	ns	4. 5
Access time from $\overline{CAS}$	t_{CAC}	–	20	–	25	–	25	ns	4. 5
Access time from column address	t_{AA}	–	40	–	40	–	50	ns	4. 6
Access time from $\overline{CAS}$ precharge	t_{CPA}	–	45	–	45	–	55	ns	4
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	–	0	–	0	–	ns	4
Output buffer turn-off delay time	t_{OFF}	0	20	0	20	0	25	ns	7
Transition time	t_T	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	–	16	–	16	–	16	ms	
$\overline{RAS}$ precharge time	t_{RP}	70	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	80	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	25	–	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	25	10,000	25	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80	–	80	–	100	–	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	22	60	25	55	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	40	20	50	ns	6
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	20	–	ns	
Column address hold time from $\overline{RAS}$	t_{AR}	60	–	60	–	75	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	40	–	50	–	ns	

AC CHARACTERISTICS (Continued)

Parameter	Symbol	MSC2340-8 YS9 / KS9		MSC2340-8A YS 9 / KS9		MSC2340-10 YS9 / KS9		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time	t_{RCH}	0	–	0	–	0	–	ns	8
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	8
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	
Write command hold time	t_{WCH}	15	–	15	–	20	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	60	–	75	–	ns	
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	25	–	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20	–	25	–	25	–	ns	
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	60	–	75	–	ns	
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	20	–	20	–	20	–	ns	
$\overline{CAS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRP}	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CAS}$ before $\overline{RAS}$)	t_{WRH}	20	–	20	–	20	–	ns	
$\overline{RAS}$ to $\overline{WE}$ set-up time (Test mode)	t_{WSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{WE}$ hold time (Test mode)	t_{WHR}	20	–	20	–	20	–	ns	

Notes: 1. An initial pause of 200 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is achieved.
In case of using internal refresh counter, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ initialization cycles is required.

2. The AC characteristics assume t_T = 5 ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2TTL loads and 100pF.

5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

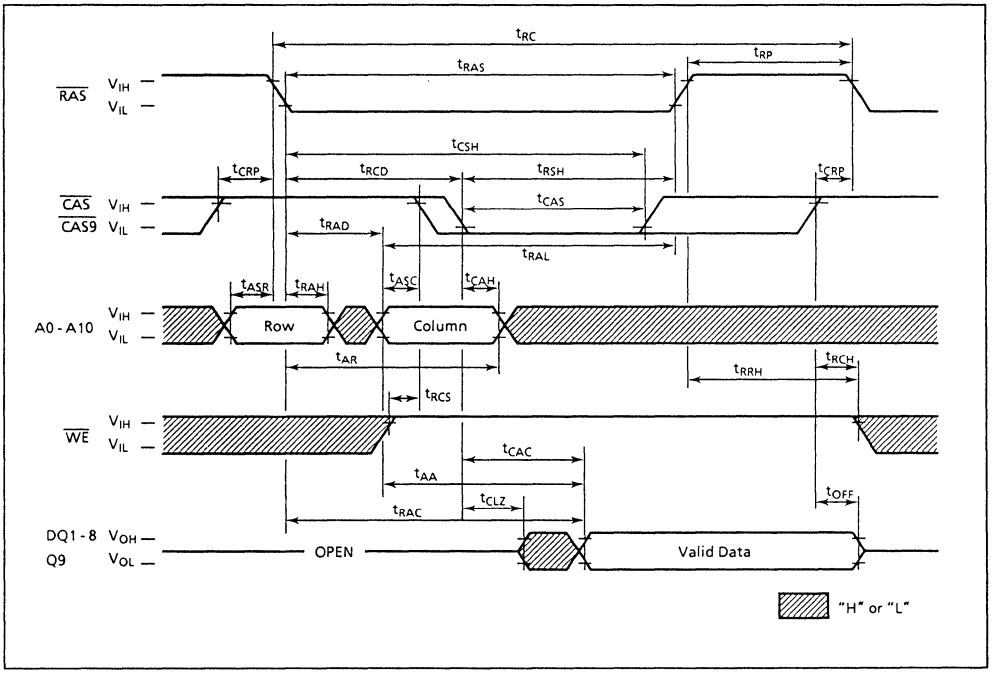
7. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

8. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

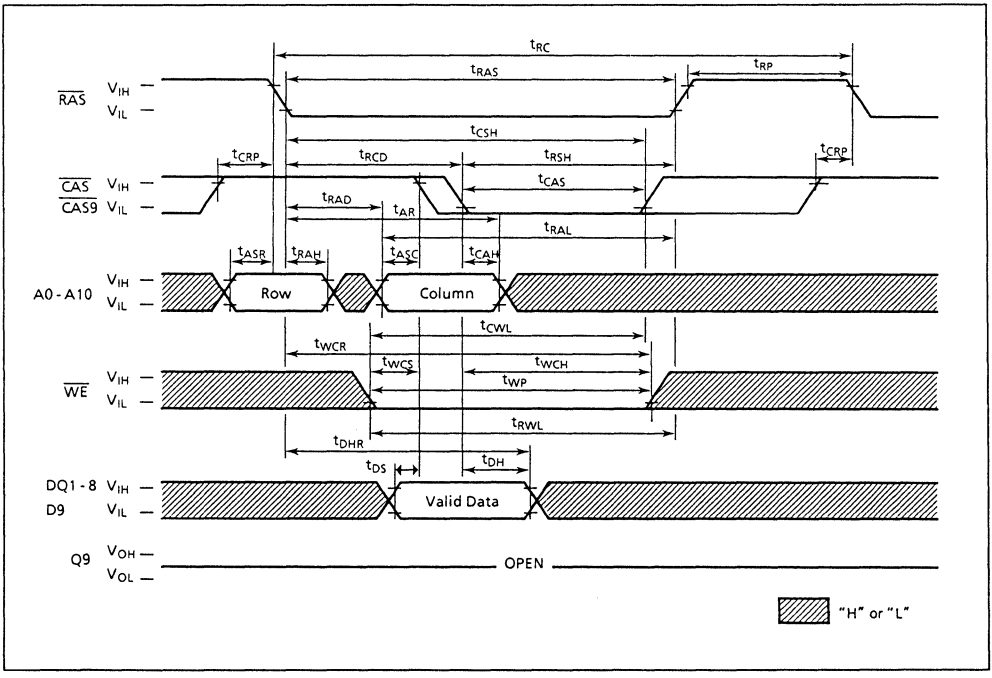
9. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remain in effect until the exit cycle is generated.
The test mode specified in this data sheet is 8-bit parallel test function.
RA10, CA10 and CA0 are not used. In a read cycle, if all internal bits are equal, the data output pin will indicate a high level. If any internal bits are not equal, then data output pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$ only refresh cycle or a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

10. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

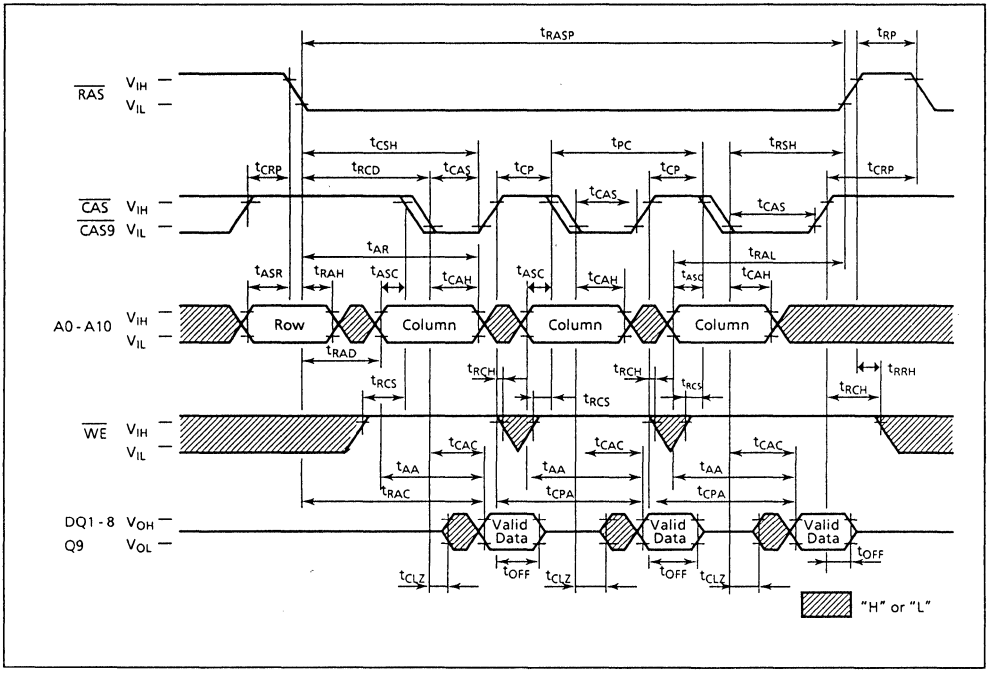
READ CYCLE



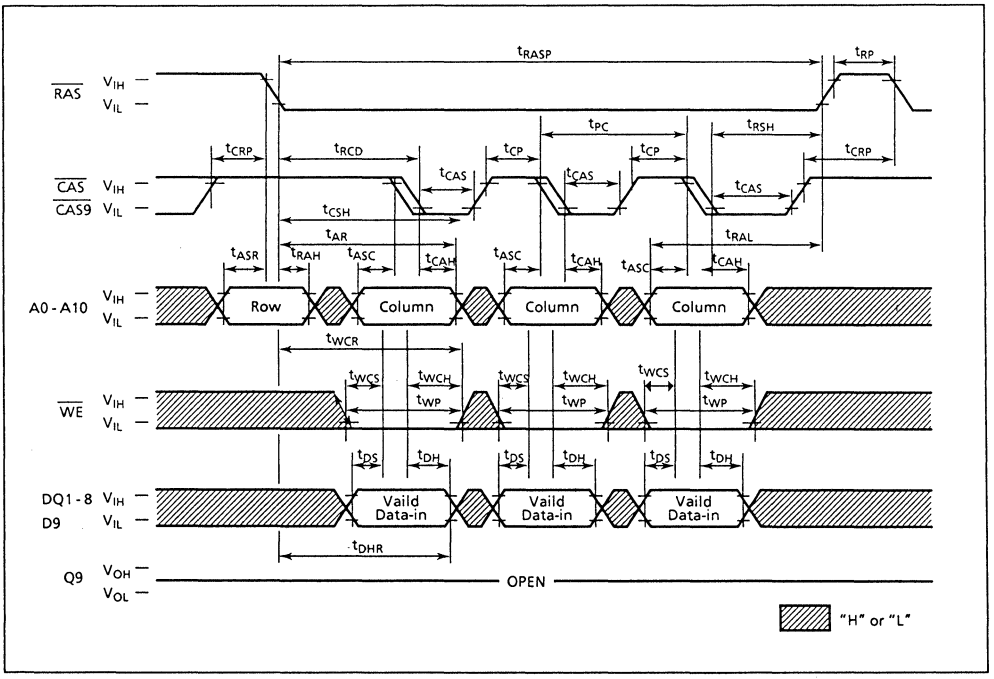
WRITE CYCLE (EARLY WRITE)



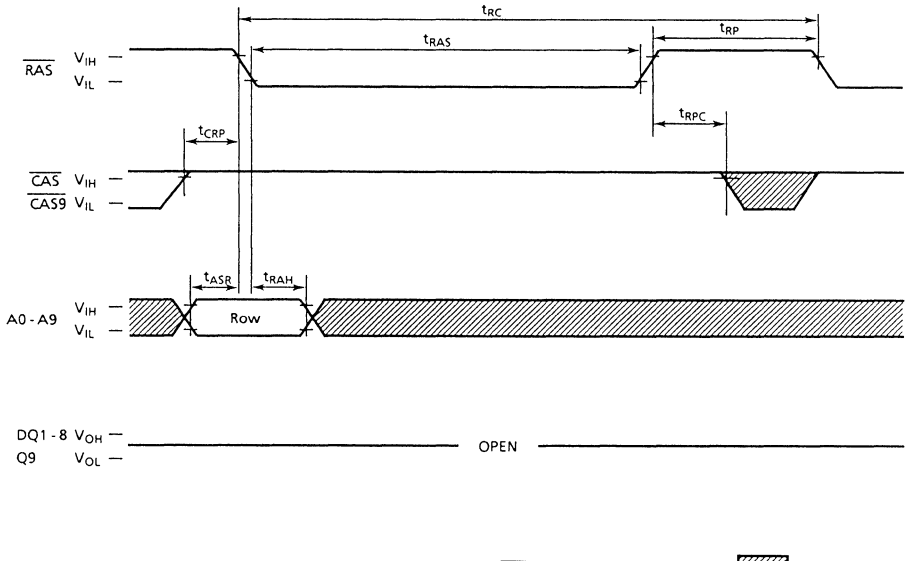
FAST PAGE MODE READ CYCLE



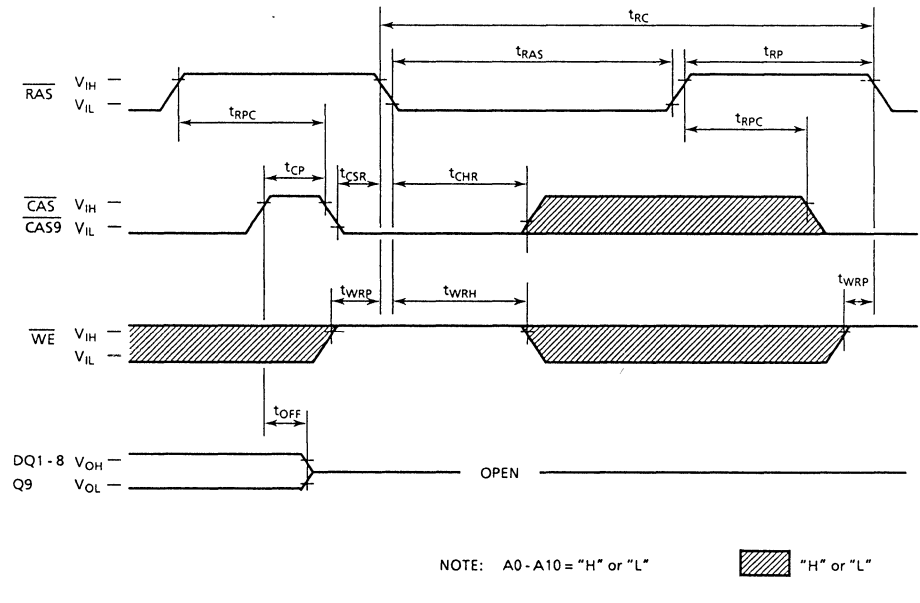
FAST PAGE MODE WRITE CYCLE (EARLY WRITE)



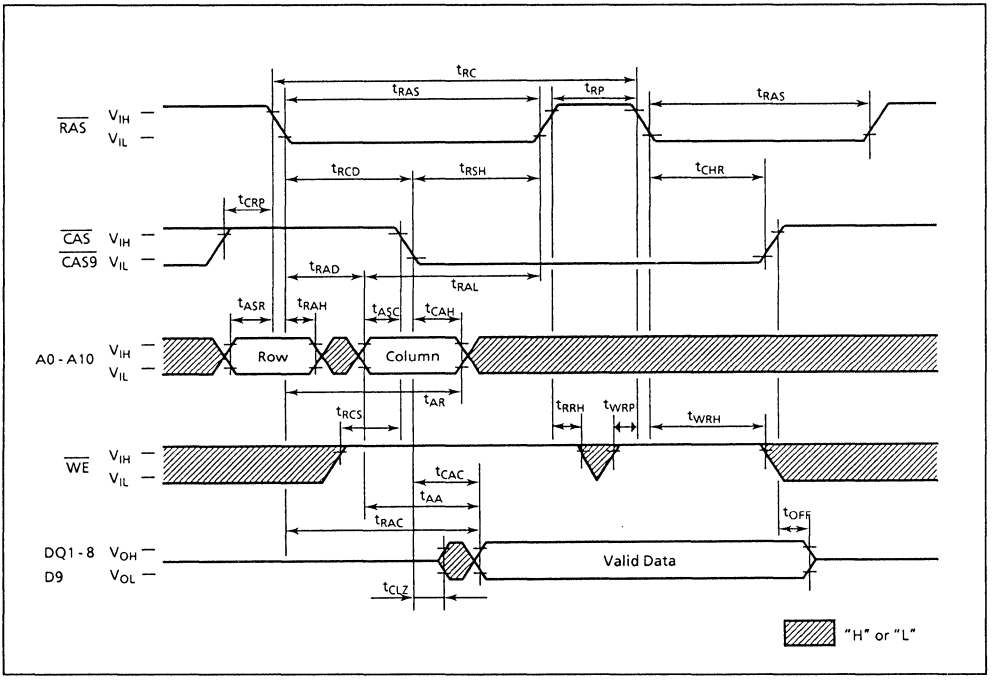
$\overline{\text{RAS}}$ ONLY REFRESH CYCLE



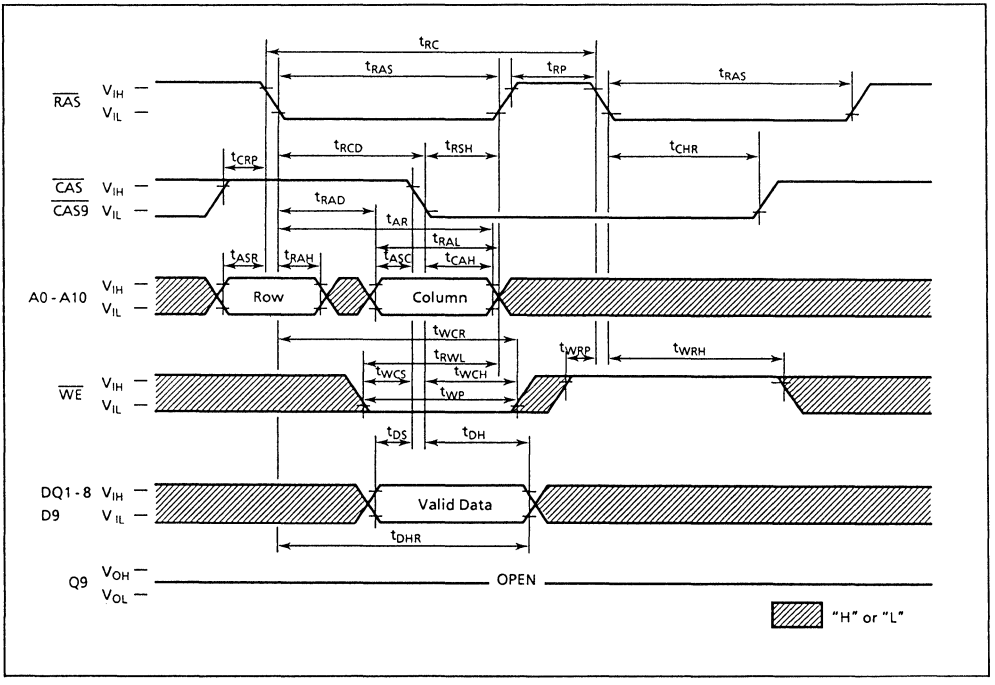
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ AUTO REFRESH CYCLE



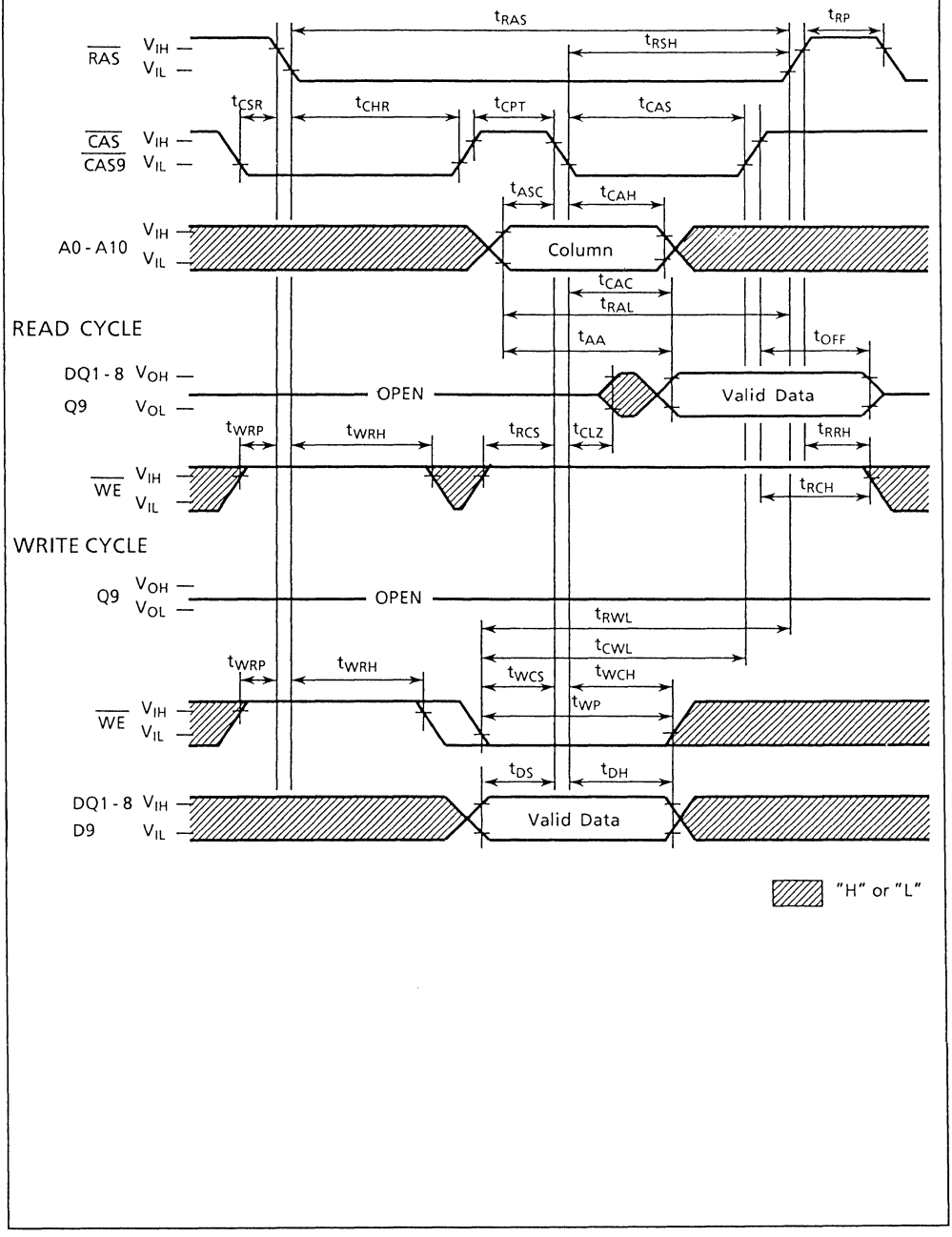
HIDDEN REFRESH READ CYCLE



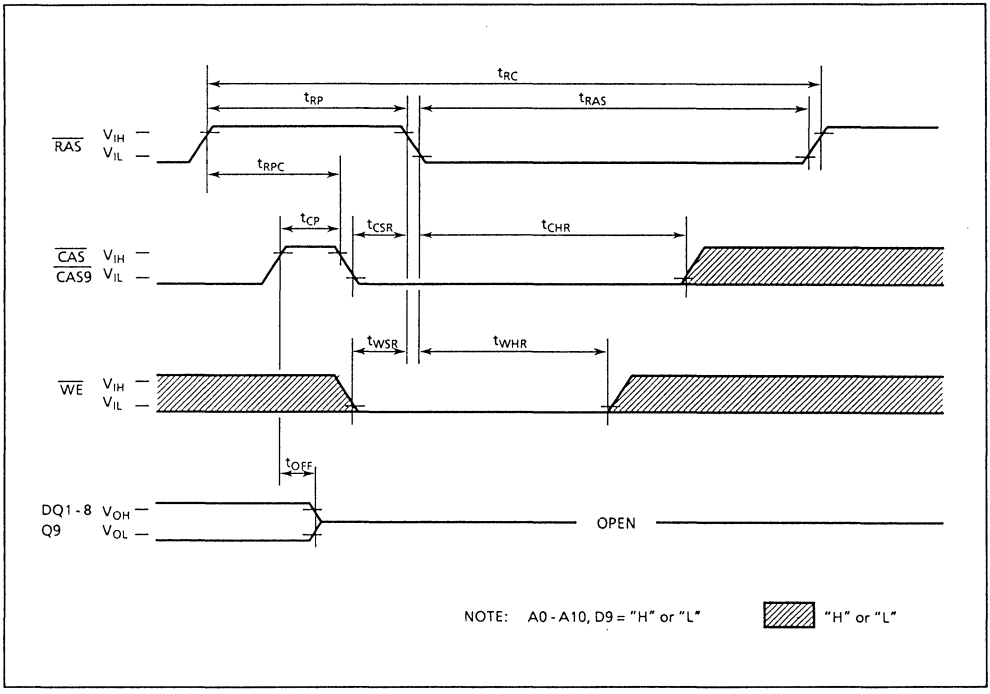
HIDDEN REFRESH WRITE CYCLE



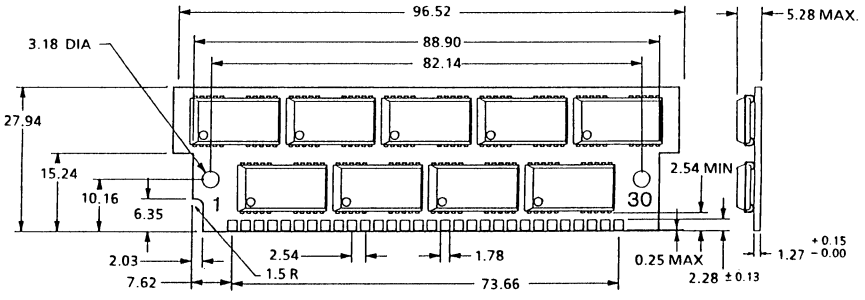
$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH COUNTER TEST



TEST MODE INITIATE CYCLE

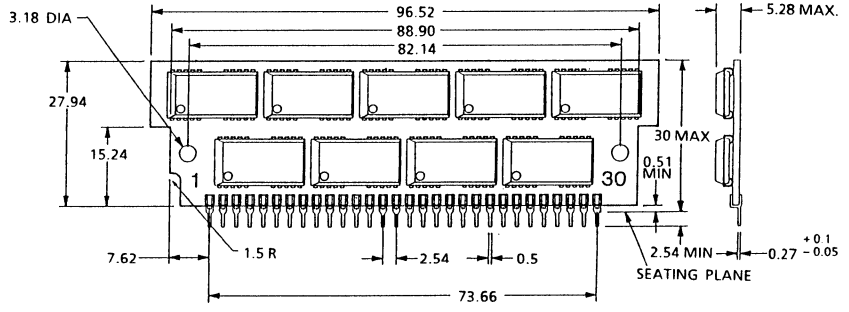


MSC2340YS9



NOTE 1) SUBSTRATE ..... GLASS EPOXY (FR-4)
2) CONTACT PADS .... Pb/Sn or Au PLATING
3) 4M x 1 DRAM x 9 pcs

MSC2340KS9



NOTE 1) SUBSTRATE ..... GLASS EPOXY (FR-4)
2) CONTACT LEAD .... Pb/Sn SOLDER
3) SEATING PLANE (PAI 0.83, PITCH 2.54)
4) 4M x 1 DRAM x 9 pcs

4

MOS STATIC RAMS

5 MOS STATIC RAMS

MSM5165AL	8,192-Word x 8-Bits RAM (CMOS)	387
MSM5188	16,384-Word x 4-Bits RAM (CMOS)	394
MSM51257AL	32,768-Word x 8-Bits RAM (CMOS)	399
MSM51257ALL	32,768-Word x 8-Bit CMOS STATIC RAM	406
MSM51256	32,768-Word x 8-Bits RAM (CMOS)	413

OKI semiconductor

MSM5165AL

8,192-WORD x 8-BIT CMOS STATIC RAM (E3-S-017-32)

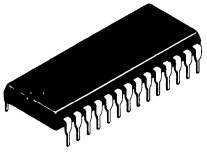
GENERAL DESCRIPTION

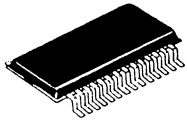
The MSM5165ALRS/GS is a 8192-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM5165ALRS/GS is also a CMOS silicon gate device which requires very low power during standby (standby current of 100μA) when there is no chip selection.
A byte system is adopted, and since there is pin compatibility with standard ultra-violet EPROMs, this device is ideal for use as a peripheral memory for microcomputers and data terminal units etc. In addition, $\overline{CE}_1$ CE_2 and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  Standby; 0.55 mW MAX
  Operation; 330 mW MAX
- High Speed (Equal Access and Cycle Time)
  100 ~ 150 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- Pin Compatible with
  64K EPROM (MSM2764)
- 28-pin DIP PKG
- 28-pin FLAT PKG

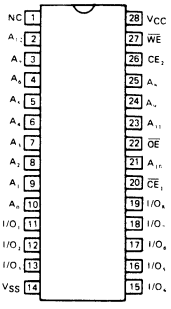
5





PIN CONFIGURATION

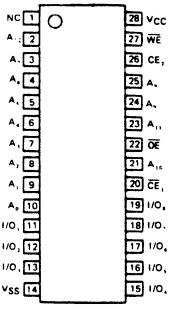
(Top View)



$A_0 \sim A_{12}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CE}_1$, CE_2 : Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

PIN CONFIGURATION

(Top View)



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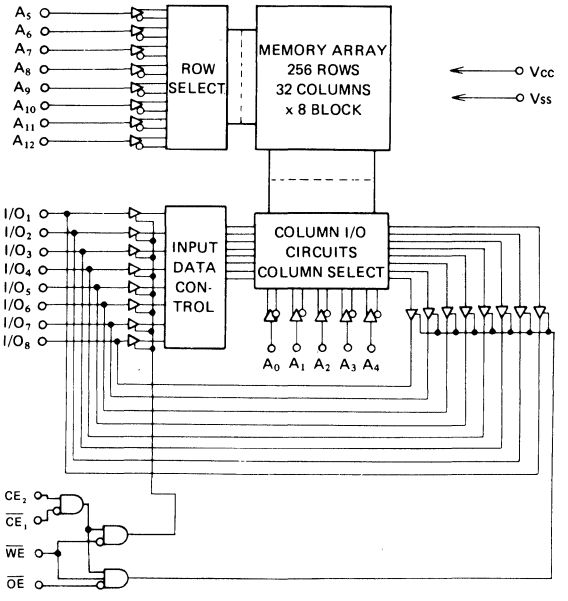
FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

Mode	$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	X	High Z
	X	L	X	X	
Read	L	H	H	H	High Z
	L	H	H	L	D_{OUT}
Write	L	H	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM5165AL			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	-1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	-1		1	μA	$\overline{CE}_1$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}
Output Voltage	V_{OH}	2.4			V	I_{OH} = -1 mA
	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Standby Supply Current	I_{CCS}		2	100	μA	$\overline{CE}_1 \geqq V_{CC}$ - 0.2V, $CE_2 \geqq V_{CC}$ - 0.2V V_{IN} = 0 to V_{CC}
						$CE_2 \leqq 0.2V$ V_{IN} = 0 to V_{CC}
	I_{CCS1}			3	mA	$\overline{CE}_1$ = V_{IH}, CE_2 = V_{IL}
Operating Supply Current	I_{CCA}			①	mA	T_{CYC} = Min Cycle, I_{OUT} = 0 mA
				15		T_{CYC} = 1 μs, I_{OUT} = 0 mA

① 5165AL-10 60 mA 5165AL-12 55 mA 5165AL-15 50 mA

AC CHARACTERISTICS

Test Condition

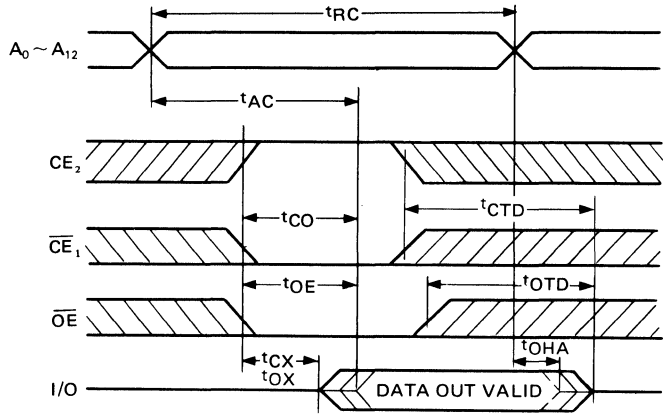
Parameter	Conditions
Input Pulse Level	V_{IH}=2.4V, V_{IL}=0.6V
Input Rise and Fall Times	10 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM5165AL-10		MSM5165AL-12		MSM5165AL-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100		120		150		ns
Address Access Time	t_{AC}		100		120		150	ns
Chip Enable Access Time	t_{CO}		100		120		150	ns
Output Enable to Output Valid	t_{OE}		50		60		70	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	10		10		15		ns
Output Enable to Output Active	t_{OX}	5		5		5		ns
Output 3-state from Output Disable	t_{OTD}	0	35	0	40	0	50	ns
Output 3-state from Chip Deselection	t_{CTD}	0	50	0	60	0	70	ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CE_1}$, a high CE_2, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CX} is specified from $\overline{CE_1}$ or CE_2 whichever occurs last.
3. t_{CTD} is specified from $\overline{CE_1}$ or CE_2 whichever occurs first.
4. t_{OHA} and t_{OTD} are specified by the time when DATA OUT is floating.

5

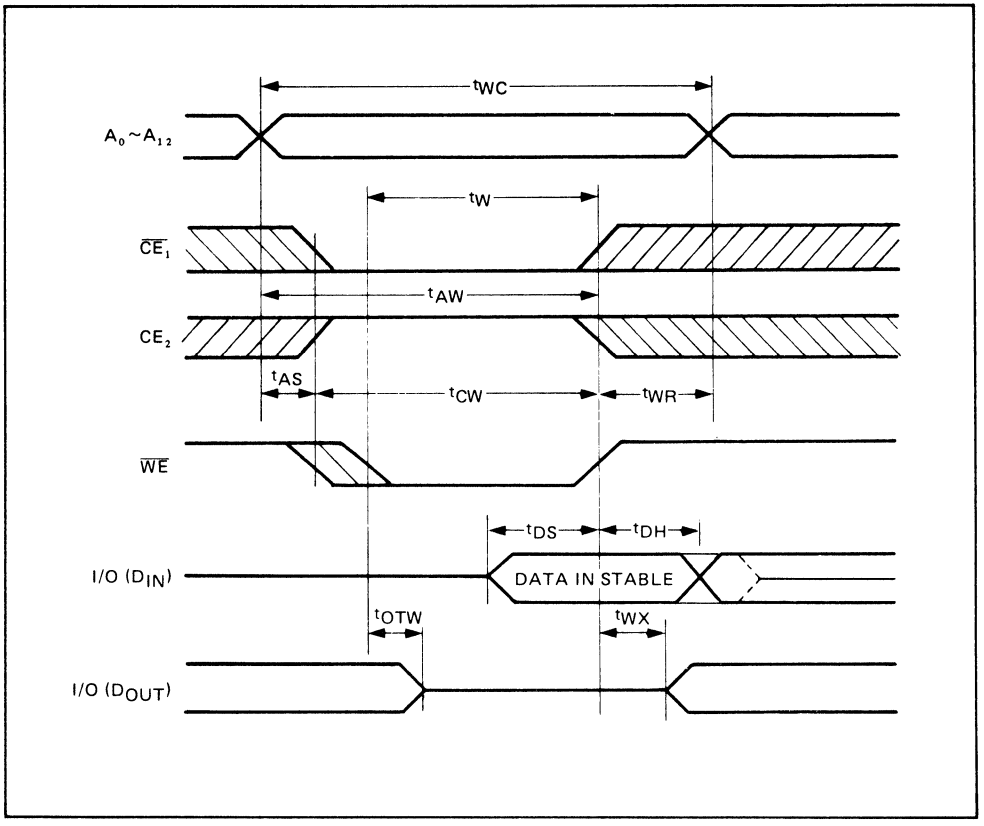
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM5165AL-10		MSM5165AL-12		MSM5165AL-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	100		120		150		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	60		70		90		ns
Write Recovery Time	t_{WR}	15		15		15		ns
Data Setup Time	t_{DS}	40		50		60		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	35	0	40	0	50	ns
Chip Selection to End of Write	t_{CW}	80		100		120		ns
Address Valid to End of Write	t_{AW}	80		100		120		ns
Output Active from End of Write	t_{WX}	5		5		5		ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CE_1}$, CE_2 or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CE_1}$, CE_2 or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE



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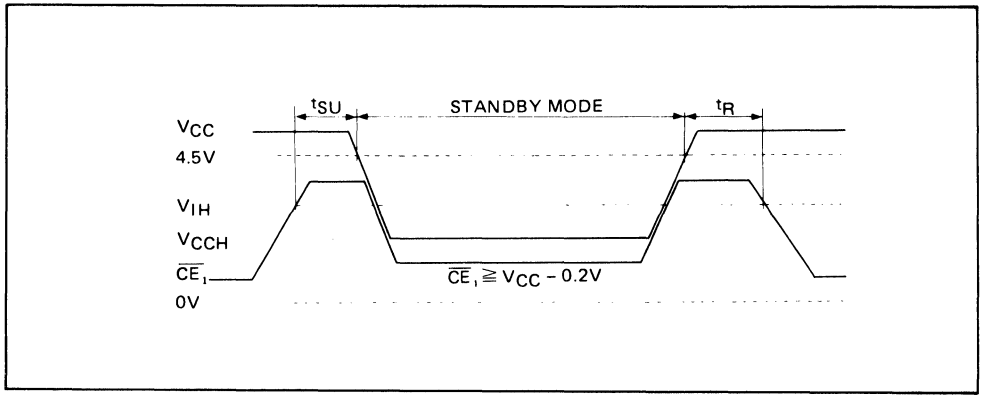
LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = 0°C to +70°C, unless otherwise noted)

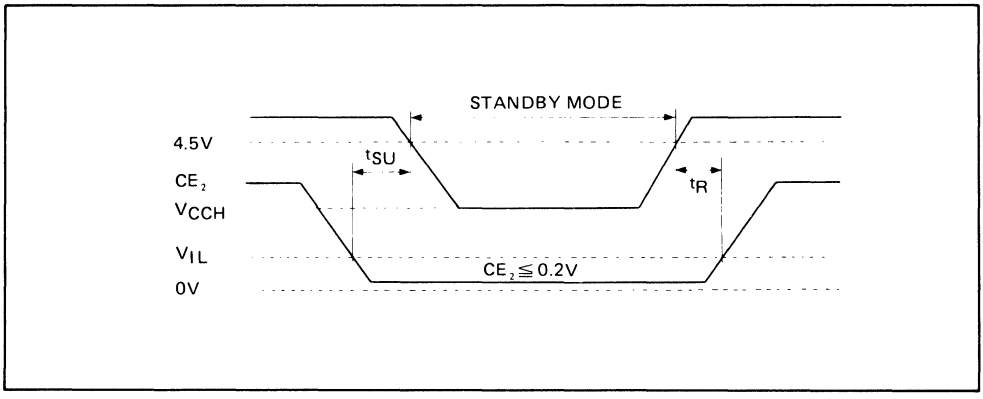
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2		5.5	V	$\overline{CE}_1 \geqq V_{CC} - 0.2V$, $CE_2 \geqq V_{CC} - 0.2V$
						$CE_2 \leqq 0.2V$
Data Retention Current	I_{CCH}		1	50	μA	V_{CC} = 3V, $\overline{CE}_1 \geqq V_{CC} - 0.2V$ $CE_2 \geqq V_{CC} - 0.2V$
						V_{CC} = 3V, $CE_2 \leqq 0.2V$
CS to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	*t_{RC}			ns	

*t_{RC} : Read Cycle Time

$\overline{CE}_1$ CONTROL



CE_2 CONTROL



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			10	pF
Input Capacitance	C_{IN}			6	pF

Note: This parameter is periodically sampled and not 100% tested.

MSM5188

16,384-WORD × 4-BIT HIGH SPEED STATIC CMOS RAM

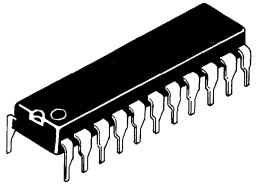
GENERAL DESCRIPTION

The MSM5188RS is a static CMOS RAM organized as 16384 words by 4 bits. It features 5V single power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary which makes this device very easy to use.

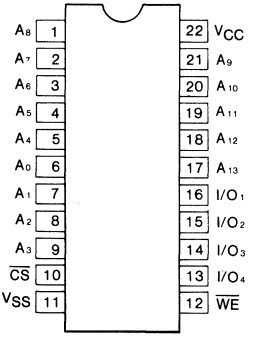
The MSM5188RS is offered in a 22-pin slim package.

FEATURES

- Single 5V supply (±10%)
- Completely static operation
- Operating temperature range Ta = 0 to 70°C
- Low power dissipation
  - Standby ..... 11 mW MAX
  - Operation ..... 605 mW MAX
- Access time
  - 45/55/70 ns MAX
- Direct TTL compatible (Input and output)
- 3-State output
- 22 pin DIP PKG (300 mil width)

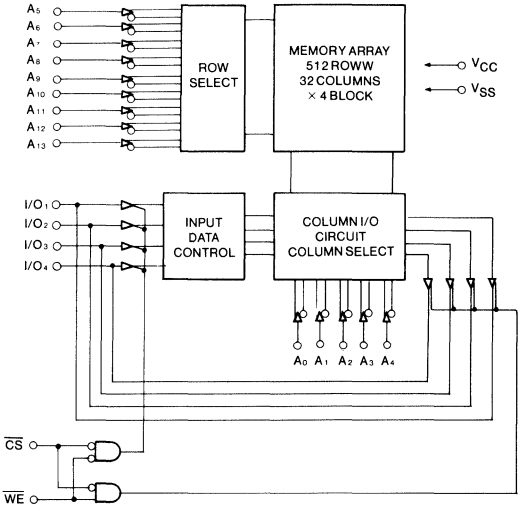


PIN CONFIGURATION



Pin Names	Function
A_0 to A_{13}	Address input
I/O_1 to I/O_4	Data input/output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
V_{CC}, V_{SS}	Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25°C Respect to V_{SS}	−0.3 to 7.0	V
Input Voltage	V_{IN}		−0.3 to 7.0	V
Power Dissipation	PD	Ta = 25°C	1.0	W
Operating Temperature	Topr	–	0 to +70	°C
Storage Temperature	Tstg	–	−55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	–	4.5	5.0	5.5	V
"H" Input Voltage	V_{IH}	V_{CC} = 5V ± 10%	2.2	–	V_{CC} +0.3	V
"L" Input Voltage	V_{IL}		−0.3	–	0.8	V
Output Load	CL	–	–	–	30	pF
	N	TTL Load	–	–	1	

* When pulse width is equal to or smaller than 20 ns, V_{IH} max = V_{CC} + 1.0V, V_{IL} min = −1.0V.

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Ta = 0°C to 70°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Leakage Current	I_{LI}	VI = 0 to V_{CC}	−1		1	μA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH} VI/O = 0 to V_{CC}	−1		1	μA
"H" Output Voltage	V_{OH}	I_{OH} = −4 mA	2.4			V
"L" Output Voltage	V_{OL}	I_{OL} = 8 mA			0.4	V
Standby Supply Current	I_{CCS}	$\overline{CS} \geqq V_{CC} - 0.2V$ VIN ≦ 0.2V OR VIN ≧ V_{CC} − 0.2V			2	mA
	I_{CCS1}	$\overline{CS}$ = V_{IH} T_{CYC} = min cycle			30	mA
Operating Supply Current	I_{CCA}	Min cycle, I_{OUT} = 0 mA			110	mA

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Condition	Min.	Max.	Unit
Input Capacitance	C_I	V_I = 0V		6	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V		8	pF

AC CHARACTERISTICS TEST CONDITIONS

Parameter	Conditions
Input Pulse Level	V_{IH} = 3.0V, V_{IL} = 0V
Input Rise and Fall Times	5 ns
Input/Output Timing Reference Level	1.5V
Output Load	CL = 30 pF, 1 TTL GATE

5

READ CYCLE

(V_{CC} = 5V±10%, Ta = 0°C to 70°C)

Parameter	Symbol	5188-45		5188-55		5188-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	T_{RC}	45		55		70		ns
Address Access Time	T_{AC}		45		55		70	ns
Chip Select Access Time	T_{CO}		45		55		70	ns
Chip Selection to Output Active	T_{CX}	5		5		5		ns
Output Hold Time from Address Change	T_{OHA}	5		5		5		ns
Output 3-state from Deselection	T_{OTD}	0	25	0	25	0	30	ns
Chip Selection to Power up Time	T_{PU}	0		0		0		ns
Chip Deselection to Power Down Time	T_{PD}	0	45	0	55	0	70	ns

Notes: 1. Read Condition: During the overlap of a low $\overline{CS}$ and a high $\overline{WE}$.
2. T_{CX} and T_{OTD} are measured ±200 mV from steady state voltage with specified loading in Figure 2.

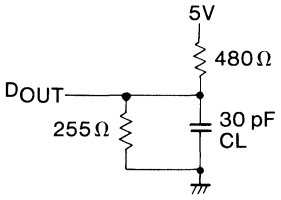


Figure 1 Output Load

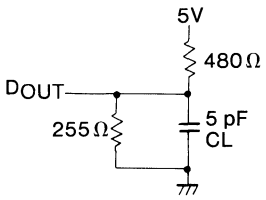


Figure 2 Output Load

Note: CL includes scope and jig.

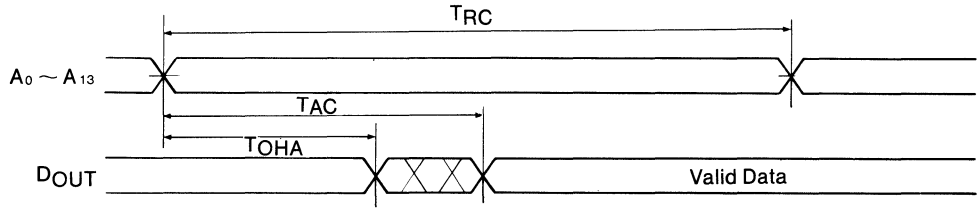
WRITE CYCLE

(V_{CC} = 5V±10%, Ta = 0°C to 70°C)

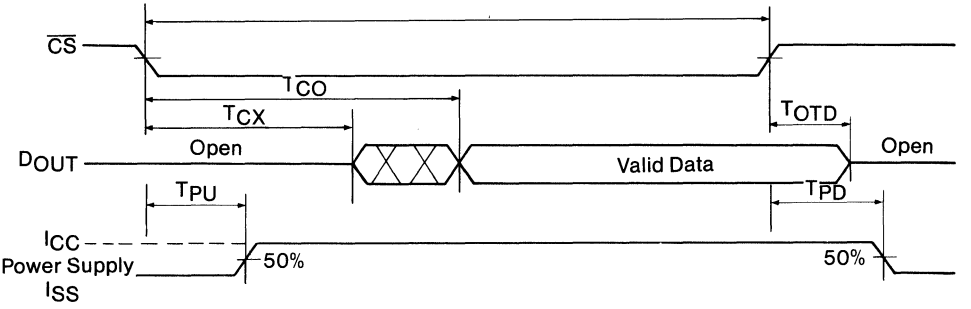
Parameter	Symbol	5188-45		5188-55		5188-70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	T_{WC}	45		55		70		ns
Chip Selection to End of Write	T_{CW}	40		45		55		ns
Address Valid to End of Write	T_{AW}	40		45		55		ns
Address to Write Setup Time	T_{AS}	0		0		0		ns
Write Time	T_W	40		45		55		ns
Write Recovery Time	T_{WR}	5		5		5		ns
Data Setup Time	T_{DS}	25		25		30		ns
Data Hold from Write Time	T_{DH}	0		0		0		ns
Output 3-state from Write	T_{OTW}	0	20	0	25	0	30	ns
Output Active from End of Write	T_{OW}	0		0		0		ns

Notes:
1. Write condition: During the overlap of a low $\overline{CS}$ and a low $\overline{WE}$.
2. T_{AS} is specified from a low $\overline{CS}$ or a low $\overline{WE}$, whichever occurs last after the address is set.
3. T_W is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$.
4. T_{WR}, T_{DS} and T_{DH} are specified from a high $\overline{CS}$ or a high $\overline{WE}$, whichever occurs first.
5. T_{OTW} and T_{OW} are measured ±200 mV from steady state voltage with specified loading in Figure 2.
6. When I/O pins are Data output mode, don't force inverse input signals to those pins.

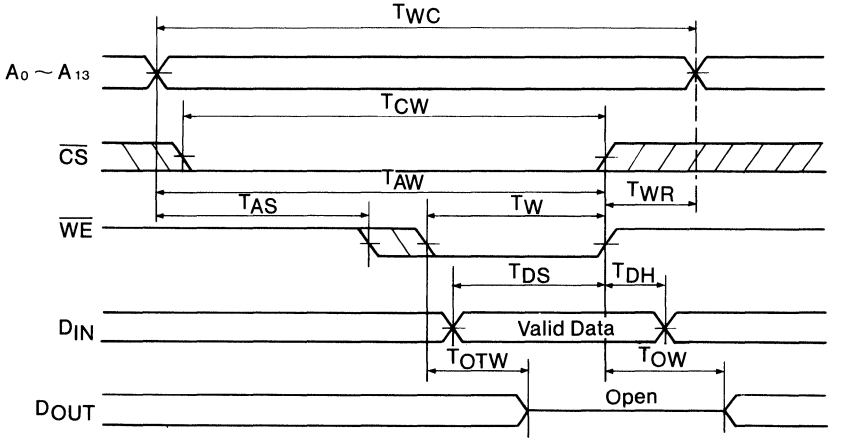
READ CYCLE TIMING 1



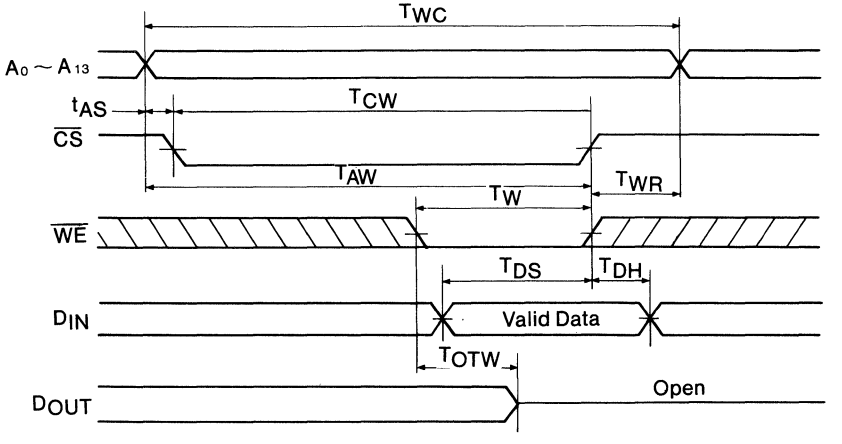
READ CYCLE TIMING 2



WRITE CYCLE TIMING 1
($\overline{WE}$ Control)



WRITE CYCLE TIMING 2
($\overline{CS}$ Control)



OKI semiconductor

MSM51257AL

32,768-WORD x 8-BIT CMOS STATIC RAM

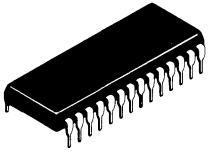
GENERAL DESCRIPTION

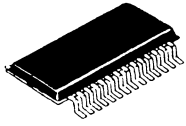
The MSM51257ALRS/GS is a 32768-word by 8-bit CMOS RAM static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very to use. The MSM51257ALRS/GS is also a CMOS silicon gate device which requires very low power during standby (standby current of 100μA) when there is no chip selection.
$\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  Standby; 0.55 mW MAX
  Operation; 385 mW MAX
- High Speed (Equal Access and Cycle Time)
  85-120 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 28-pin DIP PKG
- 28-pin FLAT PKG

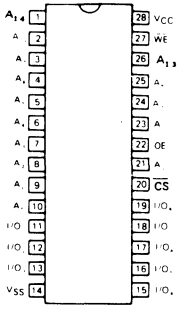
5





PIN CONFIGURATION

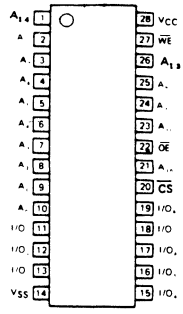
(Top View)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

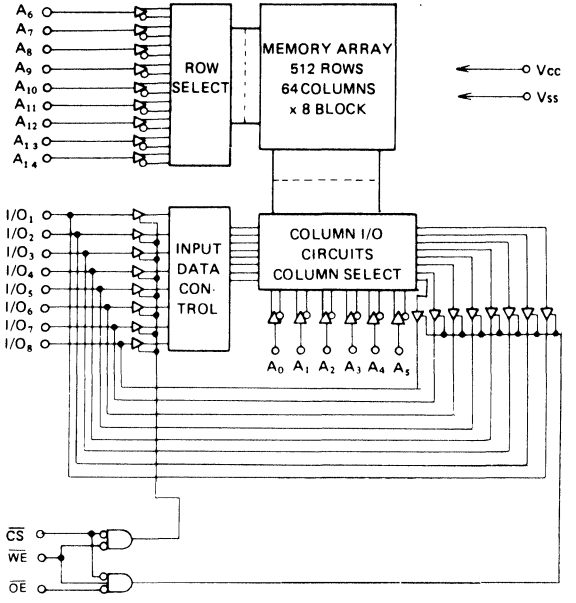
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM51257AL			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−1		1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}
Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA
	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Standby Supply Current	I_{CCS}		2	100	μA	$\overline{CS}$ ≧ V_{CC} − 0.2V V_{IN} = 0 to V_{CC}
	I_{CCS1}			3	mA	$\overline{CS}$ = V_{IH}
Operating Supply Current	I_{CCA}			①	mA	MIN CYCLE, I_{OUT} = 0 mA

① 51257AL-85 80 mA 51257AL-10/12 70 mA

AC CHARACTERISTICS

Test Condition

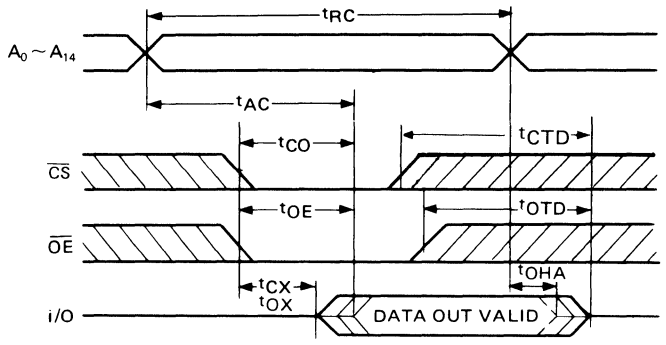
Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM51257AL-85		MSM51257AL-10		MSM51257AL-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85		100		120		ns
Address Access Time	t_{AC}		85		100		120	ns
Chip Enable Access Time	t_{CO}		85		100		120	ns
Output Enable to Output Valid	t_{OE}		45		50		60	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	5		10		10		ns
Output 3-state from Output Disable	t_{OTD}		30		35		35	ns
Output 3-state from Chip Deselection	t_{CTD}		30		35		35	ns
Output Enable to Output Active	t_{OX}	5		5		5		ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CTD} and t_{OTD} are specified by the time when DATA OUT is floating.

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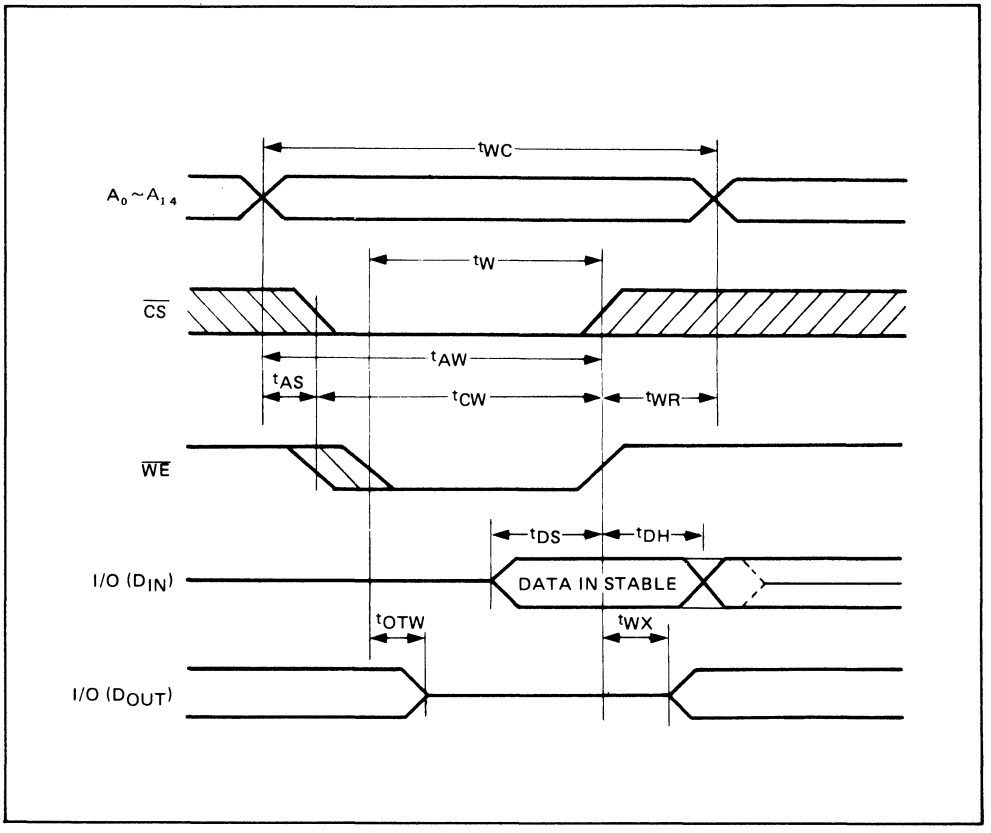
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM51257AL-85		MSM51257AL-10		MSM51257AL-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	85		100		120		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	70		75		90		ns
Write Recovery Time	t_{WR}	5		10		10		ns
Data Setup Time	t_{DS}	40		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	30	0	35	0	35	ns
Chip Selection to End of Write	t_{CW}	75		90		100		ns
Address Valid to End of Write	t_{AW}	75		90		100		ns
Output Active from End of Write	t_{WX}	5		5		5		ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$, and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$, and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE



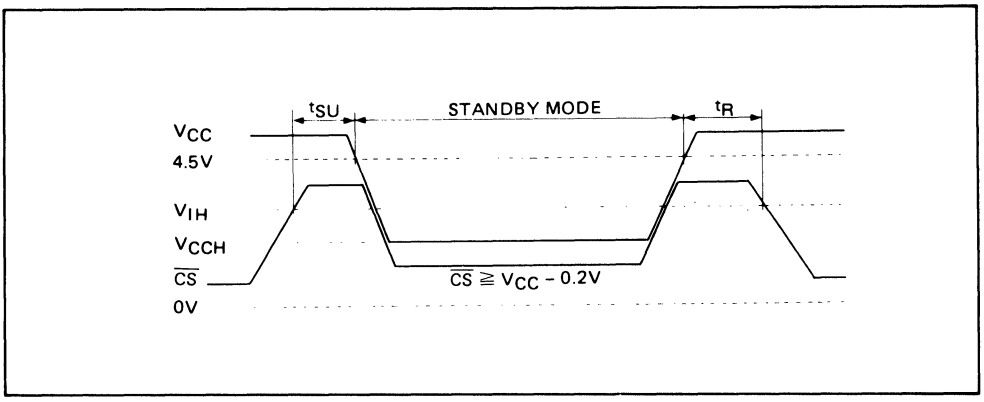
LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2		5.5	V	$\overline{CS} \geqq V_{CC} - 0.2V$
Data Retention Current	I_{CCH}		1	50	μA	V_{CC} = 3V, $\overline{CS} \geqq V_{CC} - 0.2V$
CS to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	*t_{RC}			ns	

* t_{RC} = Read Cycle Time

$\overline{CS}$ CONTROL



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			10	pF
Input Capacitance	C_{IN}			10	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM51257ALL

32,768-WORD x 8-BIT CMOS STATIC RAM

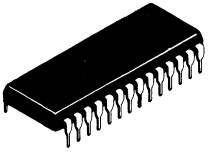
GENERAL DESCRIPTION

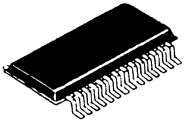
The MSM 51257ALLRS/GS is a 32768-word by 8-bit CMOS RAM static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very easy to use. The MSM51257ALLRS/GS is also a CMOS silicon gate device which requires very low power during standby (standby current of 20μA) when there is no chip selection.
$\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

5

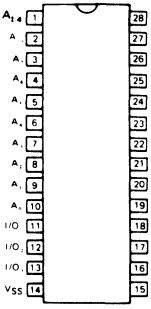
- Single 5V Supply
- 0°C ~ 70°C
- Low Power Dissipation
  Standby; 0.11 mW MAX
  Operation; 385 mW MAX
- High Speed (Equal Access and Cycle Time)
  85-120 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 28-pin DIP PKG
- 28-pin FLAT PKG





PIN CONFIGURATION

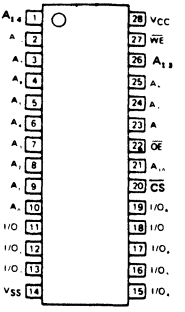
(Top View)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

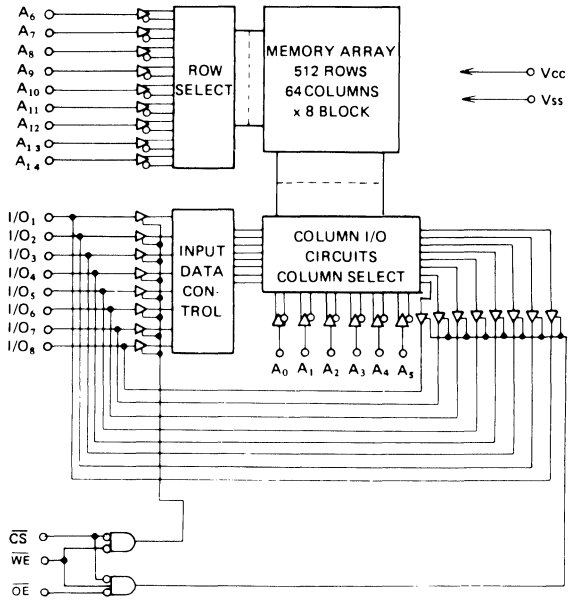
PIN CONFIGURATION

(Top View)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3* to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

* Pulse Width < 30ns : −3.0V MIN

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3*		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

* Pulse Width < 30ns : −3.0V MIN

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = 0°C to +70°C)

Paramter	Symbol	MSM51257ALL			Unit	Test Condition
		Min.	Typ.	Max.		
Input Leakage Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}
Output Leakage Current	I_{LO}	−1		1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}
Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA
	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Standby Supply Current	I_{CCS}			20*	μA	$\overline{CS}$ ≧ V_{CC} − 0.2V V_{IN} = 0 to V_{CC}
	I_{CCS1}			3	mA	$\overline{CS}$ = V_{IH}
Operating Supply Current	I_{CCA}			①	mA	MIN CYCLE, I_{OUT} = 0 mA

*Ta=0 to 40°C : 6μA MAX

① 51257ALL-85 80mA 51257ALL-10/12 70mA

AC CHARACTERISTICS

Test Condition

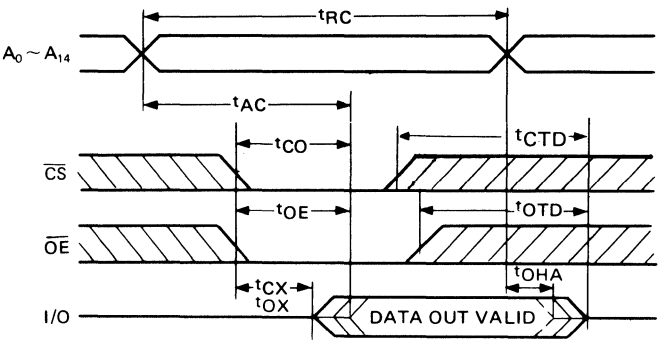
Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to 70°C)

Parameter	Symbol	MSM51257ALL-85		MSM51257ALL-10		MSM51257ALL-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	85		100		120		ns
Address Access Time	t_{AC}		85		100		120	ns
Chip Enable Access Time	t_{CO}		85		100		120	ns
Output Enable to Output Valid	t_{OE}		45		50		60	ns
Chip Selection to Output Active	t_{CX}	10		10		10		ns
Output Hold Time From Address Change	t_{OHA}	5		10		10		ns
Output 3-state from Output Disable	t_{OTD}		30		35		35	ns
Output 3-state from Chip Deselection	t_{CTD}		30		35		35	ns
Output Enable to Output Active	t_{OX}	5		5		5		ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CTD} and t_{OTD} are specified by the time when DATA OUT is floating.

5

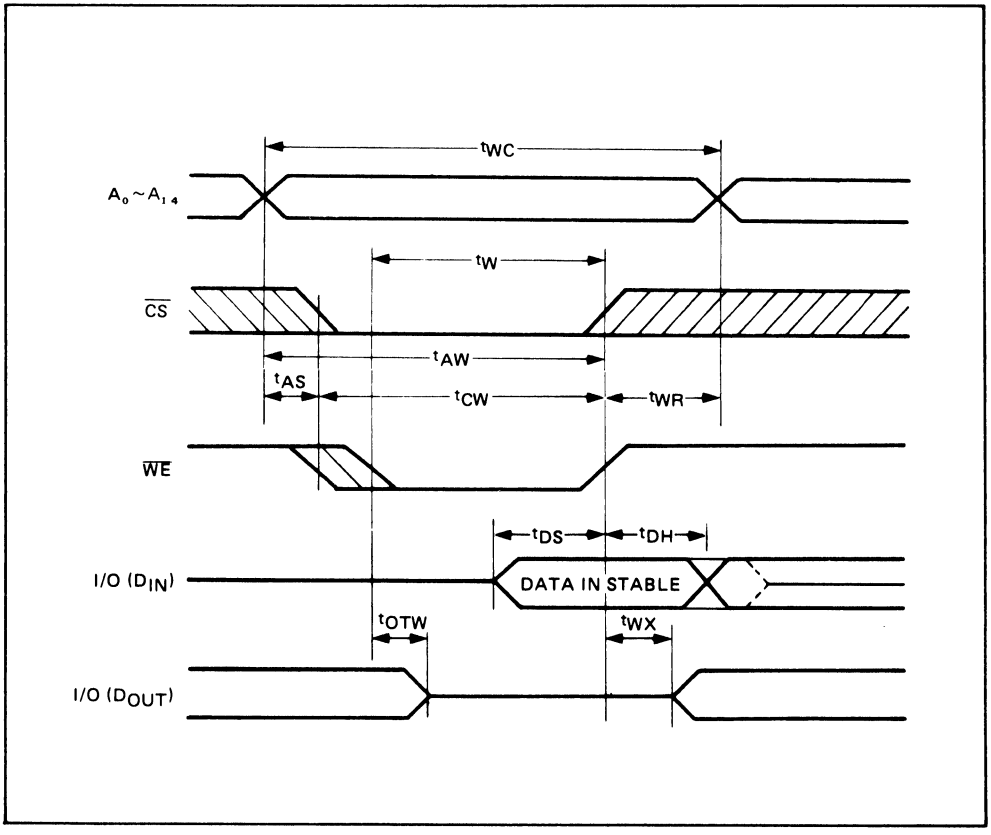
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = 0°C to +70°C)

Item	Symbol	MSM51257ALL-85		MSM51257ALL-10		MSM51257ALL-12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	85		100		120		ns
Address to Write Setup Time	t_{AS}	0		0		0		ns
Write Time	t_W	70		75		90		ns
Write Recovery Time	t_{WR}	5		10		10		ns
Data Setup Time	t_{DS}	40		40		50		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
Output 3-State from Write	t_{OTW}	0	30	0	35	0	35	ns
Chip Selection to End of Write	t_{CW}	75		90		100		ns
Address Valid to End of Write	t_{AW}	75		90		100		ns
Output Active from End of Write	t_{WX}	5		5		5		ns

Notes: 1. A Write Cycle occurs during the overlap of a low $\overline{CS}$, and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$, and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE



LOW V_{CC} DATA RETENTION CHARACTERISTICS

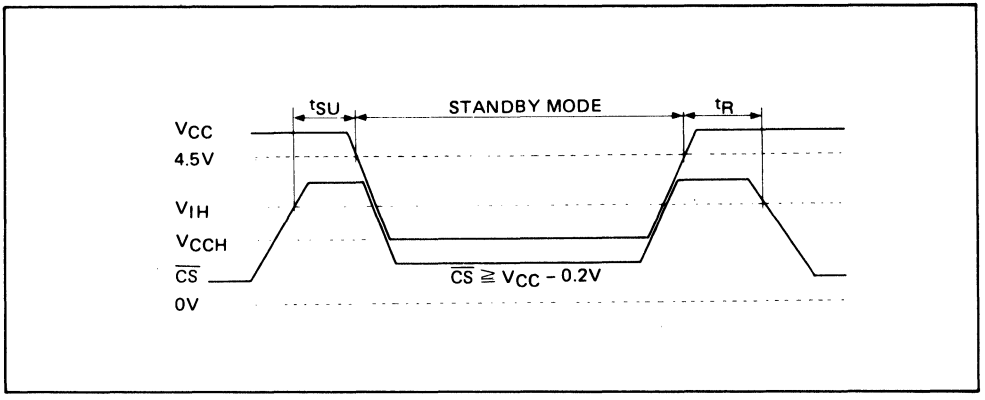
(T_a = 0°C to +70°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
V_{CC} for Data Retention	V_{CCH}	2		5.5	V	$\overline{CS} \geqq V_{CC} - 0.2V$
Data Retention Current	I_{CCH}			10*	μA	V_{CC} = 3V, $\overline{CS} \geqq V_{CC} - 0.2V$
CS to Data Retention Time	t_{SU}	0			ns	
Operation Recovery Time	t_R	**t_{RC}			ns	

* Ta=0 to 40°C : 3μA MAX

** t_{RC} : Read Cycle Time

$\overline{CS}$ CONTROL



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CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			10	pF
Input Capacitance	C_{IN}			10	pF

Note: This parameter is periodically sampled and not 100% tested.

OKI semiconductor

MSM51256

32,768-WORD x 8-BIT CMOS STATIC RAM

GENERAL DESCRIPTION

The MSM51256RS/GS is a 32768-word by 8-bit CMOS static RAM featuring 5V power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary, making this device very to use. The MSM51256RS/GS is also a CMOS silicon gate device which requires very low power during standby (standby current of 1 μA) when there is no chip selection.
$\overline{CS}$ and $\overline{OE}$ signals enable OR ties with the output terminals of other chips, thereby facilitating simple memory expansion and bus line control etc.

FEATURES

- Single 5V Supply
- −40°C ~ 85°C
- Low Power Dissipation
  Standby; 5.5 μW MAX
  Operation; 385mW MAX
- High Speed (Equal Access and Cycle Time)
  100/120 ns MAX
- Direct TTL Compatible. (Input and Output)
- 3-State Output
- 28-pin DIP PKG
- 28-pin FLAT PKG
- 3V operation

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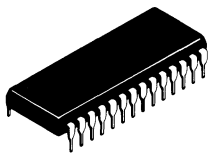
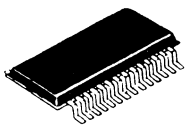
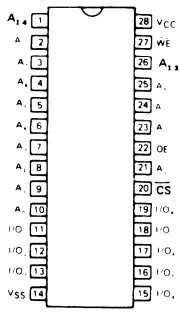




PIN CONFIGURATION

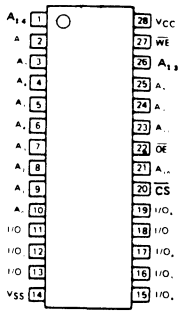
(Top View)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
$\overline{WE}$: Write Enable
$\overline{OE}$: Output Enable
V_{CC}, V_{SS} : Supply Voltage

PIN CONFIGURATION

(Top View)



$A_0 \sim A_{14}$: Address INPUTS
$I/O_1 \sim I/O_8$: Data Input/Output
$\overline{CS}$: Chip Select
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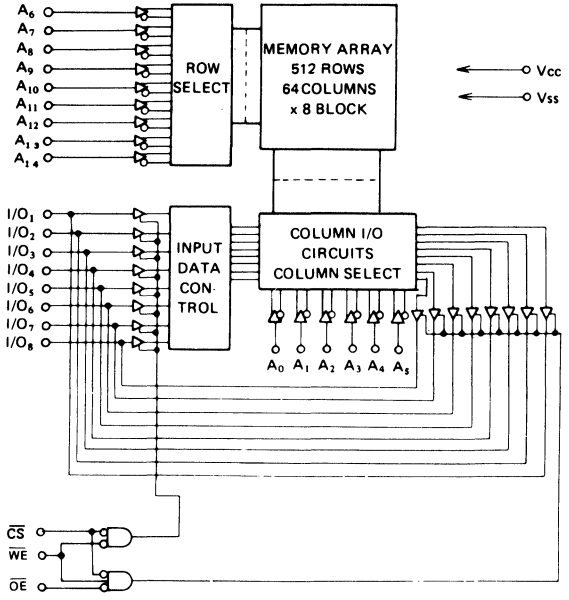
V_{CC}, V_{SS} : Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



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TRUTH TABLE

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O Operation
Standby	H	X	X	High Z
Read	L	H	H	High Z
	L	H	L	D_{OUT}
Write	L	L	X	D_{IN}

X : H or L

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit	Conditions
Supply Voltage	V_{CC}	−0.3 to 7.0	V	Respect to GND
Input Voltage	V_{IN}	−0.3 to V_{CC} + 0.3	V	
Operating Temperature	T_{opr}	−40 ~ 85	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	
Power Dissipation	P_D	1.0	W	Ta = 25°C

RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	4.5	5	5.5	V	5V ± 10%
	V_{SS}		0		V	
Data Retention Voltage	V_{CCH}	2	5	5.5	V	
Input Voltage	V_{IH}	2.2		V_{CC} + 0.3	V	5V ± 10%
	V_{IL}	−0.3		0.8	V	
Output Load	C_L			100	pF	
	TTL			1		

DC CHARACTERISTICS

(V_{CC} = 5V ±10%, T_a = −40°C to +85°C)

Paramter	Symbol	MSM51256			Unit	Test Condition	
		Min.	Typ.	Max.			
Input Leakage Current	I_{LI}	−1		1	μA	V_{IN} = 0 to V_{CC}	
Output Leakage Current	I_{LO}	−1		1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}	
Output Voltage	V_{OH}	2.4			V	I_{OH} = −1 mA	
	V_{OL}			0.4	V	I_{OL} = 2.1 mA	
Standby Supply Current	I_{CCS}			0.2	μA	Ta = 25°C	$\overline{CS} \geqq V_{CC}-0.2V$ V_{IN} = 0 to V_{CC}
				1		Ta = 60°C	
				10		Ta = 85°C	
	I_{CCS1}			3	mA	$\overline{CS}$ = V_{IH}	
Operating Supply Current	I_{CCA}			70	mA	MIN CYCLE, I_{OUT} = 0 mA	
				20		f=1 MHz, V_{IH}=V_{CC}, V_{IL}=0V, I_{OUT}=0mA	

AC CHARACTERISTICS

Test Condition

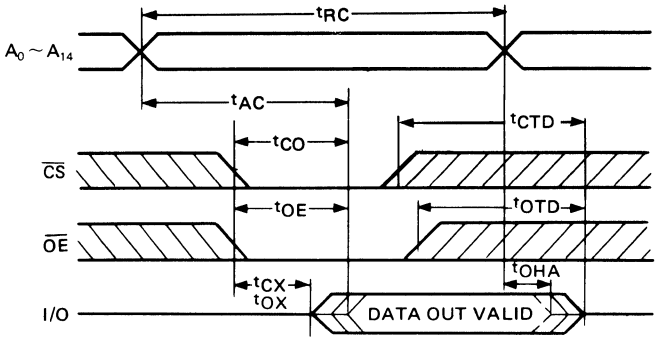
Parameter	Conditions
Input Pulse Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L=100 pF, 1 TTL Gate

READ CYCLE

(V_{CC} = 5V ± 10%, T_a = −40°C to +85°C)

Parameter	Symbol	MSM51256-10		MSM51256-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t_{RC}	100		120		ns
Address Access Time	t_{AC}		100		120	ns
Chip Enable Access Time	t_{CO}		100		120	ns
Output Enable to Output Valid	t_{OE}		50		60	ns
Chip Selection to Output Active	t_{CX}	10		10		ns
Output Hold Time From Address Change	t_{OHA}	10		10		ns
Output 3-state from Output Disable	t_{OTD}		40		50	ns
Output 3-state from Chip Deselection	t_{CTD}		50		60	ns
Output Enable to Output Active	t_{OX}	5		5		ns

READ CYCLE



Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and a high $\overline{WE}$.
2. t_{CTD} and t_{OTD} are specified by the time when DATA OUT is floating.

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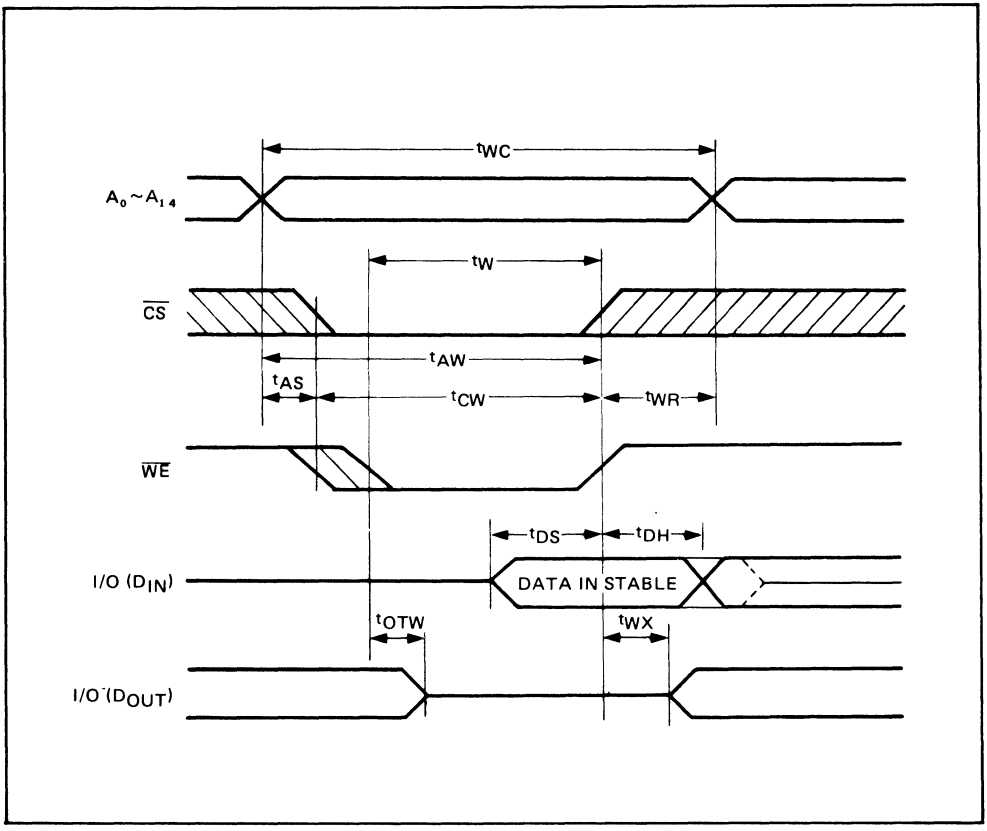
WRITE CYCLE

(V_{CC} = 5V ± 10%, T_a = −40°C to +85°C)

Item	Symbol	MSM51256-10		MSM51256-12		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t_{WC}	100		120		ns
Address to Write Setup Time	t_{AS}	0		0		ns
Write Time	t_W	75		90		ns
Write Recovery Time	t_{WR}	10		10		ns
Data Setup Time	t_{DS}	40		50		ns
Data Hold from Write Time	t_{DH}	0		0		ns
Output 3-State from Write	t_{OTW}	0	50	0	60	ns
Chip Selection to End of Write	t_{CW}	90		100		ns
Address Valid to End of Write	t_{AW}	90		100		ns
Output Active from End of Write	t_{WX}	5		5		ns

Notes:
1. A Write Cycle occurs during the overlap of a low $\overline{CS}$, and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_W is an overlap time of a low $\overline{CS}$, and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.
7. When I/O pins are Data output mode, don't force inverse signal to those pins.

WRITE CYCLE



CAPACITANCE

(Ta = 25°C, f = 1MHz)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input/Output Capacitance	$C_{I/O}$			10	pF
Input Capacitance	C_{IN}			10	pF

Note: This parameter is periodically sampled and not 100% tested.

LOW V_{CC} DATA RETENTION CHARACTERISTICS

(T_a = −40°C to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	
V_{CC} for Data Retention	V_{CCH}	2		5.5	V	$\overline{CS} \geqq V_{CC} - 0.2V$	
Data Retention Current	I_{CCH}			0.2	μA	Ta = 25°C	V_{CC} = 3V $\overline{CS} \geqq V_{CC}$—0.2V
				1		Ta = 60°C	
				10		Ta = 85°C	
CS to Data Retention Time	t_{SU}	0			ns		
Operation Recovery Time	t_R	*t_{RC}			ns		

* t_{RC} = Read Cycle Time

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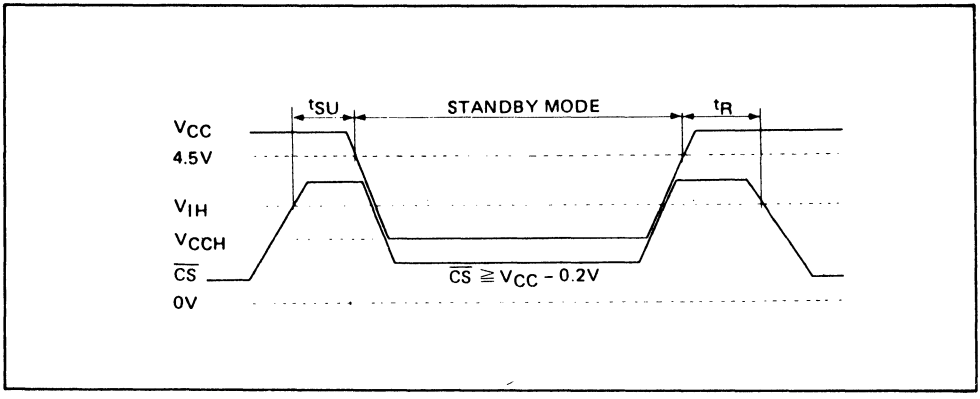
$\overline{CS}$ CONTROL



3V OPERATION

RECOMMENDED OPERATING CONDITION
(Ta = −10°C to + 60°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	V_{CC}	2.7	3.0	3.3	V	3V ± 10%
	V_{SS}	0	0	0	V	
Input Voltage	V_{IH}	V_{CC}—0.2		V_{CC}	V	3V ± 10%
	V_{IL}	0		0.2	V	
Output Load	C_L			100	pF	

3V OPERATION

DC CHARACTERISTICS

(V_{CC} = 3V ±10% Ta = −10°C to +60°C)

Parameter	Symbol	MSM51256			Unit	Test Condition	
		Min.	Typ.	Max.			
Input Leakage Current	I_{LI}	−0.1		0.1	μA	V_{IN} = 0 to V_{CC}	
Output Leakage Current	I_{LO}	−0.1		0.1	μA	$\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{CC}	
Output Voltage	V_{OH}	V_{CC}−0.1			V	I_{OH} = −20μA	
	V_{OL}			0.1	V	I_{OL} = 20μA	
Standby Supply Current	I_{CCS}		0.01	0.2	μA	Ta = 25°C	$\overline{CS}$ = V_{IH}
				1		Ta = 60°C	
Operating Supply Current	I_{CCA}			7	mA	$\overline{CS}$ = V_{IL}, f = I_{MHZ}, I_{OUT} = 0 mA	

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3V OPERATION

AC CHARACTERISTICS

Test Condition

Parameter	Conditions
Input Pulse Level	V_{IN} = V_{CC} −0.2V, V_{IL} = 0.2V
Input Rise and Fall Times	≦ 20 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 100 pF

3V OPERATION

READ CYCLE

(V_{CC} = 3V ±10% Ta = −10°C to +60°C)

Parameter	Symbol	MSM51256			Unit
		Min.	Typ.	Max.	
Read Cycle Time	t_{RC}	1000			ns
Address Access Time	t_{AC}		300	1000	ns
Chip Enable Access Time	t_{CO}		300	1000	ns
Output Enable to Output Valid	t_{OE}		150	500	ns
Chip Selection to Output Active	t_{CX}	10			ns
Output Hold Time From Address Change	t_{OHA}	20			ns
Output 3-state from Output Disable	t_{OTD}			150	ns
Output 3-state from Chip Deselection	t_{CTD}			200	ns
Output Enable to Output Active	t_{OX}	5			ns

Notes: 1. A Read occurs during the overlap of a low $\overline{CS}$, a low $\overline{OE}$ and high $\overline{WE}$.
2. t_{CTD} and t_{OTD} are specified by the time when DATA OUT is floating.

WRITE CYCLE

(V_{CC} = 3V ±10% Ta = −10°C to +60°C)

Parameter	Symbol	MSM51256			Unit
		Min.	Typ.	Max.	
Write Cycle Time	t_{WC}	1000			ns
Address to Write Setup Time	t_{AS}	100			ns
Write Time	t_{W}	500			ns
Write Recovery Time	t_{WE}	400			ns
Data Hold from Write Time	t_{DH}	50			ns
Output 3-state from Write	t_{OTW}			200	ns
Chip Selection to End of Write	t_{CW}	800			ns
Address Valid to End of Write	t_{AW}	800			ns
Output Active from End of Write	t_{WX}	10			ns

Notes:
1. A Write Cycle occurs during the overlap of a low $\overline{CS}$, and a low $\overline{WE}$.
2. $\overline{OE}$ may be both high and low in a Write Cycle.
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last.
4. t_{W} is an overlap time of a low $\overline{CS}$, and a low $\overline{WE}$.
5. t_{WR}, t_{DS} and t_{DH} are specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first.
6. **t_{OTW} is specified by the time when DATA OUT is floating, not defined by output level.**
7. **When I/O pins are Data output mode, don't force inverse signal to those pins.**

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MOS MASK ROMS

6 MOS MASK ROMS

MSM3864	8,192-Word x 8-Bits Mask ROM (NMOS)	425
MSM38128A	16,384-Word x 8-Bits Mask ROM (NMOS)	429
MSM38256	32,768-Word x 8-Bits Mask ROM (NMOS)	433
MSM38256A	32,768-Word x 8-Bits Mask ROM (NMOS)	437
MSM53256	32,768-Word x 8-Bits Mask ROM (CMOS)	441
MSM531000	131,072-Word x 8-Bits Mask ROM (CMOS)	445
MSM531001	131,072-Word x 8-Bits Mask ROM (CMOS)	449
MSM534000	262,144-Word x 16-Bits Mask ROM (CMOS)	453
MSM534000A	262,144-Word x 16-Bits MASK ROM (CMOS)	458
MSM534001A	524,288-Word x 8-Bits MASK ROM (CMOS)	463
MSM534002A	262,144-Word x 16-Bits or 524,288-Word x 8-Bits MASK ROM (CMOS)	468

OKI semiconductor

MSM3864

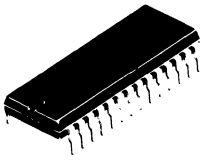
8,192 WORD x 8 BIT MASK ROM

GENERAL DESCRIPTION

The MSM3864RS is an N-channel silicon gate MOS device MASK ROM with a 8,192 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
As it provides CE, OE, and CS as the control signal, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expansion of memory and bus line control.

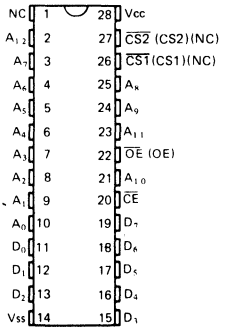
FEATURES

- 5V single power supply
- 8,192 words x 8 bits
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

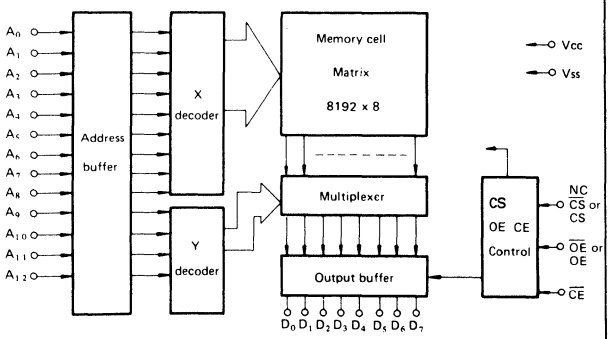
(Top View)



$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply
$A_0 \sim A_{12}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable
$\overline{CS1}$, $\overline{CS2}$	:	Chip select

Note: Please specify the OE active level and CS active level or open in ordering this IC.

FUNCTIONAL BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	Respect to V_{SS}
Output Voltage	V_O	−0.5 to 7	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	–	4.5	5	5.5	V
	V_{SS}	–	0	0	0	V
Input Signal Level	V_{IH}	–	2	5	6	V
	V_{IL}	–	−0.5	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	–	V_{CC}	V
	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	–	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or V_{CC} Chip not selected	−10	–	10	μA
Power Supply Current	IccA	V_{CC} = Max. I_O = 0 mA	–	–	100	mA
	Iccs	V_{CC} = Max. $\overline{CE}$ = V_{IH}, I_O = 0 mA	–	–	30	mA
Peak Power ON Current	Ipo	V_{CC} = GND ~ V_{CC} Min. $\overline{CE}$ = V_{CC} or V_{IH}	–	–	60	mA
Operating Temperature	T_{opr}	–	0	–	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

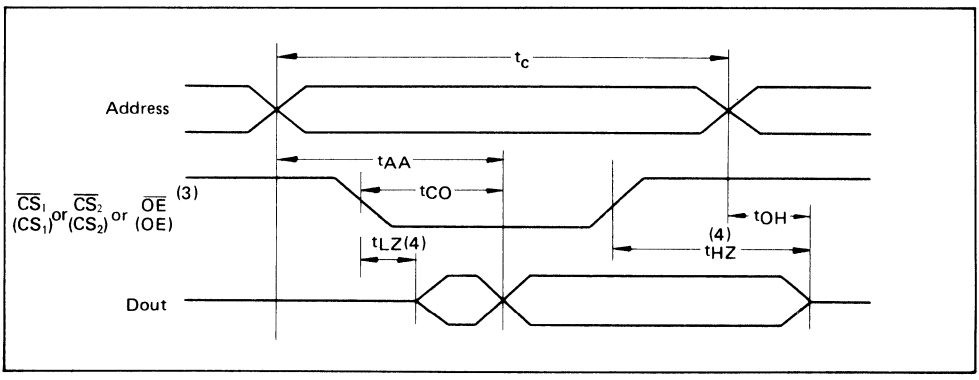
Parameter	Conditions
Input Signal Level	V_{IH}=2.4V, V_{IL}=0.6V
Input Rising, Falling Time	tr=tf= 5 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

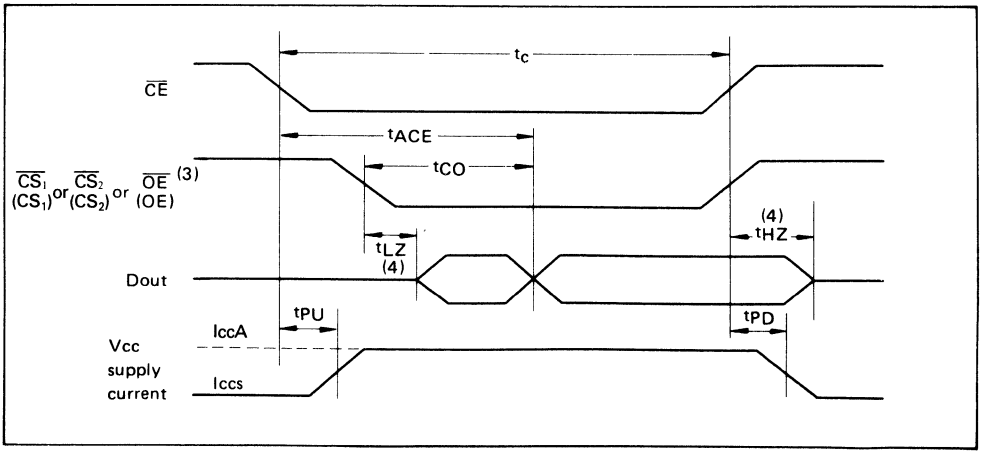
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_c	250	–	–	ns	
Address Access Time	t_{AA}	–	–	250	ns	
Chip Enable Access Time	t_{ACE}	–	–	250	ns	
Output Delay Time	t_{CO}	–	–	100	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	100	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	
Power Up Time	t_{PU}	0	–	–	ns	
Power Down Time	t_{PD}	–	–	100	ns	

1) READ CYCLE-1[1]



2) READ CYCLE-2[2]



Note: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) The $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{Lz} is determined by the later level, $\overline{CE}$ "L"/$\overline{CS}$ "L" or $\overline{OE}$ "L".
t_{Hz} is determined by the earlier $\overline{CE}$ "H"/$\overline{CS}$ "H" or $\overline{OE}$ "H".
While, t_{Hz} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	—	8	pF	V_I=0V
Output Capacitance	C_O	—	10	pF	V_O=0V

6

OKI semiconductor

MSM38128A

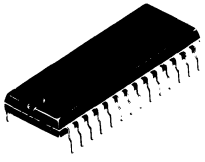
16,384 WORD x 8 BIT MASK ROM (E3-S-028-32)

GENERAL DESCRIPTION

The MSM38128ARS is an N-channel silicon gate MOS device MASK ROM with a 16,384 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
As it provides CE, OE, and CS as the control signal, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

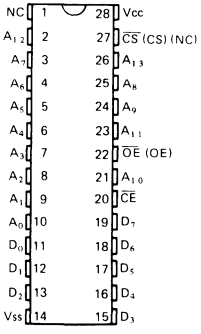
FEATURES

- 5V single power supply
- 16384 words x 8 bits
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

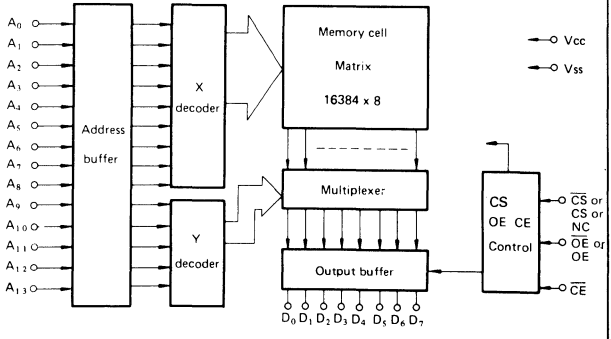
(Top View)



$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply
$A_0 \sim A_{13}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable
$\overline{CS}$	:	Chip select

Note: Please specify the $\overline{OE}$ active level and $\overline{CS}$ active level or open in ordering this IC.

FUNCTIONAL BLOCK DIAGRAM



6

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	Respect to V_{SS}
Output Voltage	V_O	−0.5 to 7	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	–	4.5	5	5.5	V
	V_{SS}	–	0	0	0	V
Input Signal Level	V_{IH}	–	2	5	6	V
	V_{IL}	–	−0.5	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	–	Vcc	V
	V_{OL}	I_{OL} = 2.1 mA	—	–	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	–	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	–	10	μA
Power Supply Current	IccA	Vcc = Max. I_O = 0 mA	–	–	100	mA
	Iccs	Vcc=Max. $\overline{CE}$=V_{IH}, I_O=0mA	–	–	30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = V_{CC} or V_{IH}	–	–	60	mA
Operating Temperature	T_{opr}	–	0	–	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

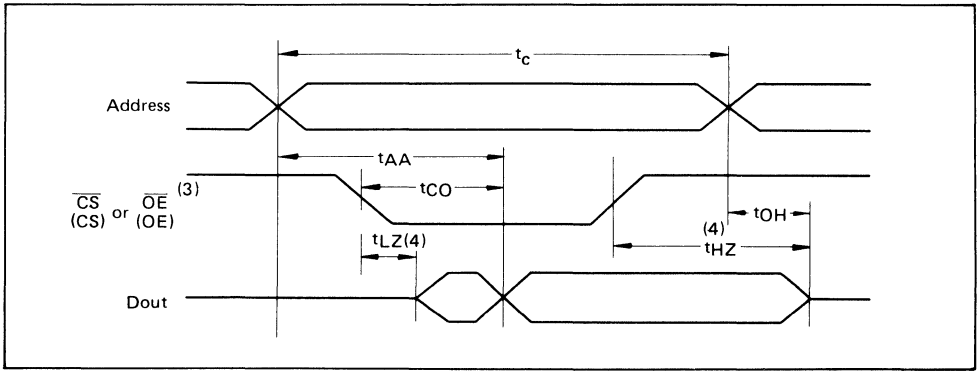
Parameter	Conditions
Input Signal Level	V_{IH}=2.4V, V_{IL}=0.6V
Input Rising, Falling Time	tr=tf= 5 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

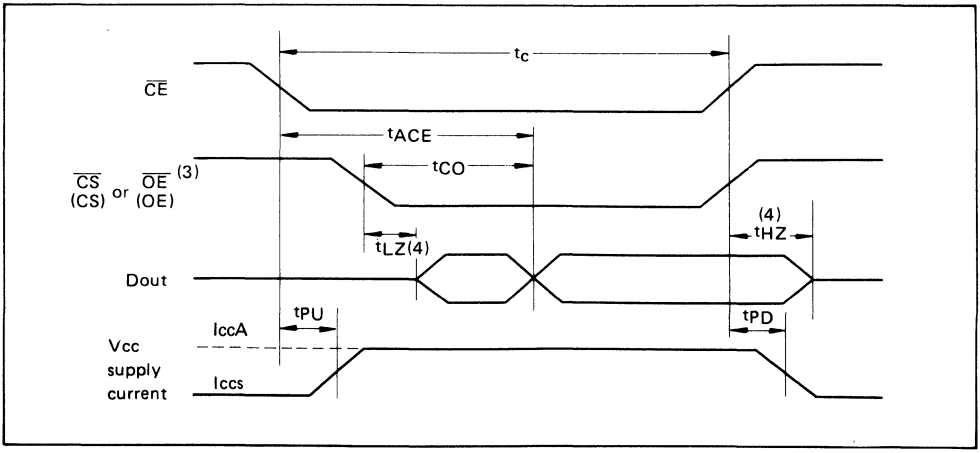
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	250	–	–	ns	
Address Access Time	t_{AA}	–	–	250	ns	
Chip Enable Access Time	t_{ACE}	–	–	250	ns	
Output Delay Time	t_{CO}	–	–	100	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	100	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	
Power Up Time	t_{PU}	0	–	–	ns	
Power Down Time	t_{PD}	–	–	100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) The $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{LZ} is determined by the later level, $\overline{CE}$ "L"/$\overline{CS}$ "L" or $\overline{OE}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H"/$\overline{CS}$ "H" or $\overline{OE}$ "H".
While, t_{HZ} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	—	8	pF	V_I=0V
Output Capacitance	C_O	—	10	pF	V_O=0V

6

OKI semiconductor

MSM38256

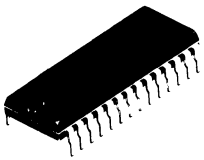
32768 WORD x 8 BIT MASK ROM (E3-S-029-32)

GENERAL DESCRIPTION

The MSM38256RS is an N-channel silicon gate MOS device ROM with a 32,768 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 30mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.
Since it provides CE, CS and OE signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

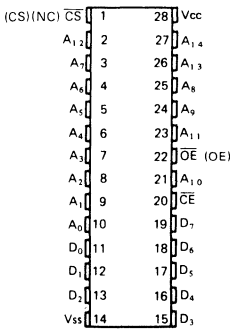
FEATURES

- 32768 words x 8 bits
- 5V single power supply
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

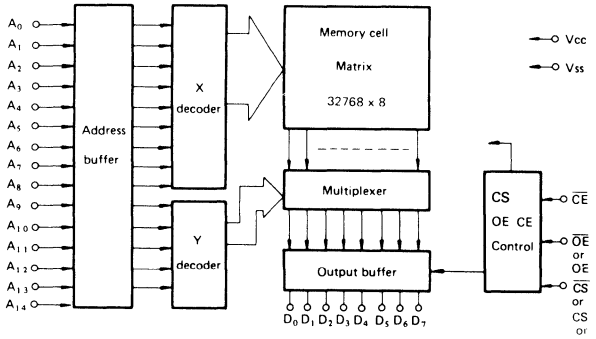
(Top View)



$\overline{CS}$	:	Chip Select
$\overline{OE}$	:	Output enable
Vcc, Vss	:	Power supply voltage
$A_0 \sim A_{14}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable

Note: The $\overline{OE}$ active level and $\overline{CS}$ active level are specified by customer.

FUNCTIONAL BLOCK DIAGRAM



6

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	
Output Voltage	V_O	−0.5 to 7	V	
Power Dissipation	PD	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{cc}	—	4.5	5	5.5	V
	V_{ss}	—	0	0	0	V
Input Signal Level	V_{IH}	—	2	5	6	V
	V_{IL}	—	−0.5	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	—	Vcc	V
	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{cc}	−10	—	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	—	10	μA
Power Supply Current	IccA	Vcc = Max. I_O = 0 mA	—	—	120	mA
	Iccs	Vcc = Max. $\overline{CE}$ = VIH, Io = 0 mA	—	—	30	mA
Peak Power ON Current	Ipo	Vcc = GND ~ Vcc Min. $\overline{CE}$ = V_{CC} or V_{IH}	—	—	60	mA
Operating Temperature	T_{opr}		0	—	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

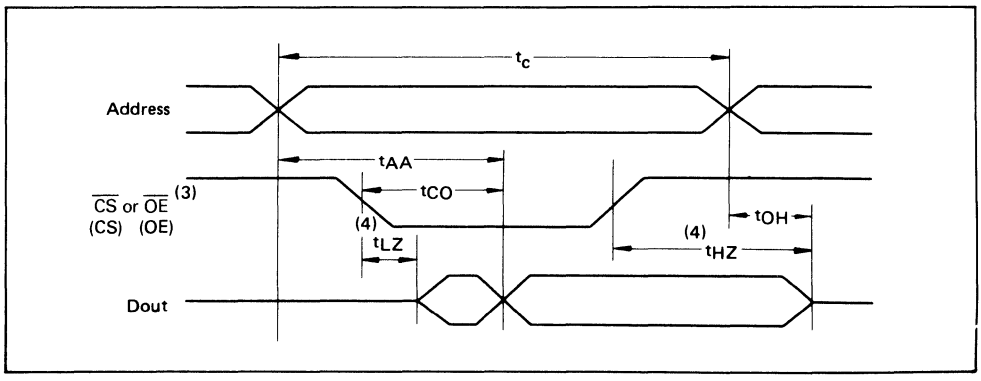
Parameter	Conditions
Input Signal Level	V_{IH}=2.4V, V_{IL}=0.6V
Input Rising, Falling Time	tr=tf = 5 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8 & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

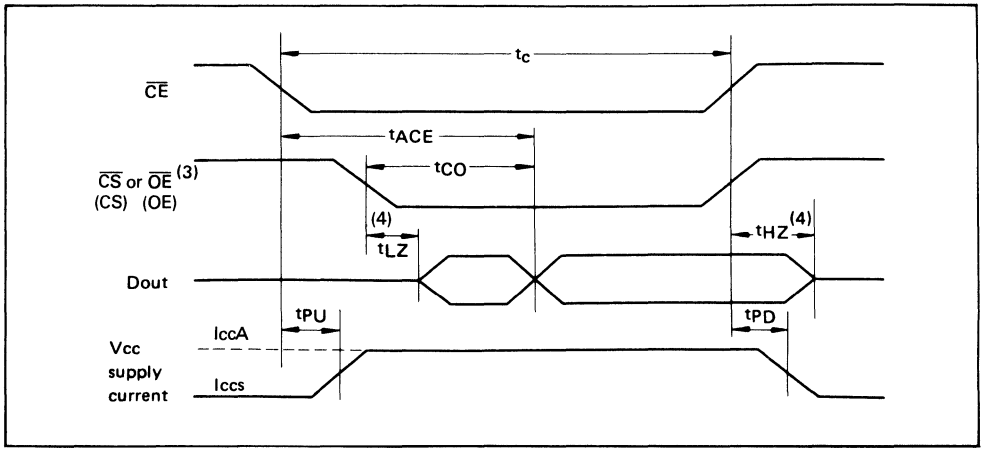
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_c	250	—	—	ns	
Address Access Time	t_{AA}	—	—	250	ns	
Chip Enable Access Time	t_{ACE}	—	—	250	ns	
Output Delay Time	t_{CO}	—	—	100	ns	
Output Setting Time	t_{LZ}	10	—	—	ns	
Output Disable Time	t_{HZ}	10	—	100	ns	
Output Retaining Time	t_{OH}	10	—	—	ns	
Power Up Time	t_{PU}	0	—	—	ns	
Power Down Time	t_{PD}	—	—	100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) $\overline{OE}$ and $\overline{CS}$ are shown in the negative logic here, however the active level is freely selected.
(4) t_{LZ} is determined by the later $\overline{CE}$ "L", $\overline{OE}$ "L" or $\overline{CS}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H", $\overline{OE}$ "H" or $\overline{CS}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	—	8	pF	V_I=0V
Output Capacitance	C_O	—	10	pF	V_O=0V

6

OKI semiconductor

MSM38256A

32768 WORD x 8 BIT MASK ROM (E3-S-030-32)

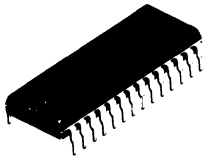
GENERAL DESCRIPTION

The MSM38256ARS is an N-channel silicon gate E/DMOS device ROM with a 32,768 word x 8 bit capacity. It operates on a 5V single power supply and the all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation which is as low as 6mA (max) when the chip is not selected. The application of a byte system and the pin compatibility with standard UV EPROMs make the device most suitable for use as a large-capacity fixed memory for microcomputers and data terminals.

Since it provides CE, OE, CS signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

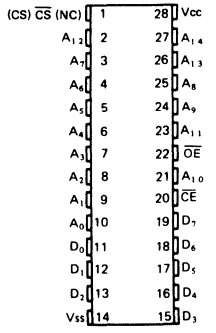
FEATURES

- 32768 words x 8 bits
- 5V single power supply
- Access time: 150 ns MAX
- Input/output TTL compatible
- 3-state output
- Power down mode
- 28-pin DIP



PIN CONFIGURATION

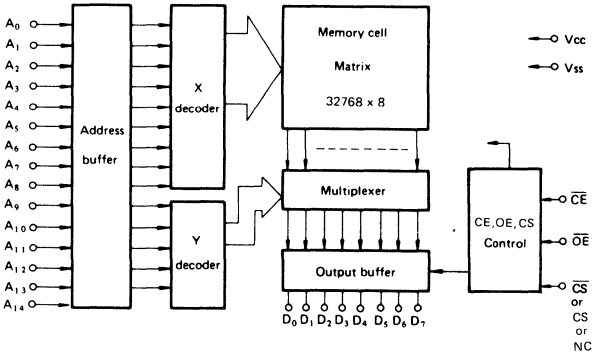
(Top View)



$\overline{CE}$	:	Chip enable
$\overline{OE}$	:	Output enable
(CS) $\overline{CS}$	:	Chip select
Vcc, Vss	:	Power supply voltage
$A_0 \sim A_{14}$	:	Address input
$D_0 \sim D_7$	:	Data output
(NC)	:	No Connection

Note: $\overline{CS}$ active level is specified by customers.

FUNCTIONAL BLOCK DIAGRAM



6

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.5 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.5 to 7	V	
Output Voltage	V_O	−0.5 to 7	V	
Power Dissipation	PD	1.0	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	
Storage Temperature	T_{stg}	−55 to 150	°C	

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Conditions	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	—	4.5	5	5.5	V
	V_{SS}	—	0	0	0	V
Input Signal Level	V_{IH}	—	2.2	5	6	V
	V_{IL}	—	−0.5	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	—	V_{CC}	V
	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	—	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or V_{CC} Chip not selected	−10	—	10	μA
Power Supply Current	IccA	V_{CC} = Max. I_O = 0 mA	—	—	60	mA
	I_{CCS}	Vcc = Max. $\overline{CE}$ = VIH, Io = 0 mA	—	—	6	mA
Peak Power On Current	I_{PO}	V_{CC} = GND ~ V_{CC} Min. CE = V_{CC} or V_{IH}	—	—	60	mA
Operating Temperature	Topr		0	—	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

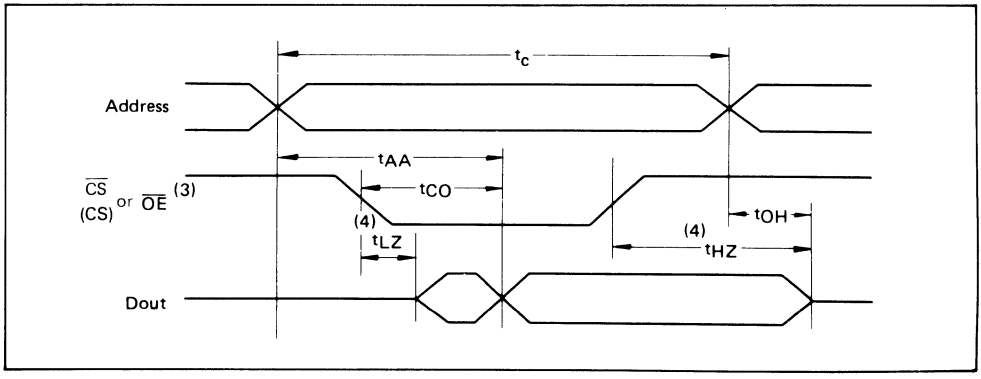
Parameter	Conditions
Input Signal Level	V_{IH}=2.4V, V_{IL}=0.6V
Input Rising, Falling Time	tr=tf= 5 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8 & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

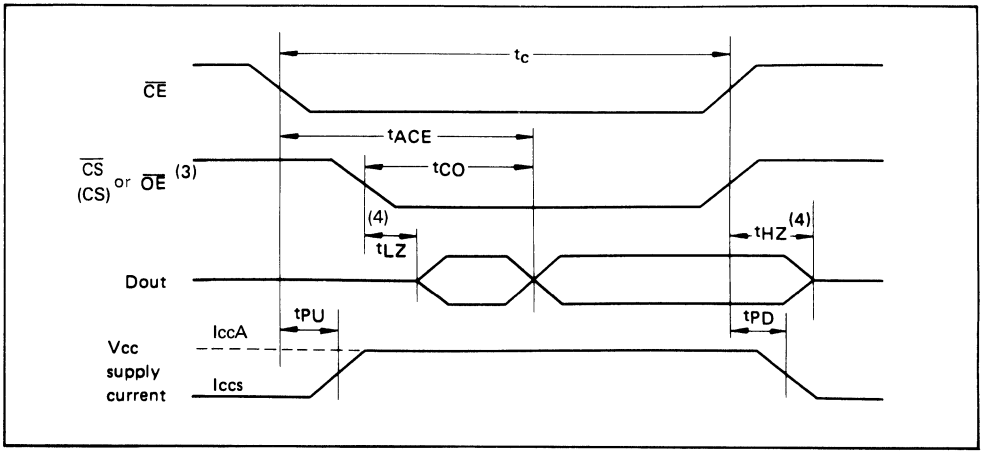
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_c	150	—	—	ns	
Address Access Time	t_{AA}	—	—	150	ns	
Chip Enable Access Time	t_{ACE}	—	—	150	ns	
Output Delay Time	t_{CO}	—	—	55	ns	
Output Setting Time	t_{LZ}	10	—	—	ns	
Output Disable Time	t_{HZ}	10	—	50	ns	
Output Retaining Time	t_{OH}	10	—	—	ns	
Power Up Time	t_{PU}	0	—	—	ns	
Power Down Time	t_{PD}	—	—	100	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) $\overline{CS}$ is shown in the negative logic here, however the active level is freely selected.
(4) t_{LZ} is determined by the later $\overline{CE}$ "L", $\overline{OE}$ "L" or $\overline{CS}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H", $\overline{OE}$ "H" or $\overline{CS}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	—	8	pF	V_I=0V
Output Capacitance	C_O	—	6	pF	V_O=0V

OKI semiconductor

MSM53256

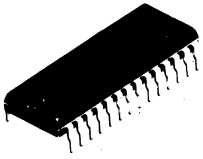
32,768 WORD x 8 BIT MASK ROM

GENERAL DESCRIPTION

The MSM53256RS is a silicon gate CMOS device ROM with 32,768 words x 8 bit capacity. It operates on a 5V single power supply and all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation when the chip is not selected. The application of a byte system is most suitable for use as a large capacity fixed memory for microcomputers and data terminals.
Since it provides signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

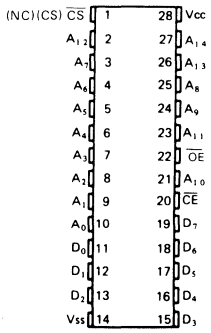
FEATURES

- 256k bits: 32,768 words x 8 bits
- High speed: access time 150 ns max
- Low power: active current 15 mA max
  standby current 0.1 mA max
- Wide tolerance operating: Vcc = 5V ± 10%
- Fully static operating: using no clock
- Fully TTL compatible
- Pin compatible to 256k EPROM
- Packaged to 28 pins plastic
- Fabricated with CMOS silicon gate technology



PIN CONFIGURATION

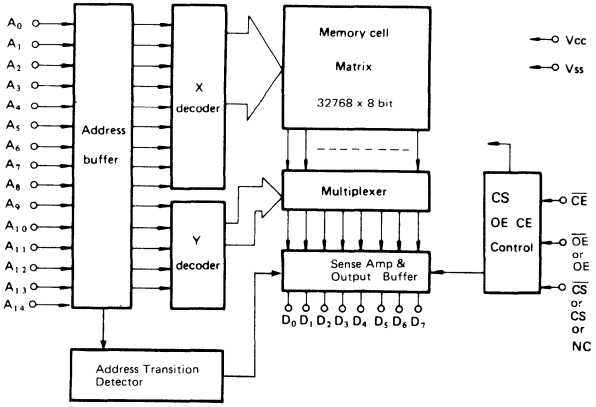
(Top View)



$\overline{CS}$	: Chip select
$\overline{OE}$	: Output enable
Vcc, Vss	: Power supply voltage
$A_0 \sim A_{14}$	: Address input
$D_0 \sim D_7$	: Data output
$\overline{CE}$	: CHip enable

Note: $\overline{CS}$ active level is specified by customer.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	−0.3 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Output Voltage	V_O	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	—
Storage Temperature	T_{stg}	−55 to 150	°C	—

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	—	4.5	5	5.5	V
	V_{SS}	—	0	0	0	V
Input Signal Level	V_{IH}	—	2.2	5	Vcc +0.3	V
	V_{IL}	—	−0.3	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	—	—	V
	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	—	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	—	10	μA
Power Supply Current	I_{CCA}	Vcc = Max. I_O = 0 mA, t_C = 150 ns	—	—	15	mA
	I_{CCS}	Vcc = Max. $\overline{CE}$ = Vcc − 0.2V	—	—	100	μA
	I_{CCS1}	Vcc = Max. $\overline{CE}$ = V_{IH} min.	—	—	500	μA
Operating Temperature	T_{opr}	—	0	—	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

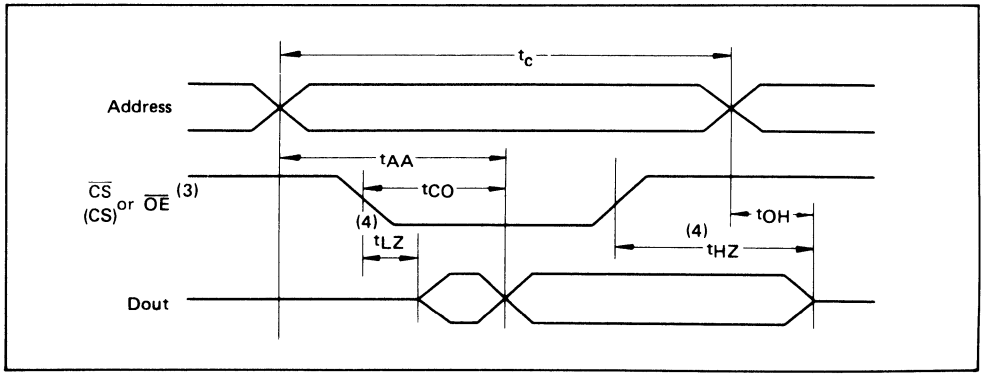
Parameter	Conditions
Input Signal Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rising, Falling Time	tr=tf= 5 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

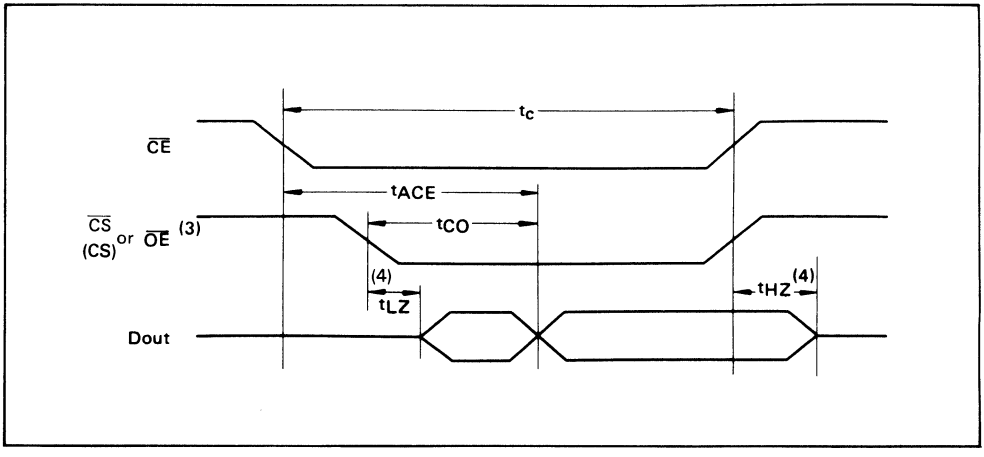
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	150	—	—	ns	
Address Access Time	t_{AA}	—	—	150	ns	
Chip Enable Access Time	t_{ACE}	—	—	150	ns	
Output Delay Time	t_{CO}	—	—	50	ns	
Output Setting Time	t_{LZ}	10	—	—	ns	
Output Disable Time	t_{HZ}	10	—	50	ns	
Output Retaining Time	t_{OH}	10	—	—	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) $\overline{CS}$ is shown in the negative logic here, however the active level is freely selected.
(4) t_{LZ} is determined by the later $\overline{CE}$ "L", $\overline{OE}$ "L" or $\overline{CS}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H", $\overline{OE}$ "H" or $\overline{CS}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	—	8	pF	V_I=0V
Output Capacitance	C_O	—	6	pF	V_O=0V

6

OKI semiconductor

MSM531000

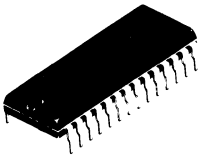
131,072 WORD x 8 BIT MASK ROM (E3-S-031-32)

GENERAL DESCRIPTION

The MSM531000RS is a silicon gate CMOS device ROM with 131,072 words x 8 bit capacity. It operates on a 5V single power supply and all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation when the chip is not selected. The application of a byte system is most suitable for use as a large capacity fixed memory for microcomputers and data terminals.
Since it provides signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control.

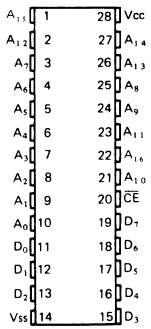
FEATURES

- 131,072 words x 8 bits
- 5V single power supply
- Access time: 250 ns MAX
- Input/output TTL compatible
- 3-state output
- 28-pin DIP



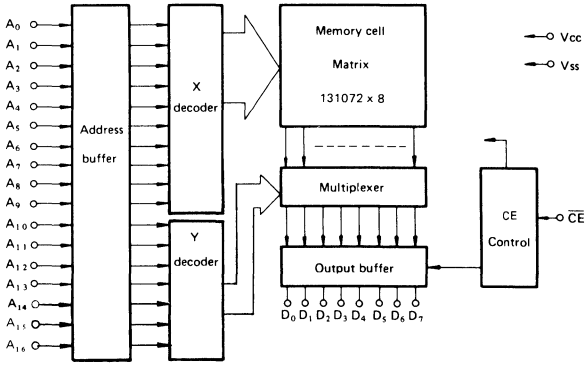
PIN CONFIGURATION

(Top View)



Vcc, Vss : Power supply voltage
$A_0 \sim A_{16}$: Address input
$D_0 \sim D_7$: Data output
$\overline{CE}$: Chip enable

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	V_{CC}	−0.3 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Output Voltage	V_O	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	—
Storage Temperature	T_{stg}	−55 to 150	°C	—

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	—	4.5	5	5.5	V
	V_{SS}	—	0	0	0	V
Input Signal Level	V_{IH}	—	2.2	5	Vcc +0.3	V
	V_{IL}	—	−0.3	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	—	—	V
	V_{OL}	I_{OL} = 2.1 mA	—	—	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	—	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	—	10	μA
Power Supply Current	I_{CCA}	Vcc = Max. I_O = 0 mA, t_C = 250 ns	—	—	15	mA
	I_{CCS}	Vcc = Max. $\overline{CE}$ = Vcc − 0.2V	—	—	100	μA
	I_{CCS1}	Vcc = Max. $\overline{CE}$ = V_{IH} min.	—	—	500	μA
Operating Temperature	T_{opr}	—	0	—	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

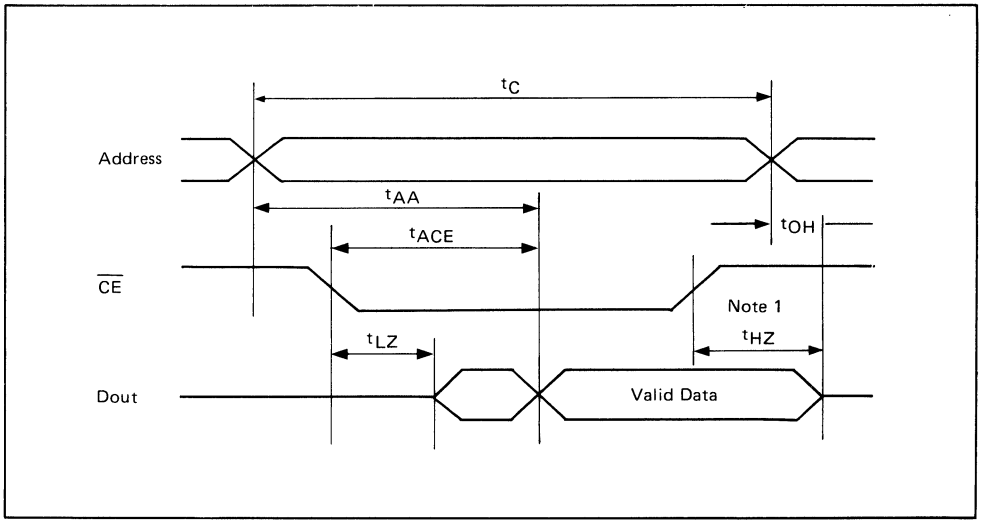
Parameter	Conditions
Input Signal Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rising, Falling Time	tr=tf=5 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	250	–	–	ns	
Address Access Time	t_{AA}	–	–	250	ns	
Chip Enable Access Time	t_{ACE}	–	–	250	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	80	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	

READ CYCLE



Note: t_{HZ} shows the time until floating and it is therefore not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	–	8	pF	V_I=0V
Output Capacitance	C_O	–	6	pF	V_O=0V

OKI semiconductor

MSM531001

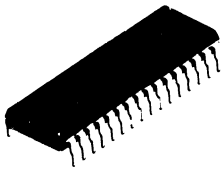
131,072 WORD x 8 BIT MASK ROM

GENERAL DESCRIPTION

The MSM531001 is a silicon gate CMOS device ROM with 131,072 words x 8 bit capacity. It operates on a 5V single powe supply and all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires n external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipatio when the chip is not selected. The application of a byte system is most suitable for use as a large capacity fixed memory fc microcomputers and data terminals.
Since it provides signals, the connection of output terminals of other chips with the wired OR is possible ensuring an eas expand operation of memory and bus line control.

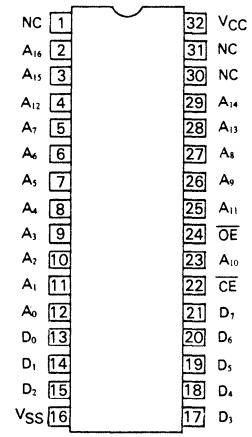
FEATURES

- 131,072 words x 8 bits
- 5V single power supply
- Access time: 200 ns MAX
- Input/output TTL compatible
- 3-state output
- 32 pin DIP



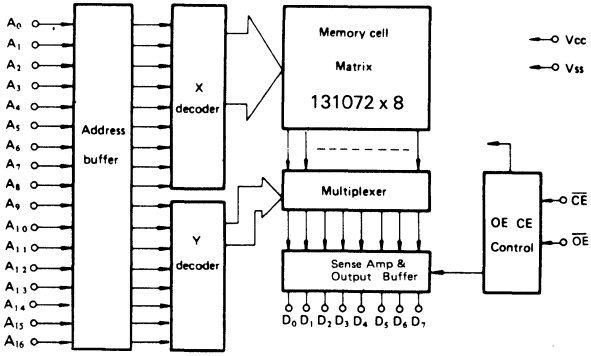
PIN CONFIGURATION

(Top View)



V_{CC}, V_{SS}	:	Power supply voltage
$A_0 \sim A_{16}$	:	Address input
$D_0 \sim D_7$	:	Data output
$\overline{CE}$	:	Chip enable
$\overline{OE}$	:	Output enable

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Conditions
Power Supply Voltage	Vcc	−0.3 to 7	V	Respect to V_{SS}
Input Voltage	V_I	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Output Voltage	V_O	−0.3 to Vcc + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	T_{opr}	0 to 70	°C	–
Storage Temperature	T_{stg}	−55 to 150	°C	–

OPERATING CONDITION AND DC CHARACTERISTICS

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	–	4.5	5	5.5	V
	V_{SS}	–	0	0	0	V
Input Signal Level	V_{IH}	–	2.2	5	Vcc +0.3	V
	V_{IL}	–	−0.3	0	0.8	V
Output Signal Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
	V_{OL}	I_{OL} = 2.1 mA	–	–	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	−10	–	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or Vcc Chip not selected	−10	–	10	μA
Power Supply Current	I_{CCA}	Vcc = Max. I_O = 0 mA, t_C = 200 ns	–	–	30	mA
	I_{CCS}	Vcc = Max. $\overline{CE}$ = Vcc − 0.2V	–	–	50	μA
	I_{CCS1}	Vcc = Max. $\overline{CE}$ = V_{IH} min.	–	–	500	μA
Operating Temperature	T_{opr}	–	0	–	70	°C

AC CHARACTERISTICS

TIMING CONDITIONS

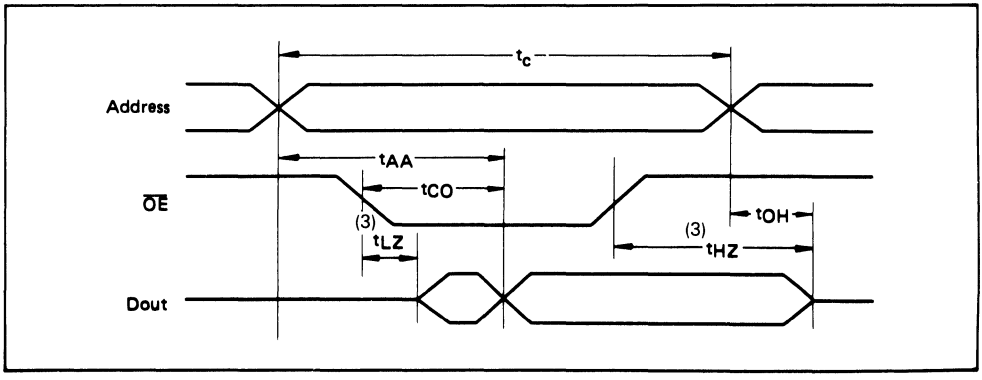
Parameter	Conditions
Input Signal Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rising, Falling Time	tr=tf= 5 ns
Timing Measuring Point Voltage	Input Voltage=1.5V
	Output Voltage=0.8V & 2.0V
Loading Condition	C_L=100 pF + 1 TTL

READ CYCLE

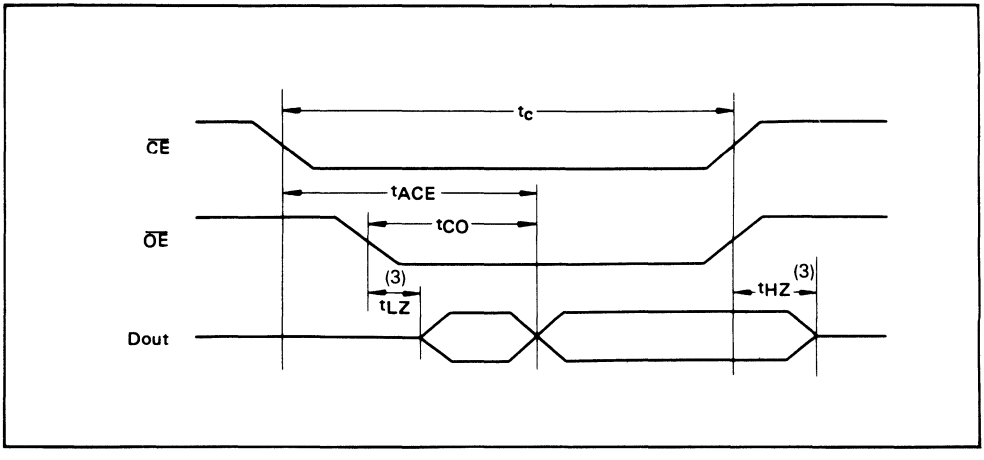
(V_{CC} = 5V ±10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	200	—	—	ns	
Address Access Time	t_{AA}	—	—	200	ns	
Chip Enable Access Time	t_{ACE}	—	—	200	ns	
Output Delay Time	t_{CO}	—	—	60	ns	
Output Setting Time	t_{LZ}	10	—	—	ns	
Output Disable Time	t_{HZ}	10	—	50	ns	
Output Retaining Time	t_{OH}	10	—	—	ns	

1) READ CYCLE-1 (1)



2) READ CYCLE-2 (2)



Notes: (1) $\overline{CE}$ is "L" level.
(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.
(3) t_{LZ} is determined by the later $\overline{CE}$ "L", $\overline{OE}$ "L"
t_{HZ} is determined by the earlier $\overline{CE}$ "H", $\overline{OE}$ "H"
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	—	8	pF	V_I=0V
Output Capacitance	C_O	—	6	pF	V_O=0V

OKI semiconductor
MSM534000

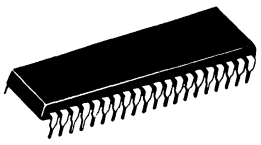
262,144 WORD x 16 BIT MASK ROM

GENERAL DESCRIPTION

The MSM534000RS is a silicon gate CMOS device ROM with 262,144 words x 16 bit capacity. It operates on a 5V single power supply and all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation when the chip is not selected. The application of a word system is most suitable for use as a large capacity fixed memory for microcomputers and data terminals.
Since it provides signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control

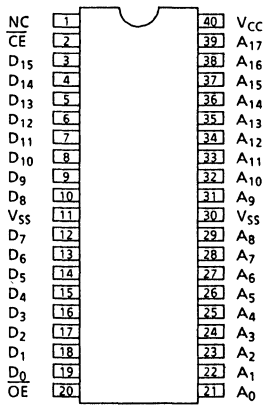
FEATURES

- 262,144 words x 16 bits
- 5V single power supply
- Access time: 200 ns MAX
- Input/output TTL compatible
- 3-state output
- 40-pin DIP



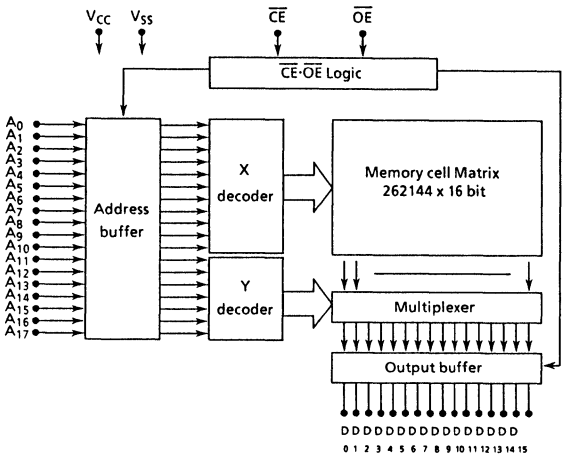
PIN CONFIGURATION

(Top View)



V_{CC}, V_{SS} :Power supply voltage
A_0~A_{17} :Address input
D_0~D_{15} :Data output
$\overline{CE}$:Chip enable
OE :Output enable

FUNCTION BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Condition
Power Supply Voltage	V_{CC}	− 0.3 to 7	V	Respect to V_{SS}
Input Voltage	V_I	− 0.3 to V_{CC} + 0.3	V	Respect to V_{SS}
Output Voltage	V_O	− 0.3 to V_{CC} + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	Topr	0 to 70	°C	−
Storage Temperature	Tstg	− 55 to 150	°C	−

OPERATING CONDITION AND DC CHARACTERISTICS

(V_{CC} = 5V ± 10% V_{SS} = 0V Ta = 0°C to + 70°C)

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	−	4.5	5	5.5	V
	V_{SS}	−	0	0	0	V
Input Signal Level	V_{IH}	−	2.2	5	V_{CC} + 0.3	V
	V_{IL}	−	− 0.3	0	0.8	V
Output signal Level	V_{OH}	I_{OH} = − 400μA	2.4	−	−	V
	V_{OL}	I_{OL} = 2.1 mA	−	−	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	− 10	−	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or V_{CC} Chip not selected	− 10	−	10	μA
Power Supply Current	I_{CCA}	V_{CC} = Max, I_O = 0mA t_C = 200 ns	−	−	50	mA
	I_{CCS}	$\overline{CE}$ = V_{CC} − 0.2V	−	−	50	μA
	I_{CCS1}	$\overline{CE}$ = V_{IH} min.	−	−	500	μA
Operating Temperature	Topr	−	0	−	70	°C

AC CHARACTERISTICS

<TIMING CONDITIONS>

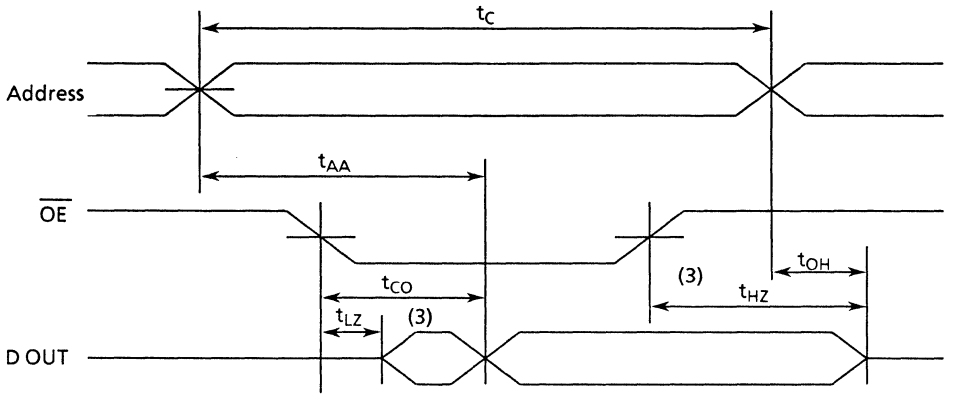
Parameter	Condition
Input Signal Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rising, Falling Time	tr = tf = 5 ns
Timing Measuring Point Voltage	Input Voltage = 1.5V
	Output Voltage = 0.8V & 2.0V
Loading Condition	C_L = 100pF + 1 TTL

<READ CYCLE>

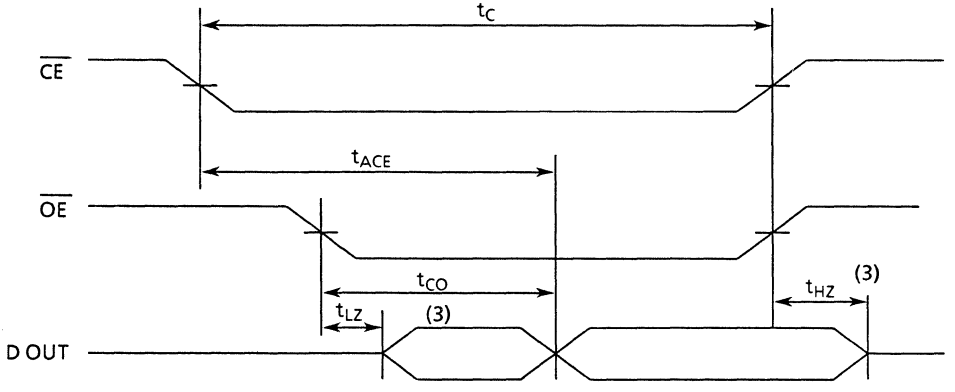
(V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	200	–	–	ns	
Address Access Time	t_{AA}	–	–	200	ns	
Chip Enable Access Time	t_{ACE}	–	–	200	ns	
Output Delay Time	t_{CO}	–	–	60	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	50	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	

- READ CYCLE-1 (NOTE 1)



- READ CYCLE-1 (NOTE 2)



Notes: (1) $\overline{CE}$ is "L" level.

(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.

(3) t_{LZ} is determined by the later $\overline{CE}$ "L" or $\overline{OE}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H" or $\overline{OE}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	–	8	pF	V_I = 0V
Output Capacitance	C_O	–	8	pF	V_O = 0V

OKI semiconductor
MSM534000A

262,144 WORD x 16 BIT MASK ROM

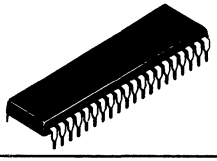
GENERAL DESCRIPTION

The MSM534000ARS is a silicon gate CMOS device ROM with 262,144 words x 16 bit capacity. It operates on a 5V single power supply and all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation when the chip is not selected. The application of a word system is most suitable for use as a large capacity fixed memory for microcomputers and data terminals.
Since it provides signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control

FEATURES

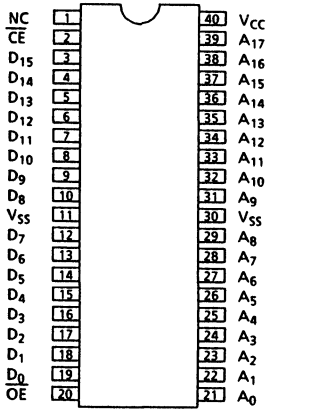
- 262,144 words x 16 bits
- 5V single power supply
- Access time: 150 ns MAX
- Input/output TTL compatible
- 3-state output
- 40-pin DIP

6



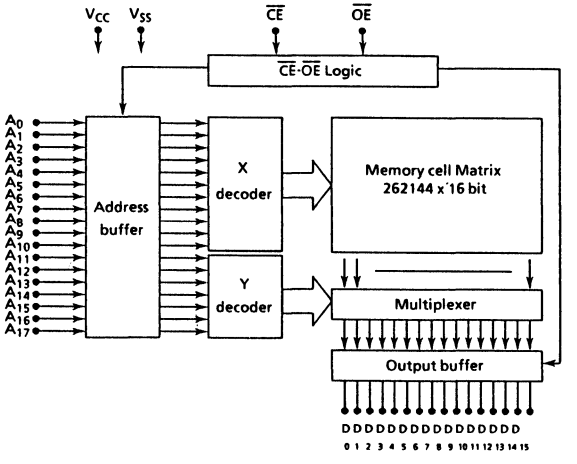
PIN CONFIGURATION

(Top View)



V_{CC}, V_{SS} :Power supply voltage
A_0~A_{17} :Address input
D_0~D_{15} :Data output
$\overline{CE}$:Chip enable
$\overline{OE}$:Output enable

FUNCTION BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Condition
Power Supply Voltage	V_{CC}	− 0.3 to 7	V	Respect to V_{SS}
Input Voltage	V_I	− 0.3 to V_{CC} + 0.3	V	Respect to V_{SS}
Output Voltage	V_O	− 0.3 to V_{CC} + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	Topr	0 to 70	°C	−
Storage Temperature	Tstg	− 55 to 150	°C	−

OPERATING CONDITION AND DC CHARACTERISTICS

(V_{CC} = 5V ± 10% V_{SS} = 0V Ta = 0°C to + 70°C)

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	−	4.5	5	5.5	V
	V_{SS}	−	0	0	0	V
Input Signal Level	V_{IH}	−	2.2	5	V_{CC} + 0.3	V
	V_{IL}	−	− 0.3	0	0.8	V
Output signal Level	V_{OH}	I_{OH} = − 400μA	2.4	−	−	V
	V_{OL}	I_{OL} = 2.1 mA	−	−	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	− 10	−	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or V_{CC} Chip not selected	− 10	−	10	μA
Power Supply Current	I_{CCA}	V_{CC} = Max, I_O = 0mA t_C = 150 ns	−	−	50	mA
	I_{CCS}	$\overline{V_{CC}}$ = Max. $\overline{CE}$ = V_{CC} − 0.2V	−	−	50	μA
	I_{CCS1}	$\overline{V_{CC}}$ = Max. $\overline{CE}$ = V_{IH} min.	−	−	500	μA
Operating Temperature	Topr	−	0	−	70	°C

6

AC CHARACTERISTICS

<TIMING CONDITIONS>

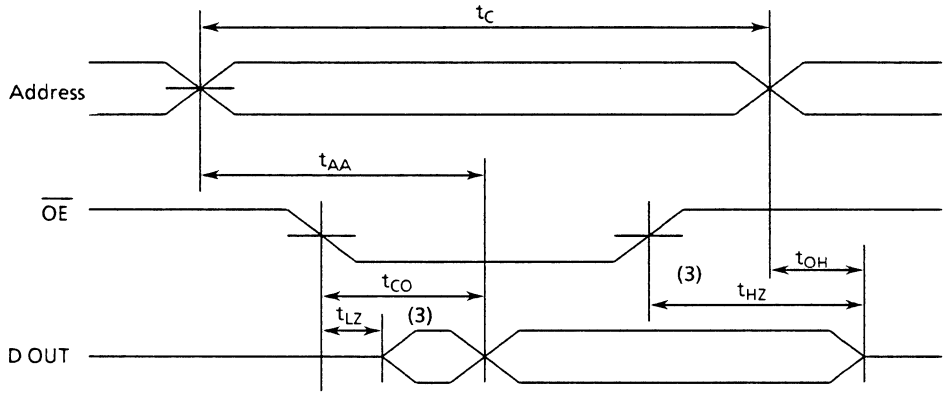
Parameter	Condition
Input Signal Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rising, Falling Time	tr = tf = 5 ns
Timing Measuring Point Voltage	Input Voltage = 1.5V
	Output Voltage = 0.8V & 2.0V
Loading Condition	C_L = 100pF + 1 TTL

<READ CYCLE>

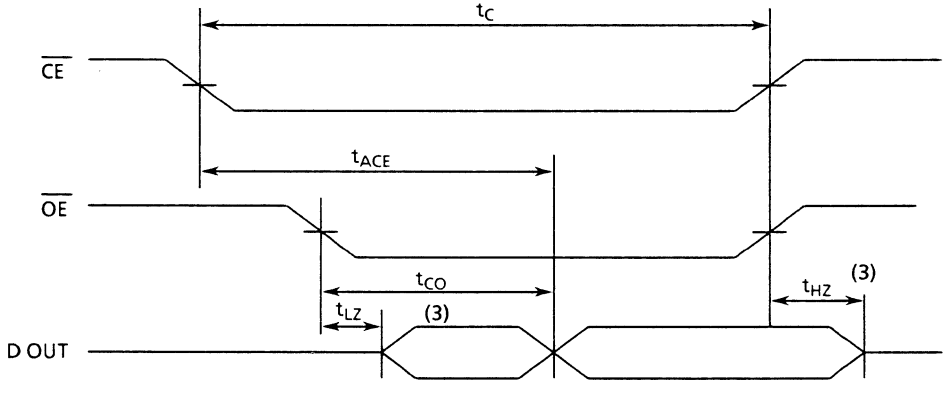
(V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	150	–	–	ns	
Address Access Time	t_{AA}	–	–	150	ns	
Chip Enable Access Time	t_{ACE}	–	–	150	ns	
Output Delay Time	t_{CO}	–	–	60	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	50	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	

- READ CYCLE-1 (NOTE 1)



- READ CYCLE-1 (NOTE 2)



Notes: (1) $\overline{CE}$ is "L" level.

(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.

(3) t_{LZ} is determined by the later $\overline{CE}$ "L" or $\overline{OE}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H" or $\overline{OE}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C , f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	–	8	pF	V_I = 0V
Output Capacitance	C_O	–	8	pF	V_O = 0V

PRELIMINARY

OKI semiconductor
MSM534001A

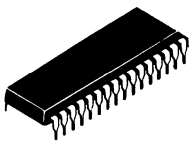
524,288 WORD x 8 BIT MASK ROM

GENERAL DESCRIPTION

The MSM534001ARS is a silicon gate CMOS device ROM with 524,288 words x 8 bit capacity. It operates on a 5V single power supply and all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation when the chip is not selected. The application of a byte system is most suitable for use as a large capacity fixed memory for microcomputers and data terminals.
Since it provides signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control

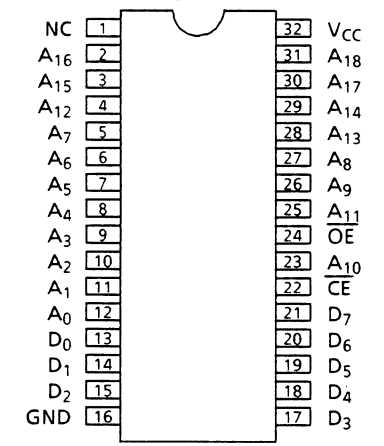
FEATURES

- 524,288 words x 8 bits
- 5V single power supply
- Access time: 150 ns MAX
- Input/output TTL compatible
- 3-state output
- 32-pin DIP



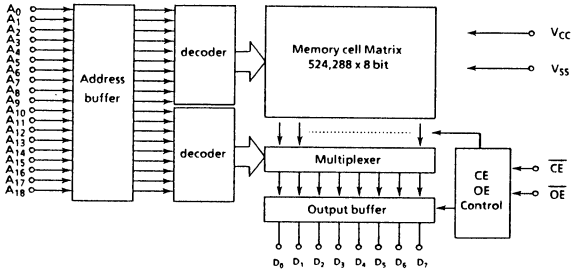
PIN CONFIGURATION

(Top View)



V_{CC}, V_{SS} :Power supply voltage
A_0~A_{18} :Address input
D_0~D_7 :Data output
$\overline{CE}$:Chip enable
OE :Output enable

FUNCTION BLOCK DIAGRAM



6

ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Condition
Power Supply Voltage	V_{CC}	− 0.3 to 7	V	Respect to V_{SS}
Input Voltage	V_I	− 0.3 to V_{CC} + 0.3	V	Respect to V_{SS}
Output Voltage	V_O	− 0.3 to V_{CC} + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	Topr	0 to 70	°C	−
Storage Temperature	Tstg	− 55 to 150	°C	−

OPERATING CONDITION AND DC CHARACTERISTICS

(V_{CC} = 5V ± 10% V_{SS} = 0V Ta = 0°C to + 70°C)

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	−	4.5	5	5.5	V
	V_{SS}	−	0	0	0	V
Input Signal Level	V_{IH}	−	2.2	5	V_{CC} + 0.3	V
	V_{IL}	−	− 0.3	0	0.8	V
Output signal Level	V_{OH}	I_{OH} = − 400μA	2.4	−	−	V
	V_{OL}	I_{OL} = 2.1 mA	−	−	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	− 10	−	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or V_{CC} Chip not selected	− 10	−	10	μA
Power Supply Current	I_{CCA}	V_{CC} = Max, I_O = 0mA t_C = 150 ns	−	−	50	mA
	I_{CCS}	$\overline{V_{CC}}$ = Max. $\overline{CE}$ = V_{CC} − 0.2V	−	−	50	μA
	I_{CCS1}	$\overline{V_{CC}}$ = Max. $\overline{CE}$ = V_{IH} min.	−	−	500	μA
Operating Temperature	Topr	−	0	−	70	°C

AC CHARACTERISTICS

<TIMING CONDITIONS>

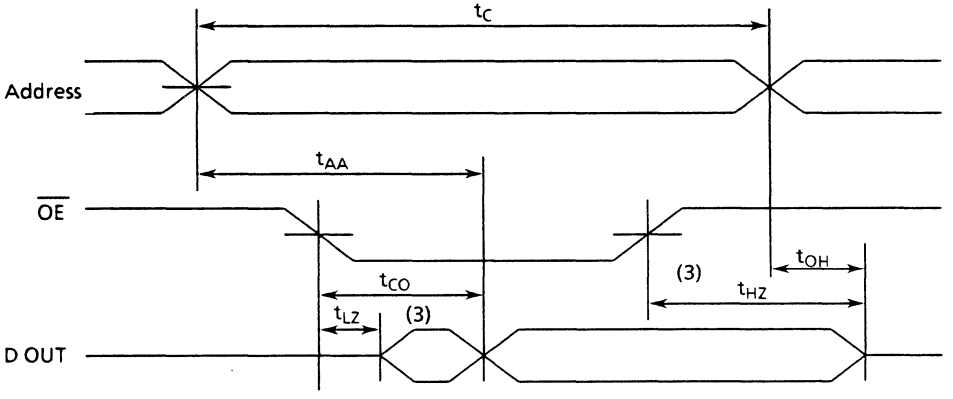
Parameter	Condition
Input Signal Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rising, Falling Time	tr = tf = 5 ns
Timing Measuring Point Voltage	Input Voltage = 1.5V
	Output Voltage = 0.8V & 2.0V
Loading Condition	C_L = 100pF + 1 TTL

<READ CYCLE>

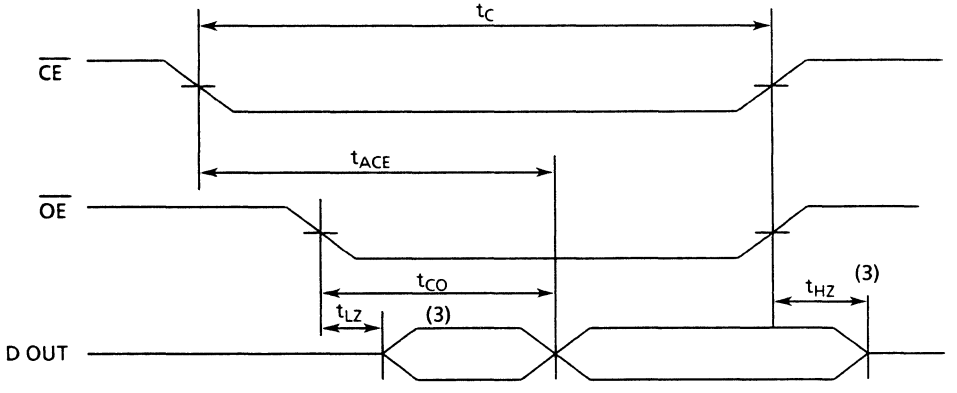
(V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0°C to + 70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	150	–	–	ns	
Address Access Time	t_{AA}	–	–	150	ns	
Chip Enable Access Time	t_{ACE}	–	–	150	ns	
Output Delay Time	t_{CO}	–	–	60	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	50	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	

- READ CYCLE-1 (NOTE 1)



- READ CYCLE-1 (NOTE 2)



Notes: (1) $\overline{CE}$ is "L" level.

(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.

(3) t_{LZ} is determined by the later $\overline{CE}$ "L" or $\overline{OE}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H" or $\overline{OE}$ "H"
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C , f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	–	8	pF	V_I = 0V
Output Capacitance	C_O	–	8	pF	V_O = 0V

OKI semiconductor
MSM534002A

262,144 WORD x 16 BIT OR 524,288 WORD x 8 BIT MASK ROM

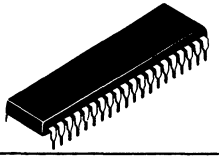
GENERAL DESCRIPTION

The MSM534002ARS is a silicon gate CMOS device ROM with 262,144 words x 16 bit or 524,288 words x 8 bit capacity. It operates on a 5V single power supply and all inputs and outputs are TTL compatible. The adoption of an asynchronous system in the circuit requires no external clock assuring extremely easy operation. The availability of power down mode contributes to the low power dissipation when the chip is not selected. The application of a byte/word system is most suitable for use as a large capacity fixed memory for microcomputers and data terminals.
Since it provides signals, the connection of output terminals of other chips with the wired OR is possible ensuring an easy expand operation of memory and bus line control

FEATURES

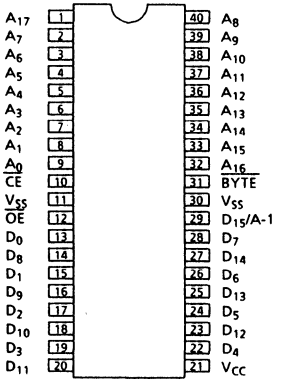
- 262,144 words x 16 bits or 524,288 words x 8 bits
- 5V single power supply
- Access time: 150 ns MAX
- Input/output TTL compatible
- 3-state output
- 40-pin DIP

6



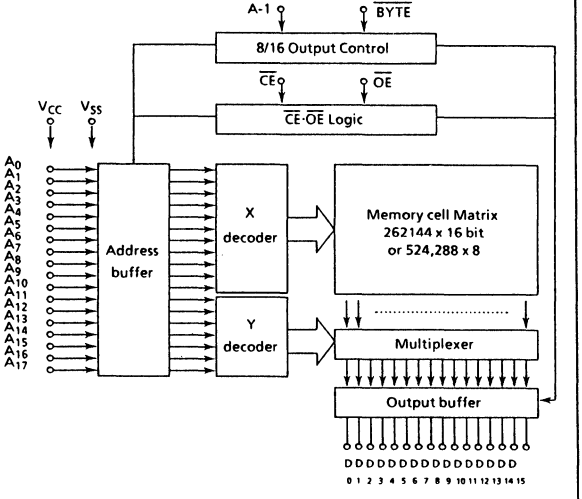
PIN CONFIGURATION

(Top View)



V_{CC}, V_{SS} :Power supply voltage
A_0~A_{17}:Address input
D_0~D_{14}:Data output
$\overline{CE}$: Chip enable
$\overline{OE}$: Output enable
D_{15}/A-1: Output/Input
$\overline{BYTE}$: Mode Switch

FUNCTION BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Ta = 25°C)

Rating	Symbol	Value	Unit	Condition
Power Supply Voltage	V_{CC}	− 0.3 to 7	V	Respect to V_{SS}
Input Voltage	V_I	− 0.3 to V_{CC} + 0.3	V	Respect to V_{SS}
Output Voltage	V_O	− 0.3 to V_{CC} + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	Topr	0 to 70	°C	-
Storage Temperature	Tstg	− 55 to 150	°C	-

OPERATING CONDITION AND DC CHARACTERISTICS

(V_{CC} = 5V ± 10% V_{SS} = 0V Ta = 0°C to + 70°C)

Parameter	Symbol	Measuring Condition	Rating			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	V_{CC}	-	4.5	5	5.5	V
	V_{SS}	-	0	0	0	V
Input Signal Level	V_{IH}	-	2.2	5	V_{CC} + 0.3	V
	V_{IL}	-	− 0.3	0	0.8	V
Output signal Level	V_{OH}	I_{OH} = − 400μA	2.4	-	-	V
	V_{OL}	I_{OL} = 2.1 mA	-	-	0.4	V
Input Leakage Current	I_{LI}	V_I = 0V or V_{CC}	− 10	-	10	μA
Output Leakage Current	I_{LO}	V_O = 0V or V_{CC} Chip not selected	− 10	-	10	μA
Power Supply Current	I_{CCA}	V_{CC} = Max, I_O = 0mA t_C = 150 ns	-	-	50	mA
	I_{CCS}	$\overline{V_{CC}}$ = Max. $\overline{CE}$ = V_{CC} − 0.2V	-	-	50	μA
	I_{CCS1}	$\overline{V_{CC}}$ = Max. $\overline{CE}$ = V_{IH} min.	-	-	500	μA
Operating Temperature	Topr	-	0	-	70	°C

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FUNCTION TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A-1 (D15)	D0~D7	D8~D15	Dout MODE	LSB	MSB
H	X	X	X	Hi-Z	Hi-Z	Hi-Z	—	—
L	H	X	X	Hi-Z	Hi-Z			
L	L	H	INPUT FORBIDDEN (D15)	D0~D7	D8~D15	16 bit	A0	A17
L	L	L	L	D0~D7	Hi-Z	8 bit	A-1	A-17
L	L	L	H	D8~D15	Hi-Z			

X: Don't Care

AC CHARACTERISTICS

<TIMING CONDITIONS>

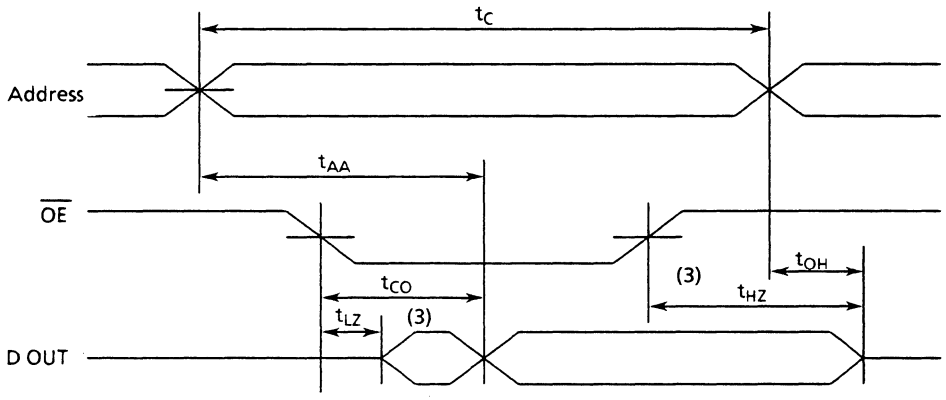
Parameter	Condition
Input Signal Level	V_{IH} = 2.4V, V_{IL} = 0.6V
Input Rising, Falling Time	tr = tf = 5 ns
Timing Measuring Point Voltage	Input Voltage = 1.5V
	Output Voltage = 0.8V & 2.0V
Loading Condition	C_L = 100pF + 1 TTL

<READ CYCLE>

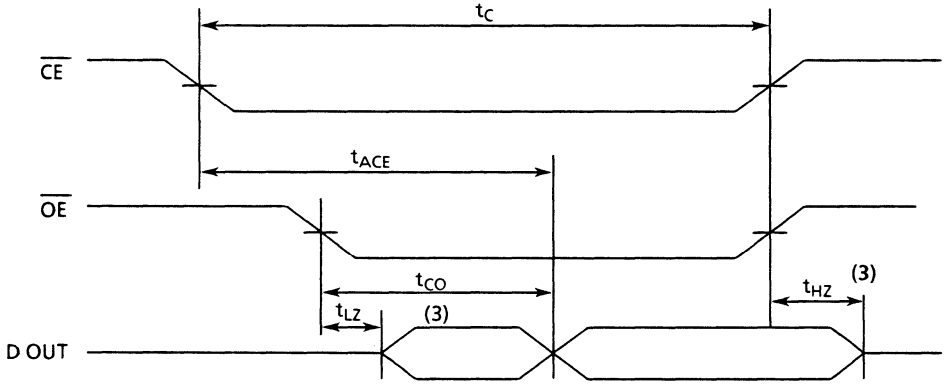
(V_{CC} = 5V ± 10%, V_{SS} = 0V, Ta = 0°C to +70°C)

Parameter	Symbol	Specification Value			Unit	Remarks
		Min.	Typ.	Max.		
Cycle Time	t_C	150	–	–	ns	
Address Access Time	t_{AA}	–	–	150	ns	
Chip Enable Access Time	t_{ACE}	–	–	150	ns	
Output Delay Time	t_{CO}	–	–	60	ns	
Output Setting Time	t_{LZ}	10	–	–	ns	
Output Disable Time	t_{HZ}	10	–	50	ns	
Output Retaining Time	t_{OH}	10	–	–	ns	

- READ CYCLE-1 (NOTE 1)



- READ CYCLE-1 (NOTE 2)



Notes: (1) $\overline{CE}$ is "L" level.

(2) The address is decided at the same time as or ahead of $\overline{CE}$ "L" level.

(3) t_{LZ} is determined by the later $\overline{CE}$ "L" or $\overline{OE}$ "L".
t_{HZ} is determined by the earlier $\overline{CE}$ "H" or $\overline{OE}$ "H".
t_{HZ} shows time until floating therefore it is not determined by the output level.

INPUT/OUTPUT CAPACITANCE

(Ta = 25°C , f = 1 MHz)

Parameter	Symbol	Specification Value		Unit	Remarks
		Min.	Max.		
Input Capacitance	C_I	–	8	pF	V_I = 0V
Output Capacitance	C_O	–	8	pF	V_O = 0V

MOS EPROMS OTPS

7 MOS EPROMS/OTPS

MSM2764A	8,192-Word x 8-Bits EPROM (NMOS)	475
MSM27128A	16,384-Word x 8-Bits EPROM (NMOS)	483
MSM27256	32,768-Word x 8-Bits EPROM (NMOS)	491
MSM27512	65,536-Word x 8-Bits EPROM (NMOS)	499
MSM271000	131,072-Word x 8-Bits EPROM (NMOS)	506
MSM271024	65,536-Word x 16-Bits EPROM (NMOS)	513
MSM27C256	32,768-Word x 8-Bits EPROM (CMOS)	520
MSM27C256H	32,768-Word x 8-Bits EPROM (CMOS)	528
MSM27C1024	65,536-Word x 16-Bits EPROM (CMOS)	536
MSM27C2000	262,144-Word x 8-Bits EPROM (CMOS)	543
MSM27C2048	131,072-Word x 16-Bits EPROM (CMOS)	550
MSM2764AZB	8,192-Word x 8-Bits OTP ROM (NMOS)	557
MSM27128AZB	16,384-Word x 8-Bits OTP ROM (NMOS)	564
MSM27256ZB	32,768-Word x 8-Bits OTP ROM (NMOS)	571
MSM27512ZB	65,536-Word x 8-Bits OTP ROM (NMOS)	578
MSM271000ZB	131,072-Word x 8-Bits OTP ROM (NMOS)	585
MSM271024ZB	65,536-Word x 16-Bits OTP ROM (CMOS)	591
MSM27C256ZB	32,768-Word x 8-Bits OTP ROM (CMOS)	598
MSM27C256HZB	32,768-Word x 8-Bits OTP ROM (CMOS)	605

MSM2764A

8192 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

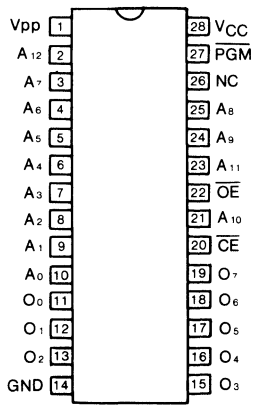
The MSM2764A is a 8192 words x 8 bit ultraviolet erasable and electrically programmable read-only memory. The MSM2764A is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.

FEATURES

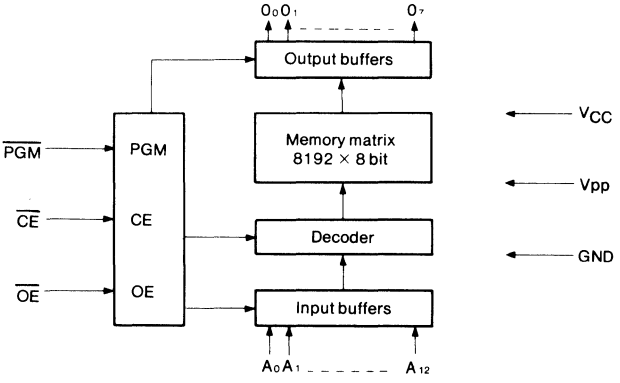
- +5V single power supply
- 8192 words × 8 bit configuration
- Access time:
  - MAX 120 ns (MSM2764A - 12)
  - MAX 150 ns (MSM2764A - 15)
  - MAX 200 ns (MSM2764A - 20)
  - MAX 250 ns (MSM2764A - 25)
- Power consumption:
  - MAX525 mW (during operation)
  - MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (three state output)

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

7

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	− 0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

7

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V± 5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.0	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

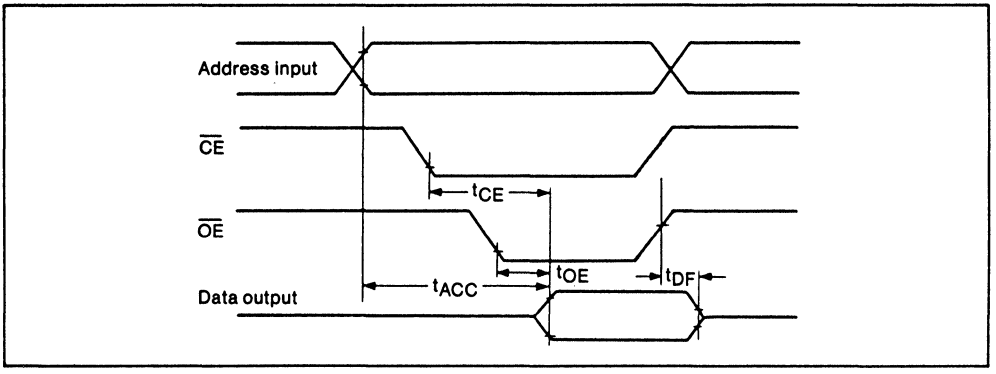
Parameter	Symbol	Conditions	2764A-12		2764A-15		2764A-20		2764A-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	120	–	150	–	200	–	250	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	120	–	150	–	200	–	250	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	50	–	60	–	70	–	100	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	40	0	50	0	55	0	60	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

7

TIME CHART


Address input
$\overline{CE}$
$\overline{OE}$
Data output
t_{CE}
t_{OE}
t_{DF}
t_{ACC}

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V ±0.5V, Ta = 25°C±5°C)

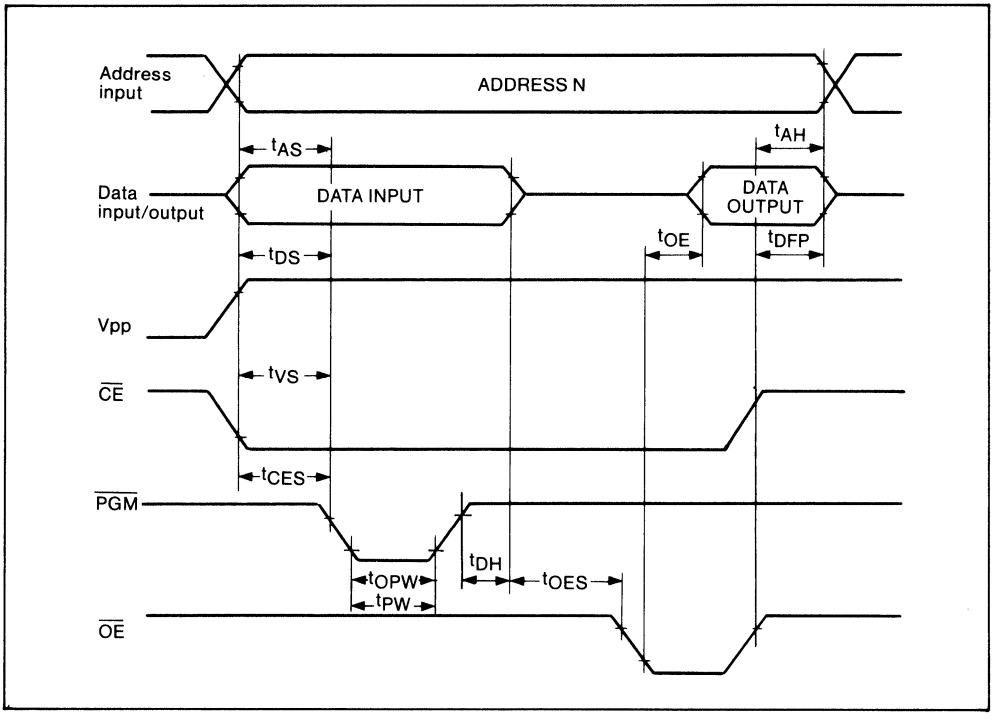
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5 °C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	Vcc=6V±0.25V	0.95	1.0	1.05	ms
$\overline{PGM}$ Program Pulse Width	t_{PW}	Vcc=6.25V±0.25V	95	100	105	μs
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	Vcc=6V±0.25V	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART

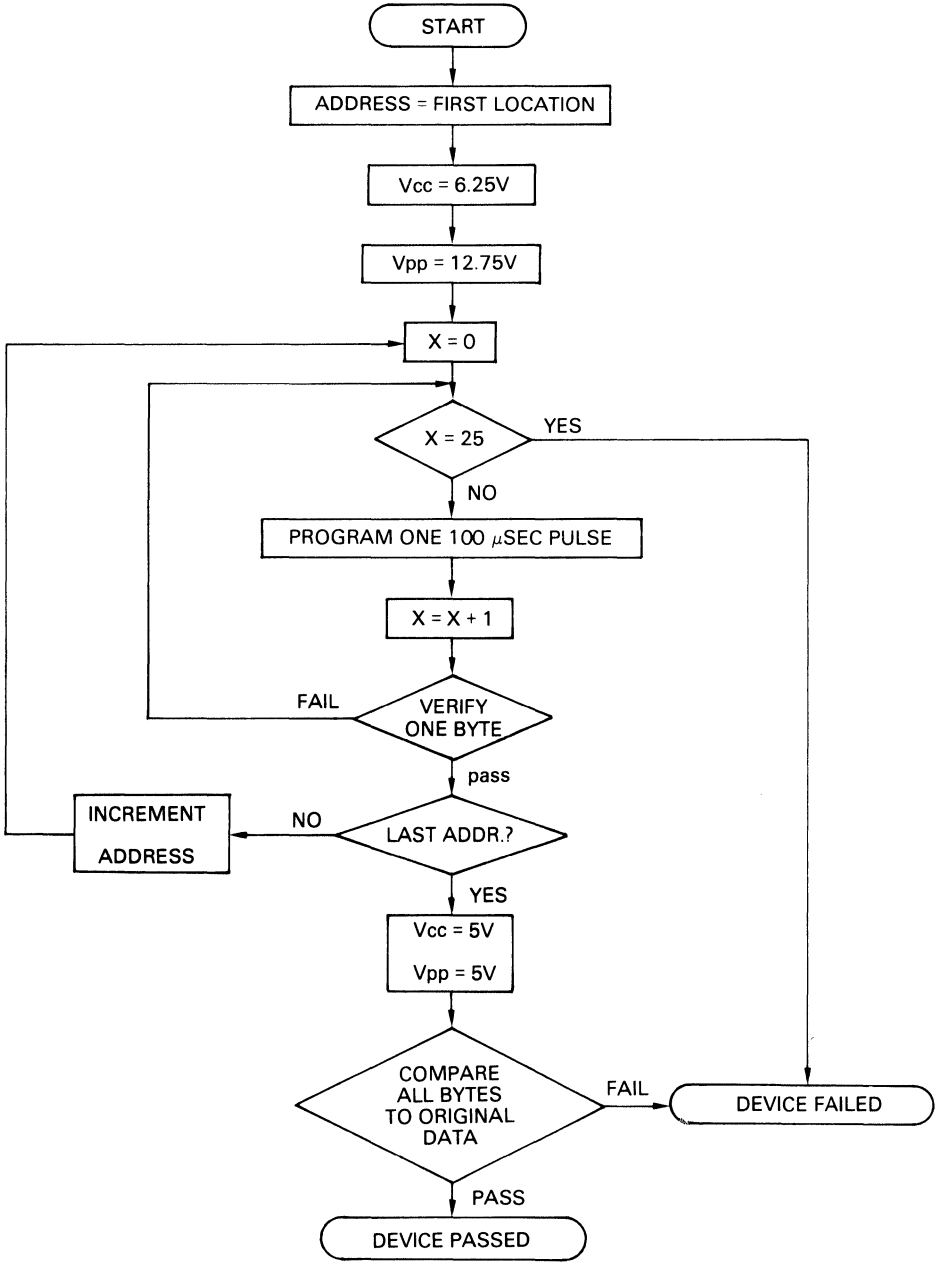


7

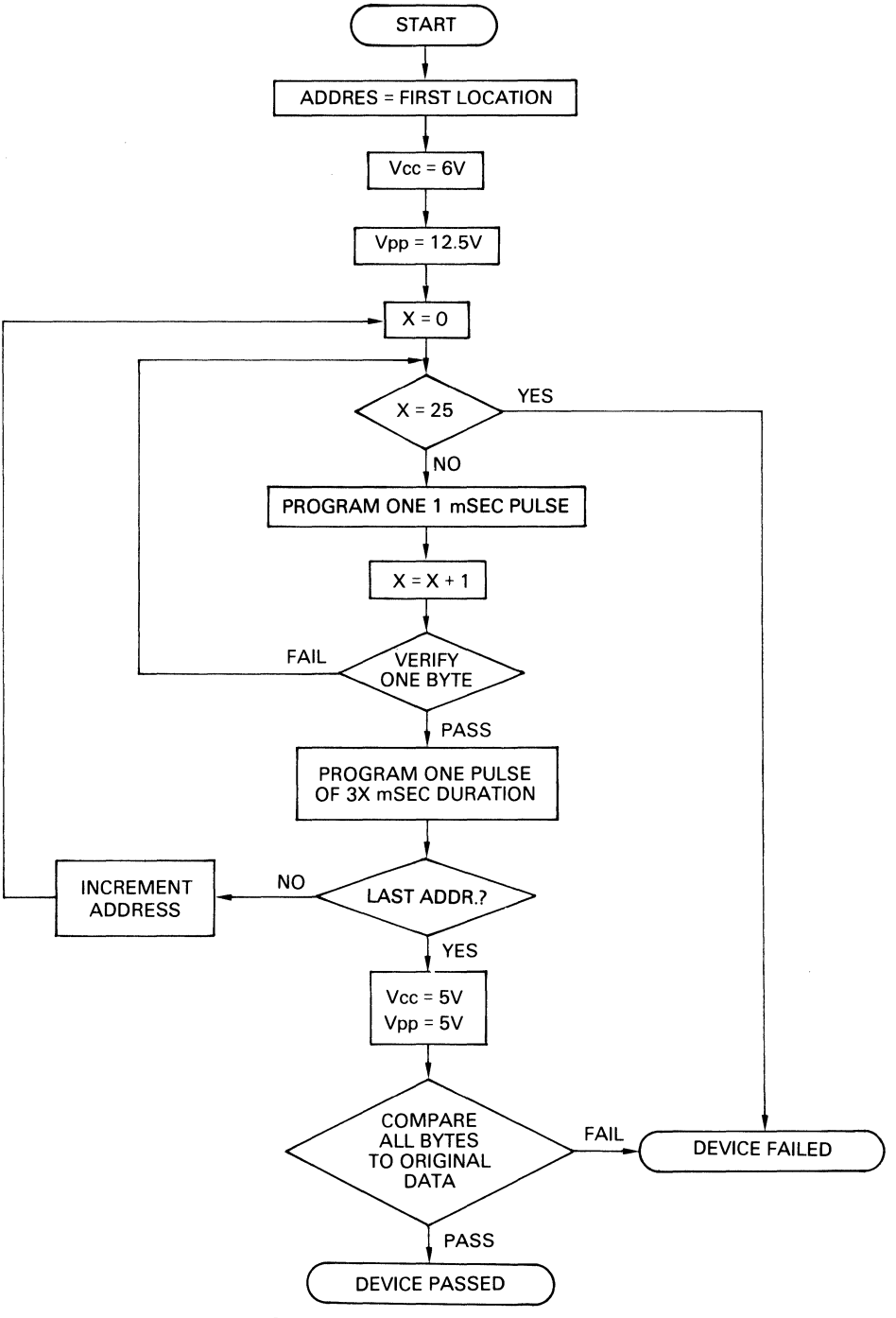
CAPACITANCE

(Ta = 25°C, f = 1 MHz, Vcc=5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF



Programming Flowchart Example (I)



Programming Flowchart Example (II)

MSM27128A

16384 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

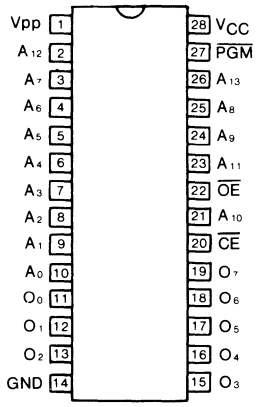
The MSM27128A is a 16384 words x 8 bit ultraviolet erasable and electrically programmable read-only memory. The MSM27128A is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.

FEATURES

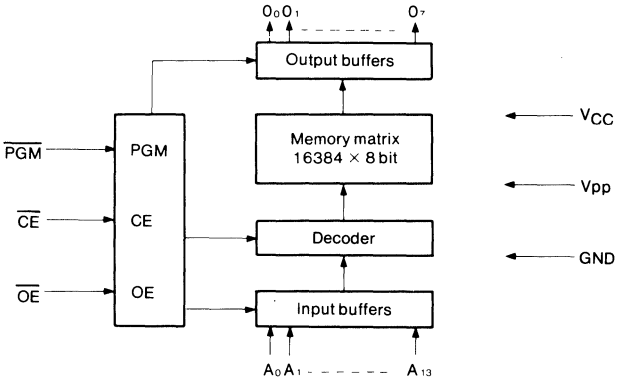
- +5V single power supply
- 16384 words × 8 bit configuration
- Access time:
  - MAX 120 ns (MSM27128A-12)
  - MAX 150 ns (MSM27128A-15)
  - MAX 200 ns (MSM27128A-20)
  - MAX 250 ns (MSM27128A-25)
- Power consumption:
  - MAX525 mW (during operation)
  - MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (three state output)

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

7

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP_1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

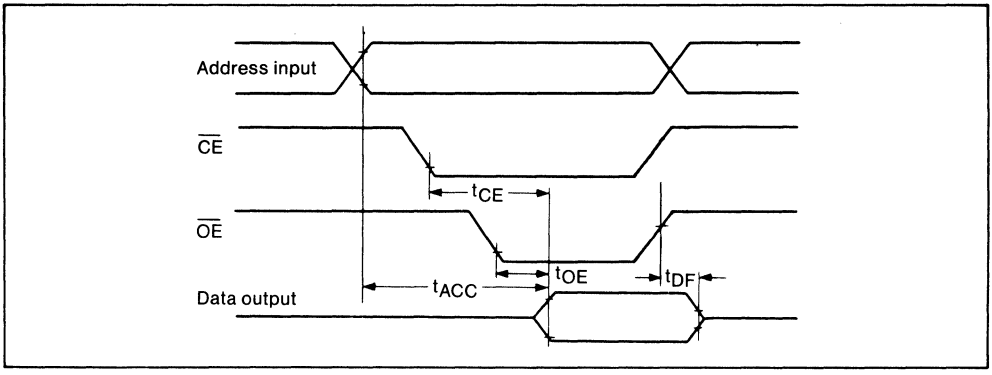
(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	27128A-12		27128A-15		27128A-20		27128A-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	120	–	150	–	200	–	250	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	120	–	150	–	200	–	250	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	50	–	60	–	70	–	100	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	40	0	50	0	55	0	60	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V ±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

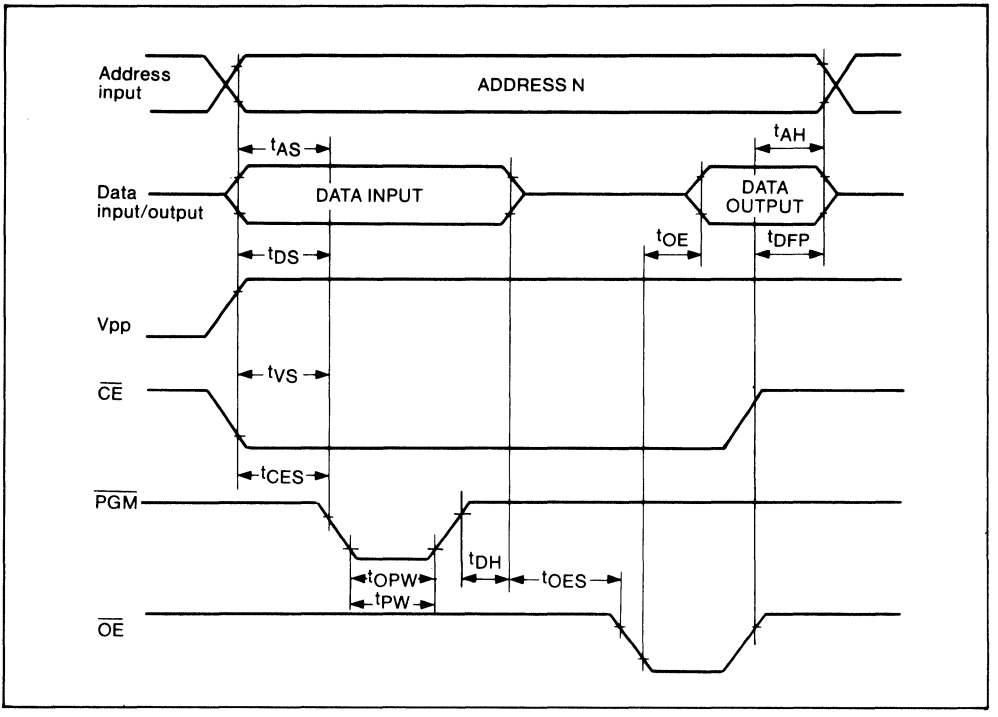
AC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	Vcc = 6V ±0.25V	0.95	1.0	1.05	ms
$\overline{PGM}$ Program Pulse Width	t_{PW}	Vcc =6.25V ±0.25V	95	100	105	μs
$\overline{PGM}$ Overprogram Pluse Width	t_{OPW}	Vcc = 6V ±0.25V	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

7

TIME CHART

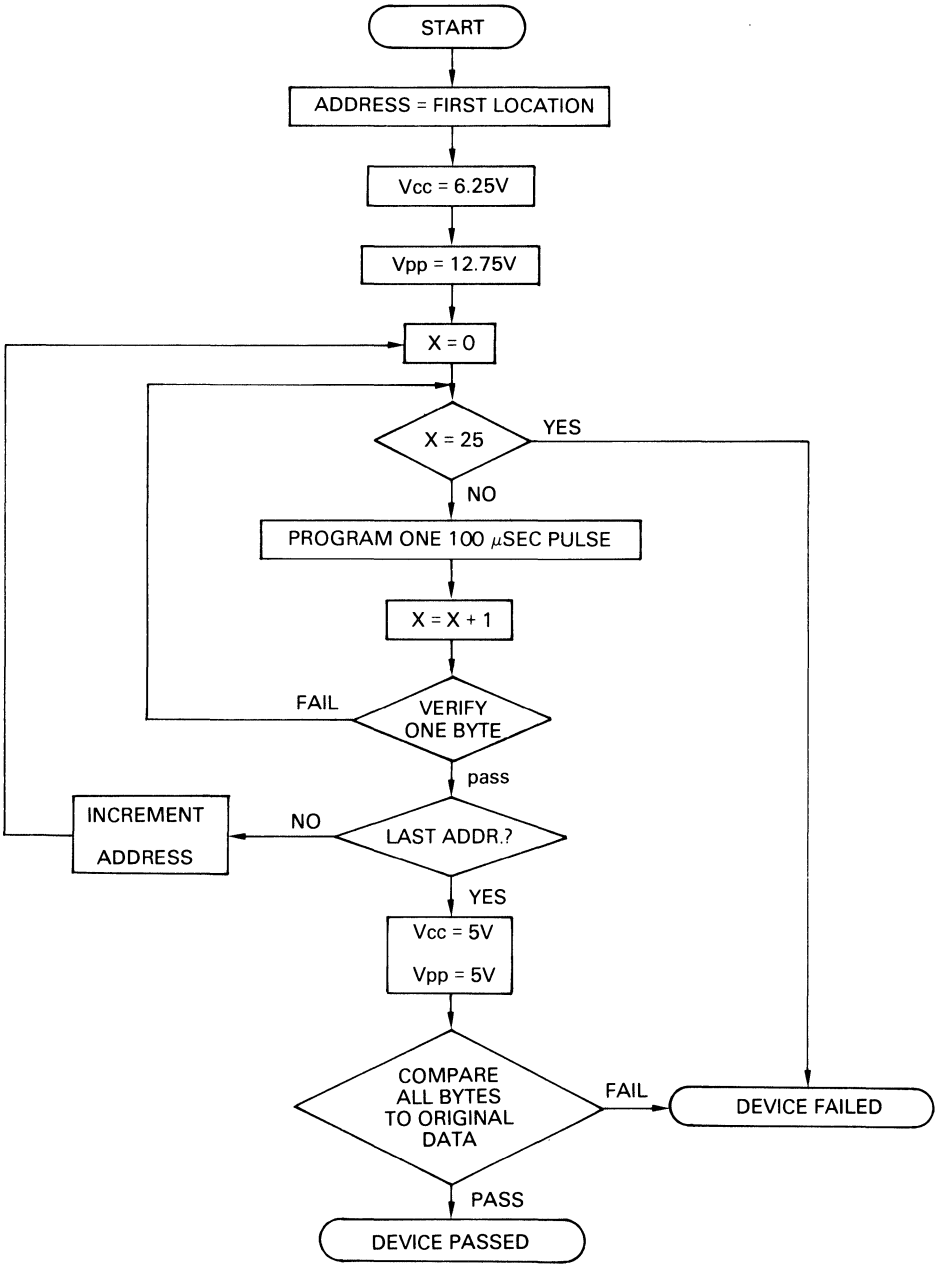


7

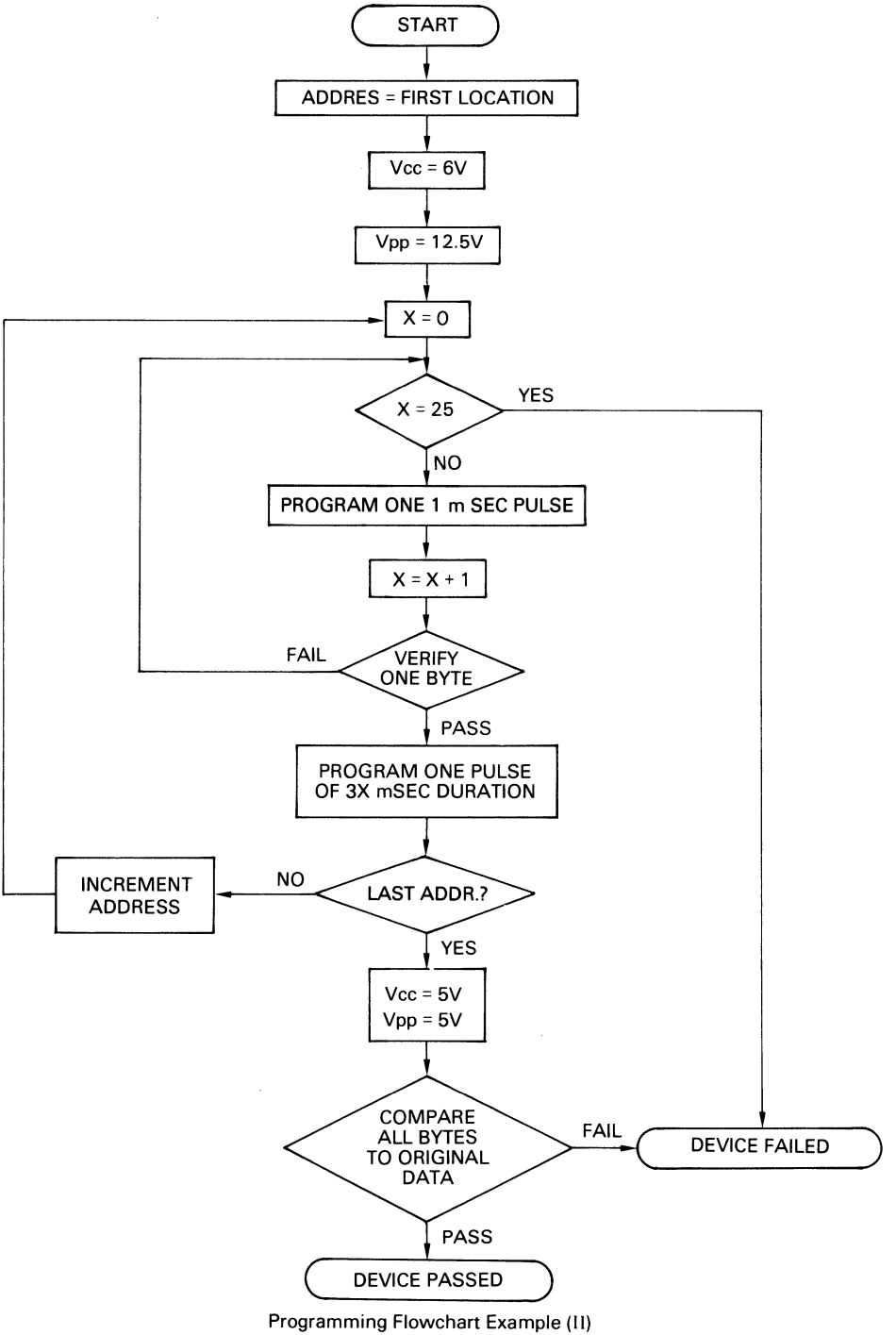
CAPACITANCE

(Ta = 25°C, f = 1 MHz, V_{CC} = 5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF



Programming Flowchart Example (I)



Programming Flowchart Example (II)

MSM27256

32768 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

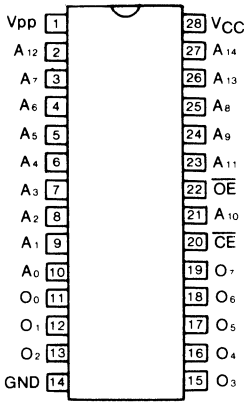
The MSM27256 is a 32768 words x 8 bit ultraviolet erasable and electrically programmable read-only memory. The MSM27256 is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.

FEATURES

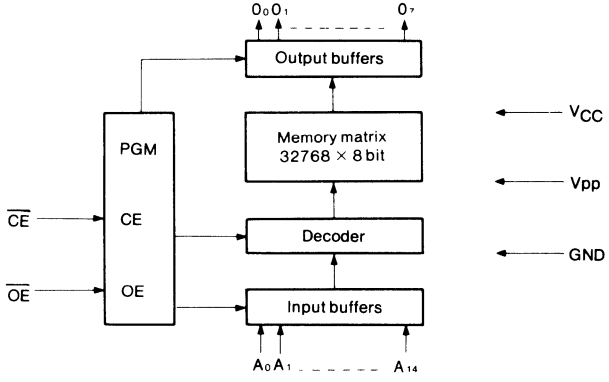
- +5V single power supply
- 32768 words × 8 bit configuration
- Access time:
  - MAX 120 ns (MSM27256-12)
  - MAX 150 ns (MSM27256-15)
  - MAX 200 ns (MSM27256-20)
  - MAX 250 ns (MSM27256-25)
- Power consumption:
  - MAX525 mW (during operation)
  - MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (three state output)

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

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FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	+12.5V	+6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	V_{IH}	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}	−0.6V ~ 13.5V
	V_{OUT}	−0.6V ~ 7V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

7

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.0	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

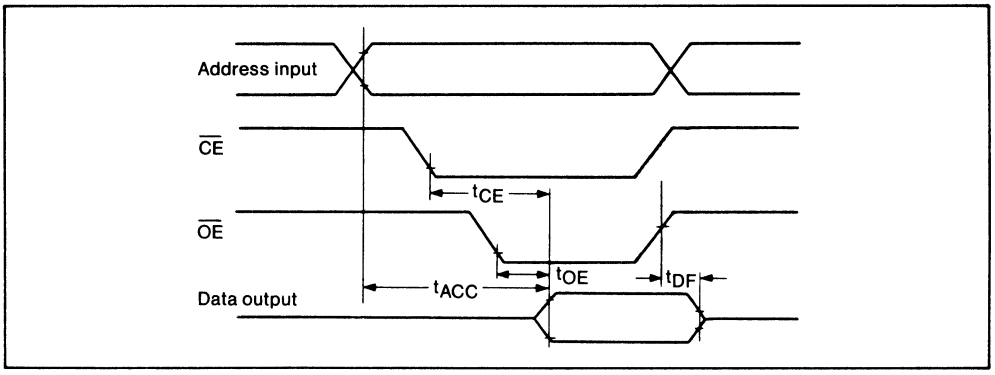
Parameter	Symbol	Conditions	27256-12		27256-15		27256-20		27256-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	120	–	150	–	200	–	250	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	120	–	150	–	200	–	250	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	50	–	60	–	70	–	100	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	40	0	50	0	55	0	60	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

7

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

< PROGRAMMING OPERATION >

DC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

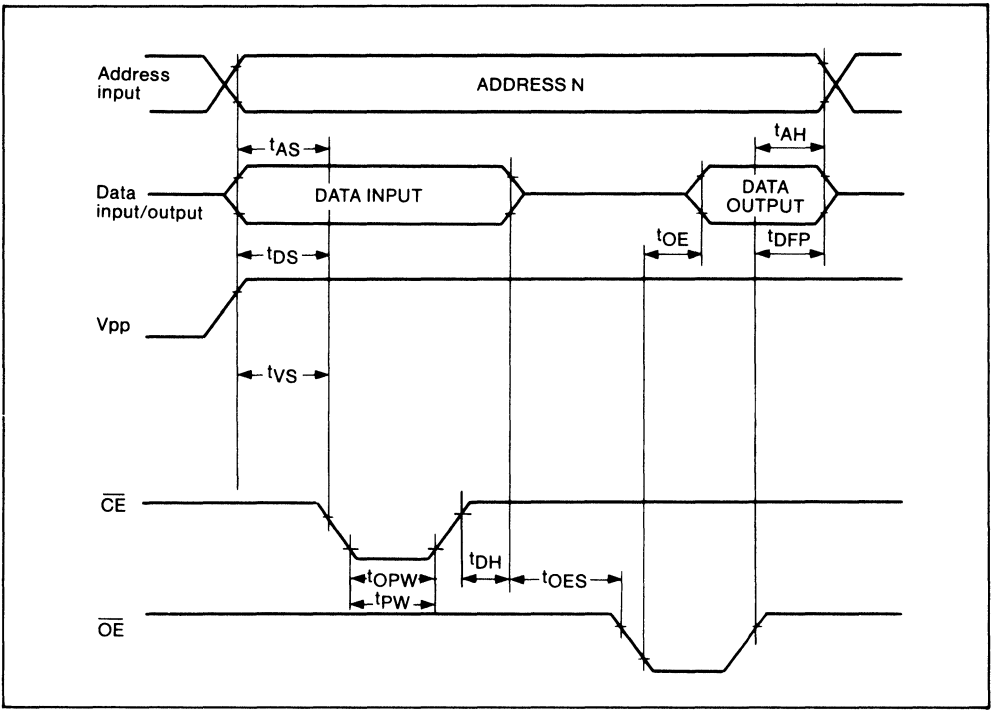
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	Vcc=6V±0.25V	0.95	1.0	1.05	ms
$\overline{CE}$ Program Pulse Width	t_{PW}	Vcc=6.25V±0.25V	95	100	105	μs
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	Vcc=6V±0.25V	2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART

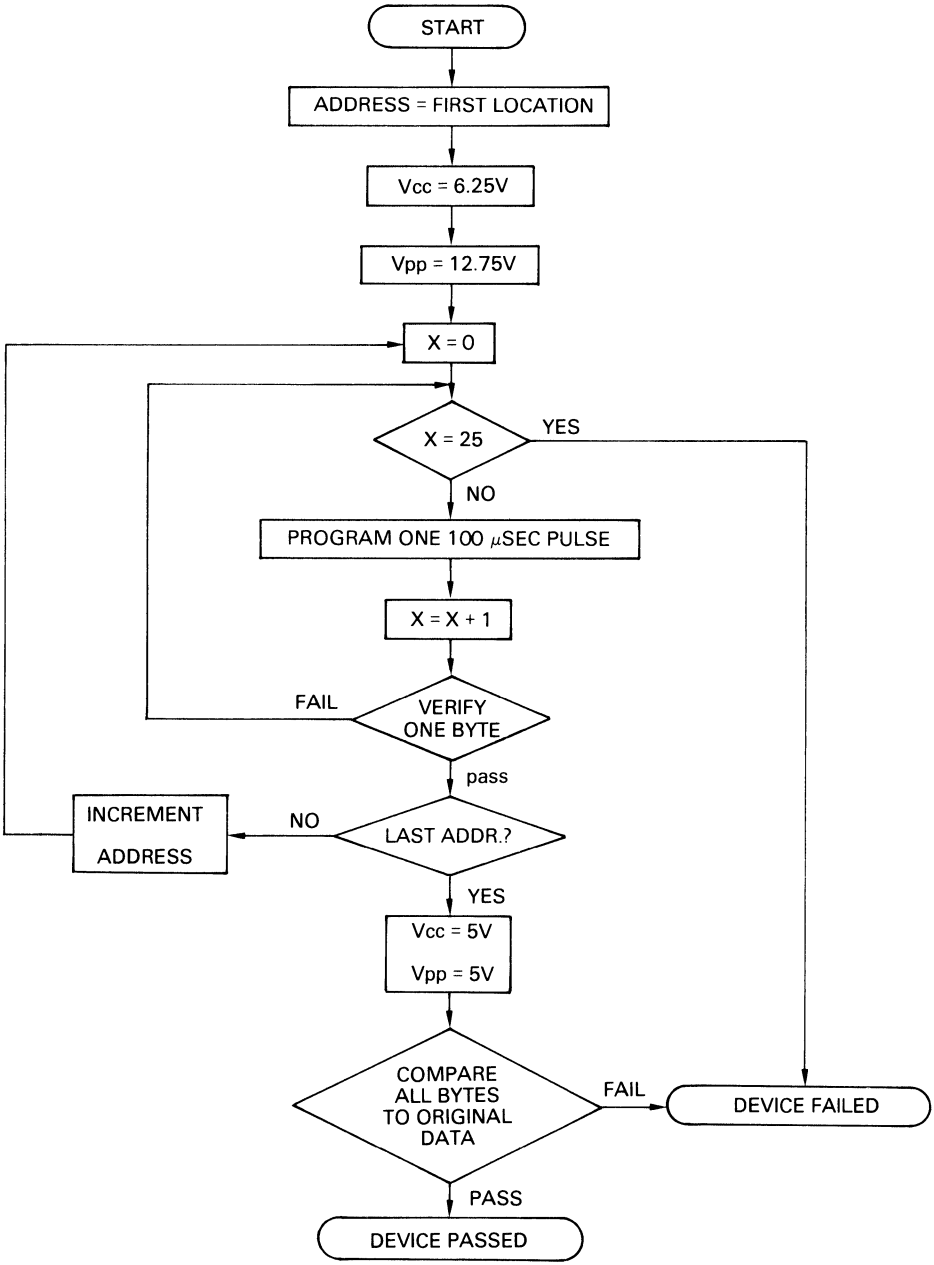


7

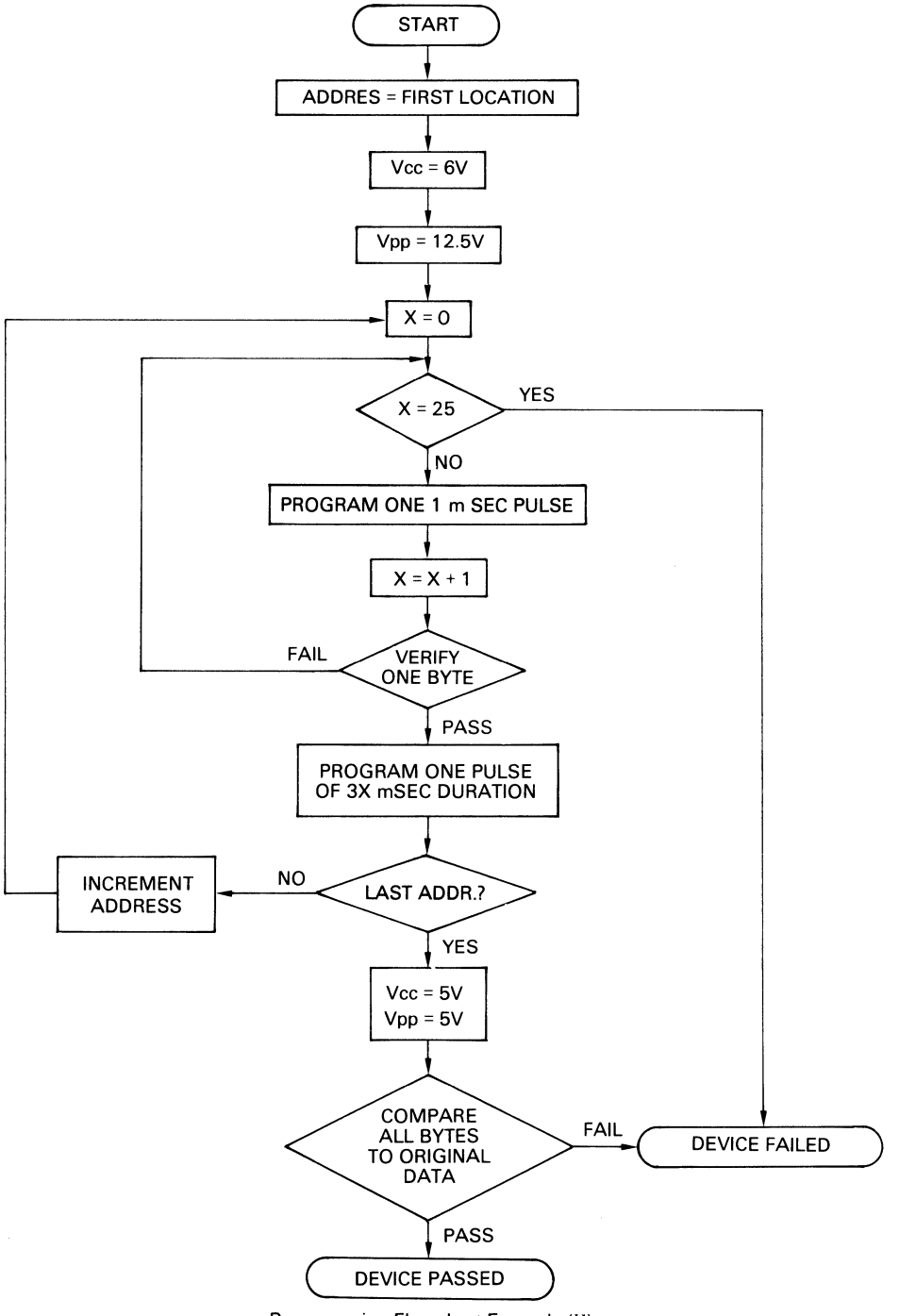
CAPACITANCE

(Ta = 25°C, f = 1 MHz, Vcc = 5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF



Programming Flowchart Example (I)



Programming Flowchart Example (II)

MSM27512

65536 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

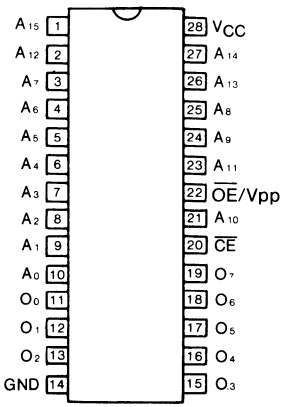
The MSM27512 is a 65536 words x 8 bit ultraviolet erasable and electrically programmable read-only memory. The MSM27512 is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.

FEATURES

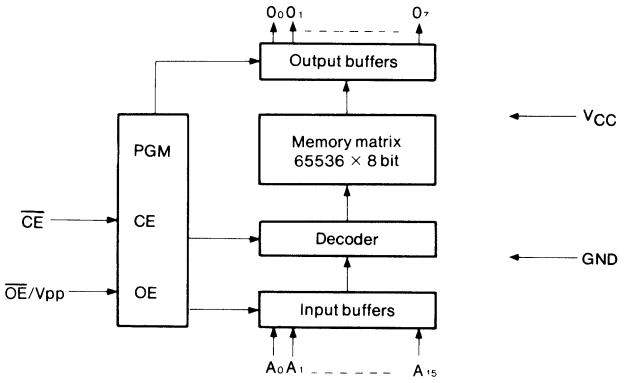
- +5V single power supply
- 65536 words × 8 bit configuration
- Access time:
  - MAX 120 ns (MSM27512-12)
  - MAX 150 ns (MSM27512-15)
  - MAX 200 ns (MSM27512-20)
  - MAX 250 ns (MSM27512-25)
- Power consumption:
  - MAX525 mW (during operation)
  - MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (three state output)

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$/Vpp (22)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	High impedance
Stand-by	V_{IH}	–	+5V	High impedance
Program	V_{IL}	12.5V	+6V	D_{IN}
Program Inhibit	V_{IH}	12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}	−0.6V ~ 13.5V
	V_{OUT}	−0.6V ~ 7V
V_{CC} Supply Voltage	V_{CC}	− 0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

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ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5%	V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

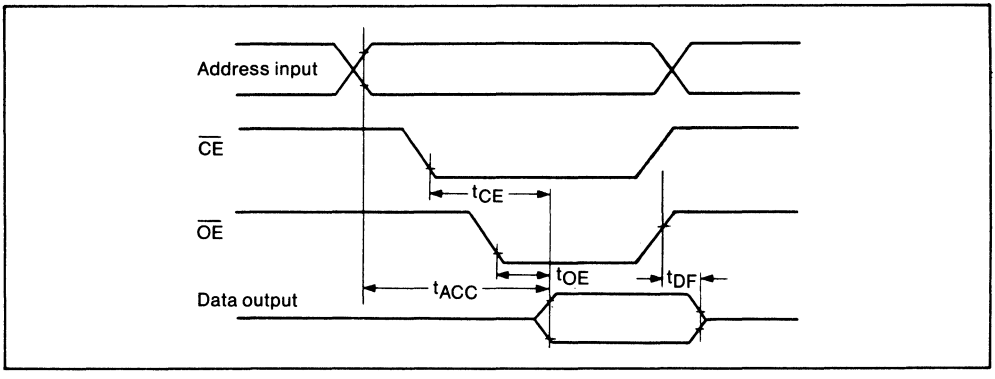
(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	27512-12		27512-15		27512-20		27512-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$=$\overline{OE}$/Vpp=V_{IL}	–	120	–	150	–	200	–	250	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$/Vpp=V_{IL}	–	120	–	150	–	200	–	250	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	50	–	60	–	70	–	100	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	40	0	50	0	55	0	60	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART



< PROGRAMMING OPERATION >

DC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V ± 0.5V, Ta = 25°C ± 5°C)

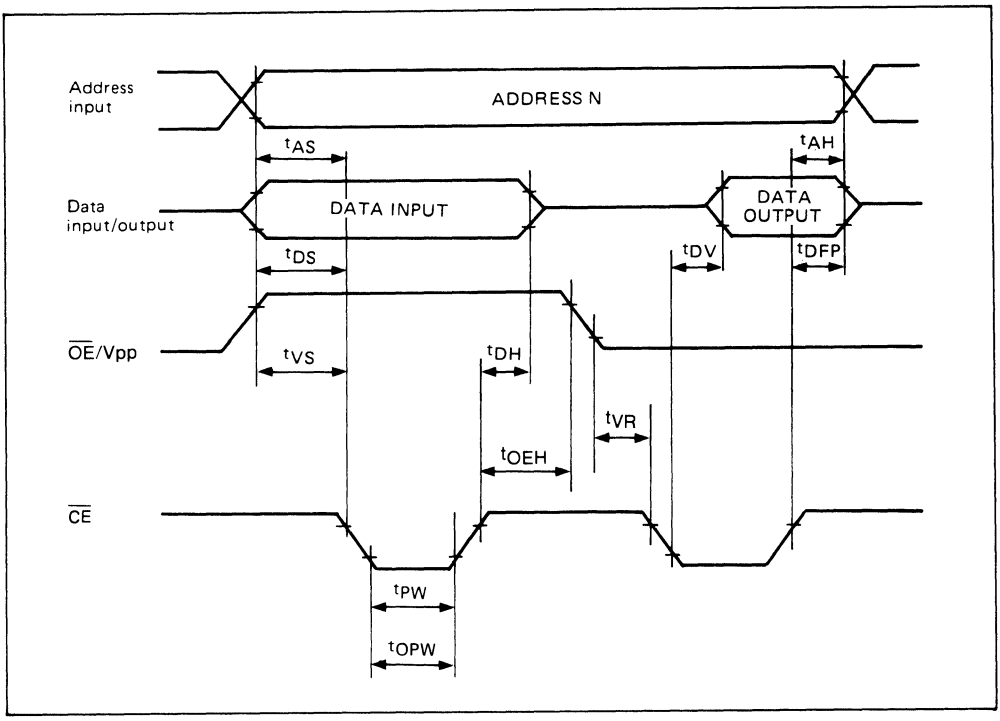
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE}$ = V_{IL}	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V ± 0.5V, Ta = 25°C ± 5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	V_{CC}=6V±0.25V	0.95	1.0	1.05	ms
$\overline{CE}$ Program Pulse Width	t_{PW}	V_{CC}=6.25V±0.25V	95	100	105	μs
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	V_{CC}=6V±0.25V	2.85	–	78.75	ms
$\overline{OE}$/Vpp Hold Time	t_{OEH}	–	2	–	–	μs
Data Valid from $\overline{CE}$	t_{DV}	–	–	–	1	μs
$\overline{OE}$/Vpp Recovery Time	t_{VR}	–	2	–	–	μs

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz, V_{CC} = 5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

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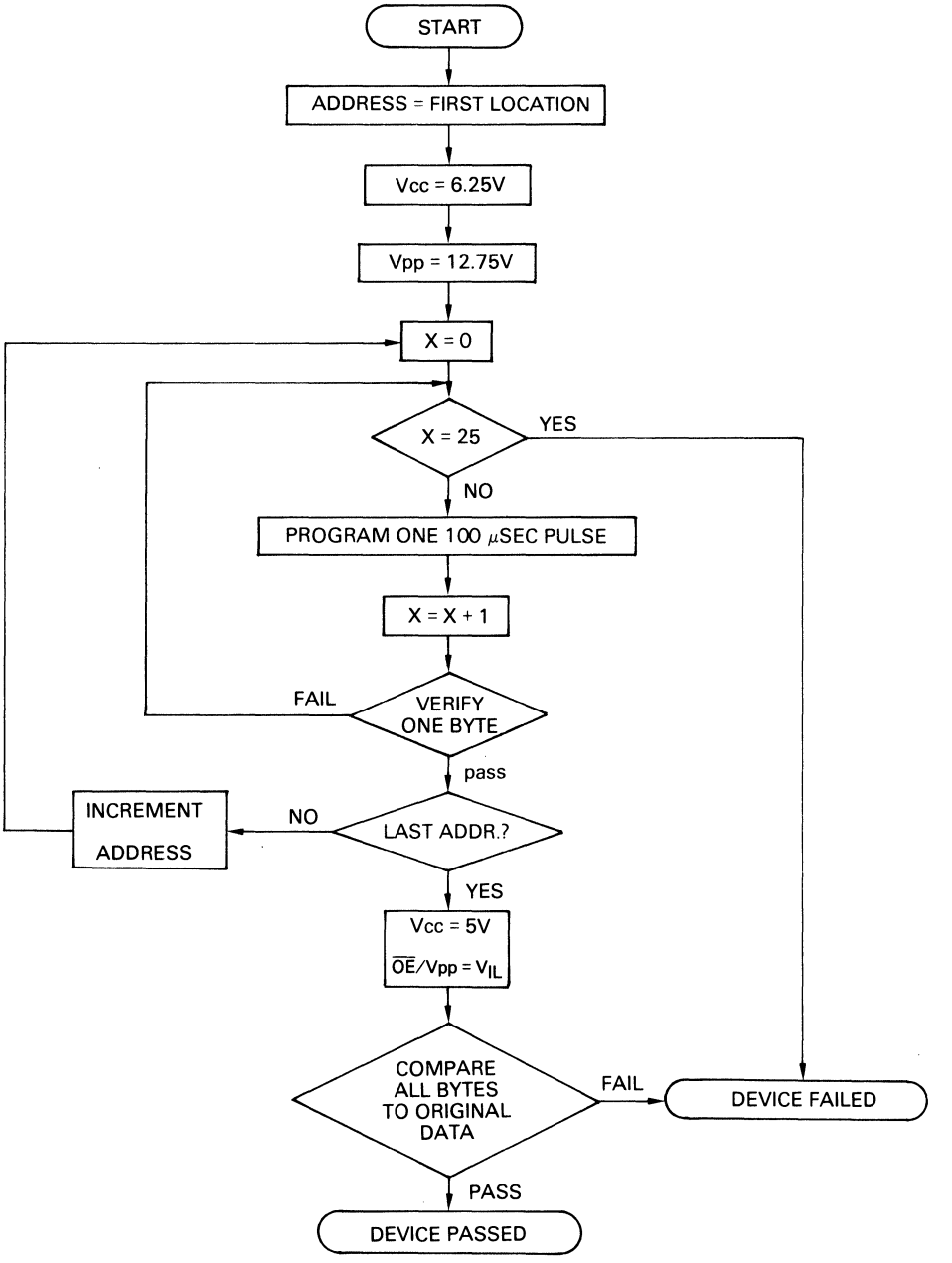
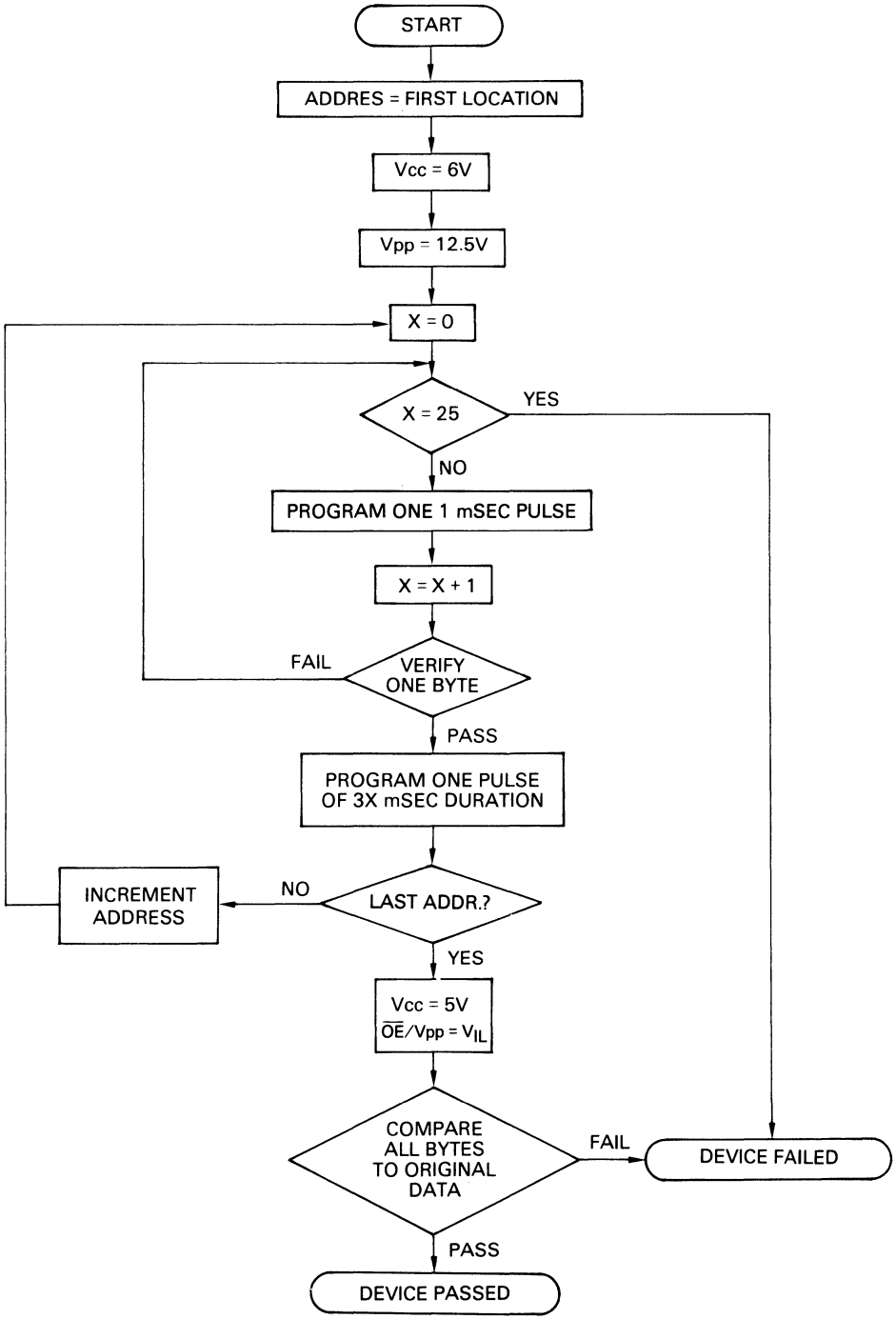


Programming Flowchart Example (I)



Programming Flowchart Example (II)

OKI semiconductor

MSM271000

131072 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

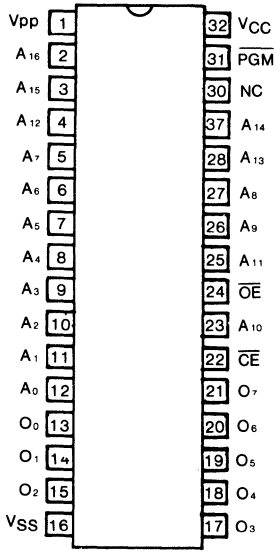
GENERAL DESCRIPTION

The MSM271000 is a 131072 words x 8 bit ultraviolet erasable and electrically programmable read-only memory. The MSM271000 is manufactured by the N channel double silicon gate MOS technology and is contained in the 32 pin package.

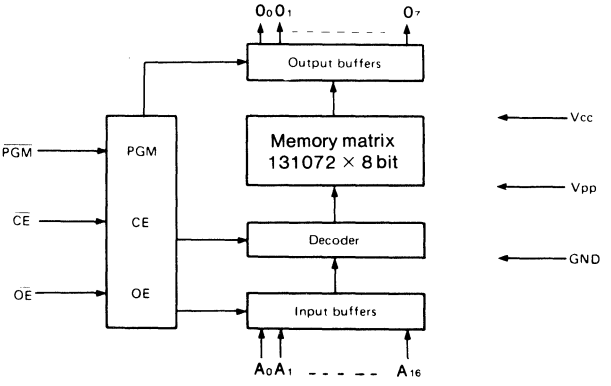
FEATURES

- +5V single power supply
- 131072 words × 8 bit configuration
- Access time:
  MAX120 ns (MSM271000-12)
  MAX150 ns (MSM271000-15)
  MAX200 ns (MSM271000-20)
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (three state output)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	VPP (1)	VCC (32)	Outputs
Read	V_{IL}	V_{IL}	—	—	+5V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	—	—	+5V	High impedance
Stand-by	V_{IH}	—	—	—	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.75V	+6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.75V	+6.25V	D_{OUT}
Program Inhibit	V_{IH}	—	—	+12.75V	+6.25V	High impedance

NOTES:
—; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}	−0.6V ~ 13.5V
	V_{OUT}	−0.6V ~ 7V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V± 5%	V
Vpp Voltage	Vpp	- 0.1	—	Vcc + 1			V
"H" Level Input Voltage	V_{IH}	2.0	—	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	—	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP_1}	Vpp = V_{CC}	–	–	10	μA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

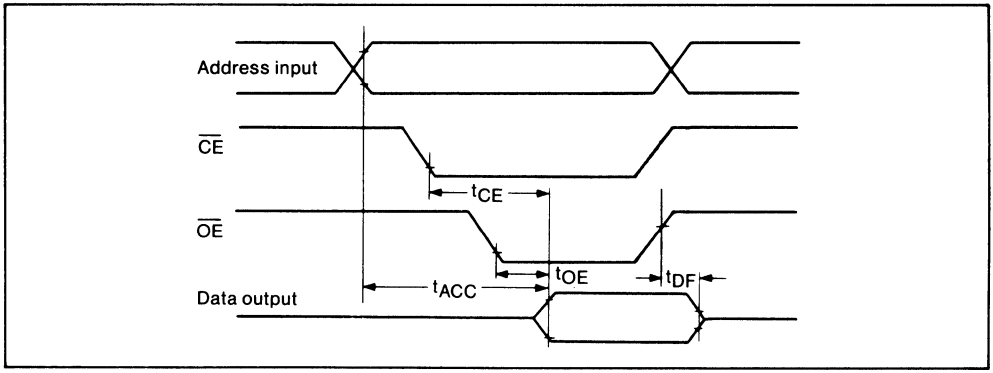
(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	271000-12		271000-15		271000-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	120	–	150	–	200	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	120	–	150	–	200	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	50	–	60	–	70	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	40	0	50	0	55	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V±0.25V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V±0.25V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
Program Pulse Width	t_{PW}	—	95	100	105	μs
$\overline{CE}$ Set-up Time	t_{CES}	—	2	—	–	μs
Data Valid from $\overline{OE}$	t_{OE}	—		–	150	ns

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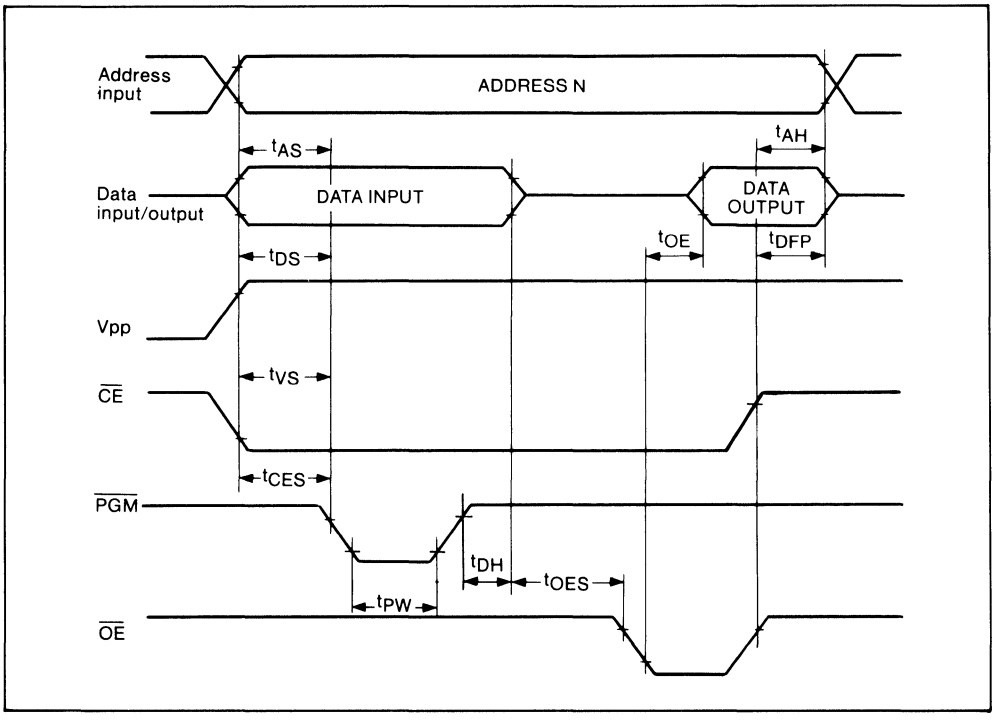
TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz, V_{CC} = 5V)

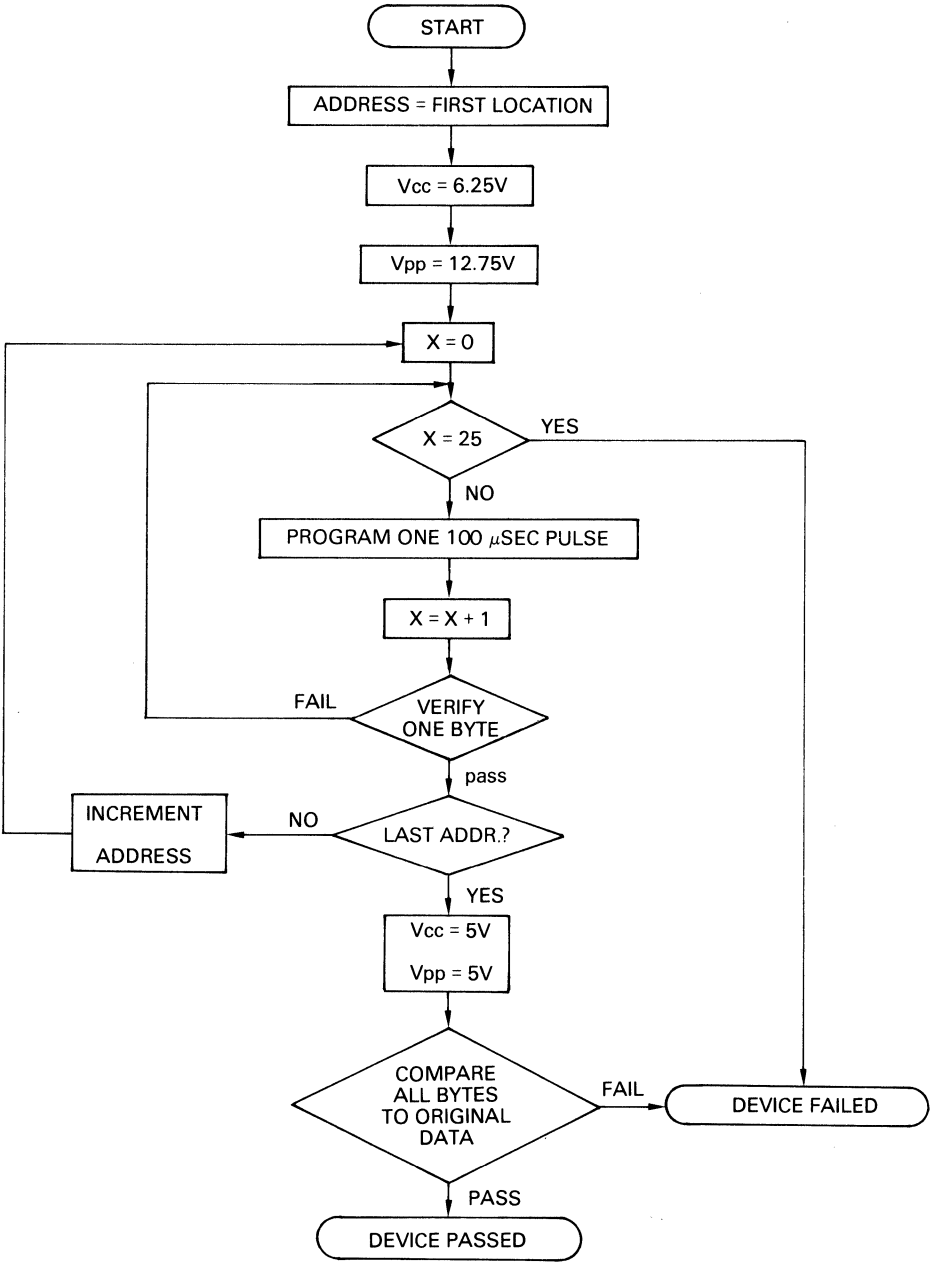
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	–	15	pF

MSM271000 IDENTIFIER BYTES

Pins / Code	A_0 (12)	D_7 (21)	D_6 (20)	D_5 (19)	D_4 (18)	D_3 (17)	D_2 (15)	D_1 (14)	D_0 (13)	Hex Data
Manufacter Code	V_{IL}	1	0	1	0	1	1	1	0	AE
Device Code	V_{IH}	1	0	0	0	0	1	0	1	85

Notes: 1. A_9 = 12.0 ± 0.5V

2. $A_1 \sim A_8$, $A_{10} \sim A_{16}$, $\overline{CE}$, $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH} OR V_{IL}, Vpp = V_{IH} OR V_{IL}



Programming Flowchart Example (I)

Preliminary

OKI semiconductor

MSM271024

65536 × 16 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

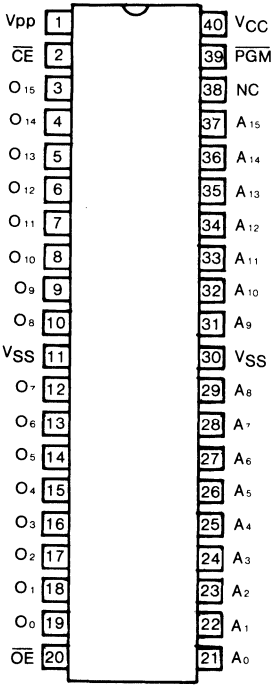
GENERAL DESCRIPTION

The MSM271024 is a 65536 words x 16 bit ultraviolet erasable and electrically programmable read-only memory. The MSM271024 is manufactured by the N channel double silicon gate MOS technology and is contained in the 40 pin package.

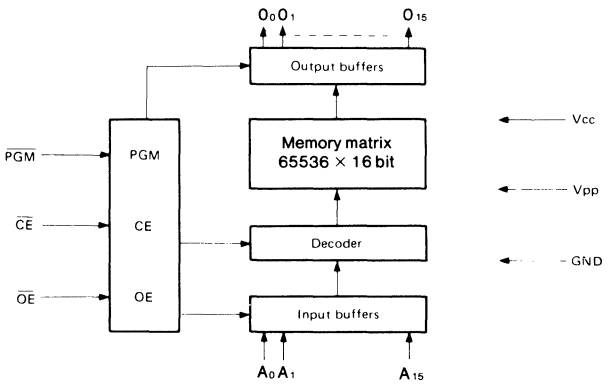
FEATURES

- +5V single power supply
- 65536 words × 16 bit configuration
- Access time:
  MAX120 ns (MSM271024-12)
  MAX150 ns (MSM271024-15)
  MAX200 ns (MSM271024-20)
- Power consumption:
  MAX630 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (three state output)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

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FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (2)	$\overline{OE}$ (20)	$\overline{PGM}$ (39)	VPP (1)	VCC (40)	Outputs
Read	V_{IL}	V_{IL}	—	—	+5V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	—	—	+5V	High impedance
Stand-by	V_{IH}	—	—	—	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.75V	+6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.75V	+6.25V	D_{OUT}
Program Inhibit	V_{IH}	—	—	+12.75V	+6.25V	High impedance

NOTES:
—; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}	−0.6V ~ 13.5V
	V_{OUT}	−0.6V ~ 7V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

7

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±0.25V	V
Vpp Voltage	Vpp	−0.1V	—	V_{CC} +1			V
"H" Level Input Voltage	V_{IH}	2.00	—	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	—	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	120	mA
Program Power Current	I_{PP_1}	V_{PP} = V_{CC}	–	–	10	μA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

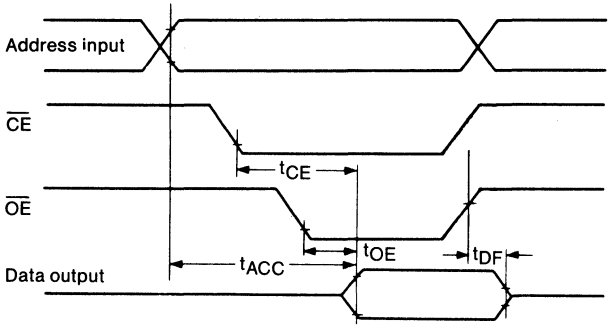
(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	271024-12		271024-15		271024-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL},	–	120	–	150	–	200	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL},	–	120	–	150	–	200	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL},	–	50	–	60	–	70	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL},	0	40	0	50	0	55	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
$\overline{OE}$
Data output
t_{CE}
t_{OE}
t_{DF}
t_{ACC}

7

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V±0.25V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	120	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

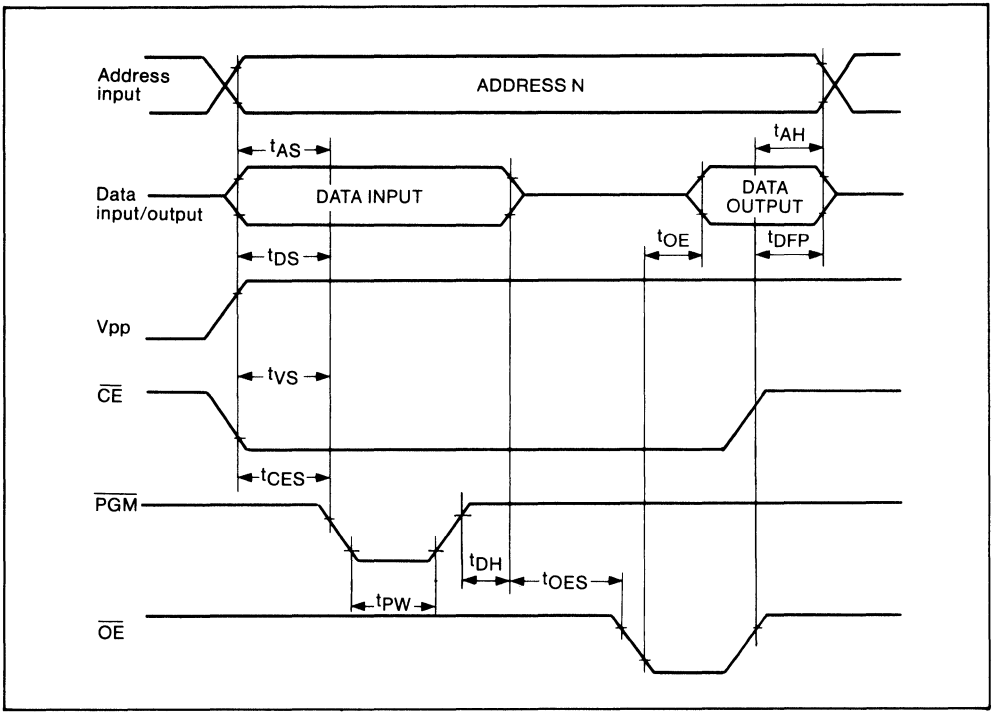
AC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V±0.25V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Program Pulse Width	t_{PW}	—	95	100	105	μs
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

7

TIME CHART



7

CAPACITANCE

(Ta = 25°C, f = 1 MHz, V_{CC} = 5V)

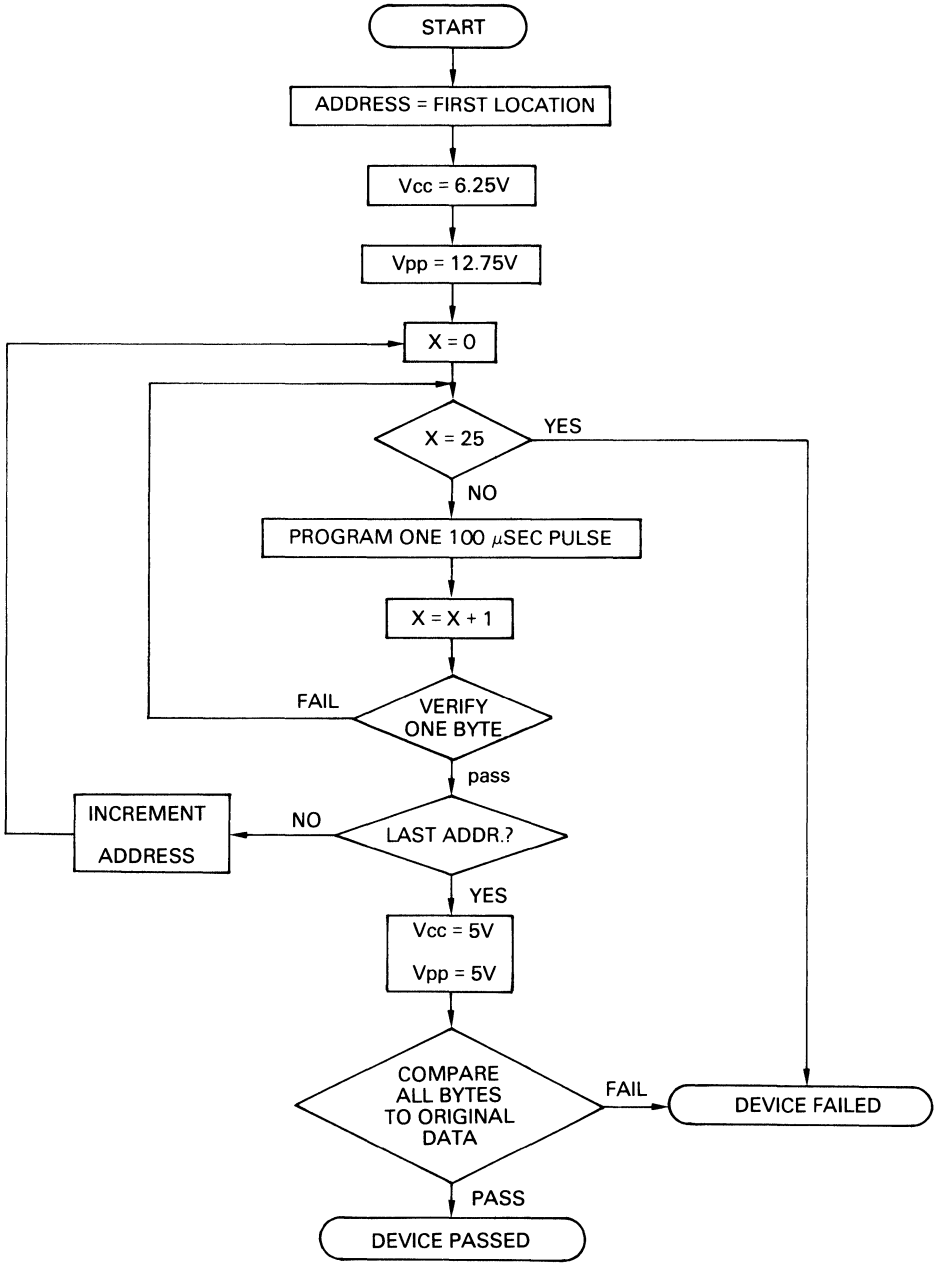
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	–	15	pF

MSM271024 **IDENTIFIER BYTES**

Pins / Code	A_0 (21)	$D_{15} \sim D_8$ (3) ~ (10)	D_7 (12)	D_6 (13)	D_5 (14)	D_4 (15)	D_3 (16)	D_2 (17)	D_1 (18)	D_0 (19)	Hex Data
Manufacter Code	V_{IL}	0 ~ 0	1	0	1	0	1	1	1	0	00AE
Device Code	V_{IH}	0 ~ 0	1	0	0	0	0	1	1	0	0086

Notes: 1. $A_9 = 12.0 \pm 0.5V$

2. $A_1 \sim A_8$, $A_{10} \sim A_{15}$, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$ OR V_{IL}, Vpp = V_{IH} OR V_{IL}



Programming Flowchart Example (I)

MSM27C256

32768 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

The MSM27C256 is a 32768 words x 8 bit ultraviolet erasable and electrically programmable read-only memory. The MSM27C256 is manufactured by the CMOS double silicon gate technology and is contained in the 28 pin package.

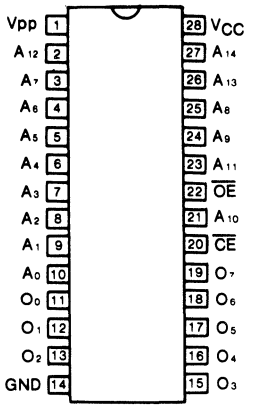
FEATURES

- +5V single power supply
- 32768 words × 8 bit configuration
- Access time:
  - MAX 100ns (MSM27C256-10)
  - MAX 120 ns (MSM27C256-12)
  - MAX 150 ns (MSM27C256-15)
  - MAX 200 ns (MSM27C256-20)
  - MAX 250 ns (MSM27C256-25)
- Power consumption:
  - MAX165 mW (during operation)
  - MAX0.55 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (three state output)

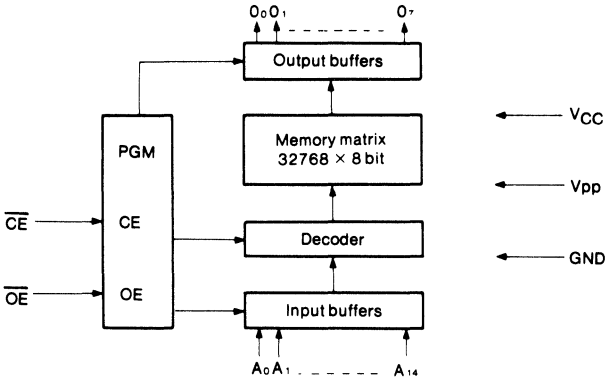
7

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	+12.5V	+6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	V_{IH}	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input Voltage	V_{IN}	−0.6V ~ 13V
All Output Voltage	V_{OUT}	−0.6V ~ V_{CC} +0.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

7

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.5	5.0	5.5	0°C ~ 70°C	V_{CC}=5V ±10% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.5	5.0	5.5			V
"H" Level Input Voltage	V_{IH}	2.0	–	V_{CC} +0.5			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	1	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5V	–	–	1	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{CC}	–	–	100	μA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	30	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	100	μA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC} +0.5	V
Input Voltage "L" Level	V_{IL}	–	-0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

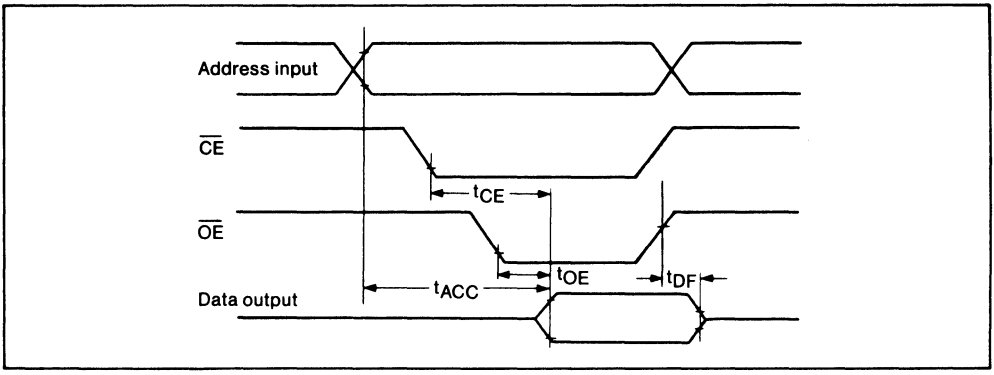
(V_{CC} = 5V±10%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	27C256-10		27C256-12		27C256-15		27C256-20		27C256-25		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	100	–	120	–	150	–	200	–	250	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	100	–	120	–	150	–	200	–	250	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	50	–	50	–	60	–	70	–	100	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	40	0	40	0	50	0	55	0	60	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
Data output
t_{ACC}

< PROGRAMMING OPERATION >

DC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+0.5	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

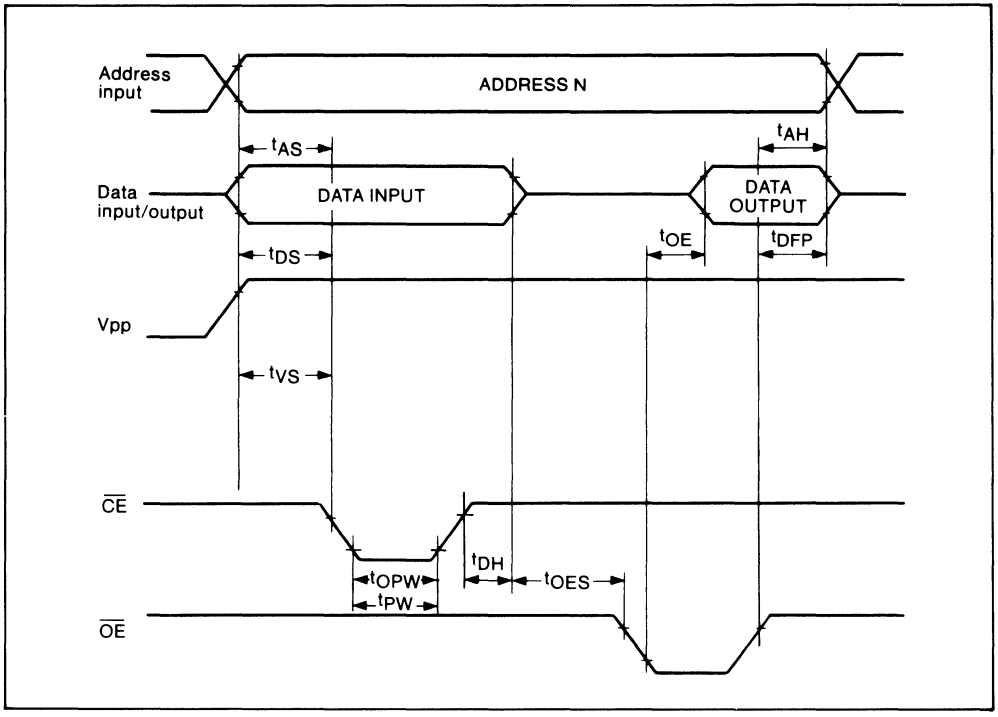
AC CHARACTERISTICS

(V_{CC} = 5.75V ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	Vcc=6V±0.25V	0.95	1.0	1.05	ms
$\overline{CE}$ Program Pulse Width	t_{PW}	Vcc=6.25V±0.25V	95	100	105	μs
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	Vcc=6V±0.25V	2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

7

TIME CHART

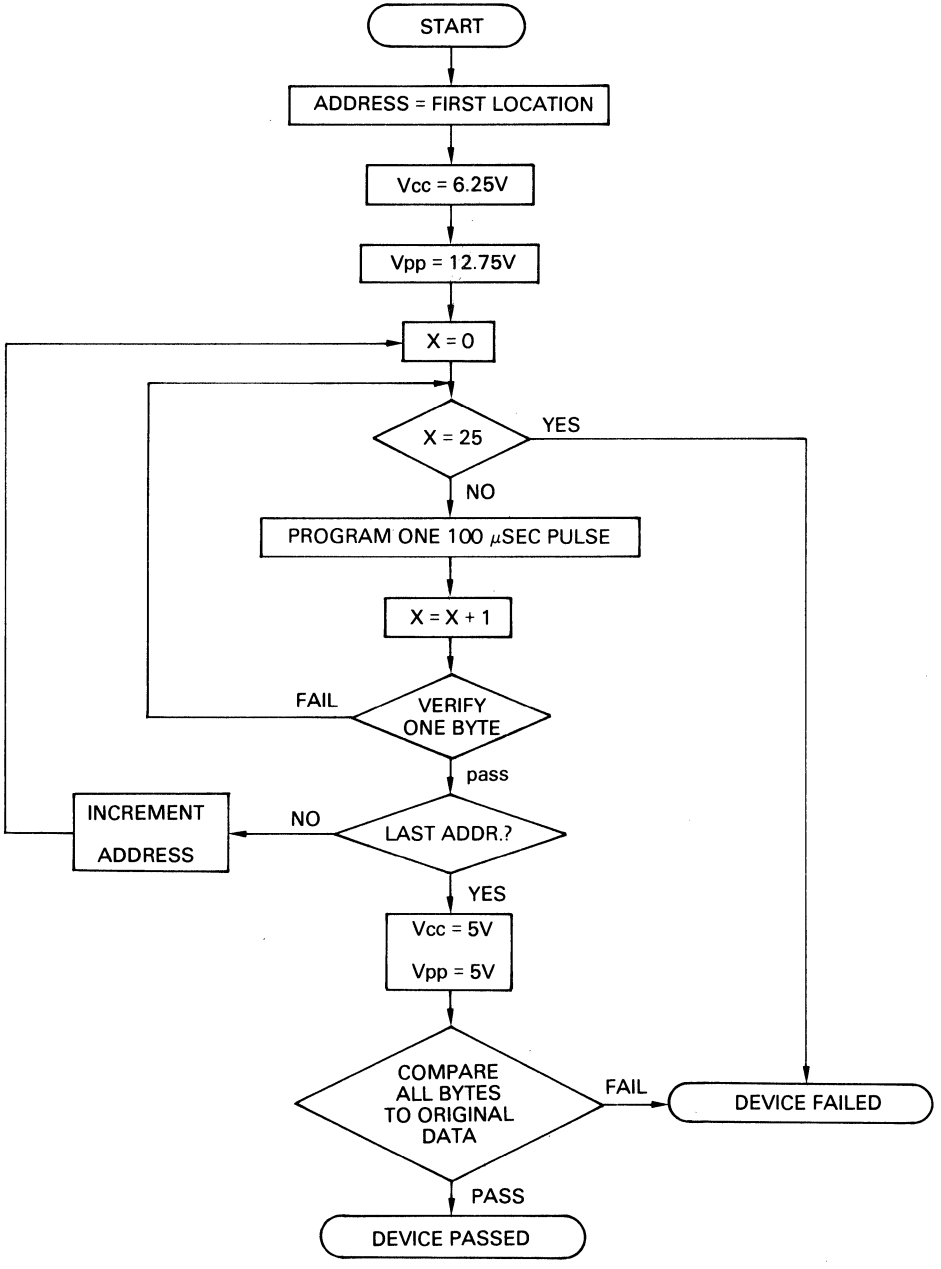


CAPACITANCE

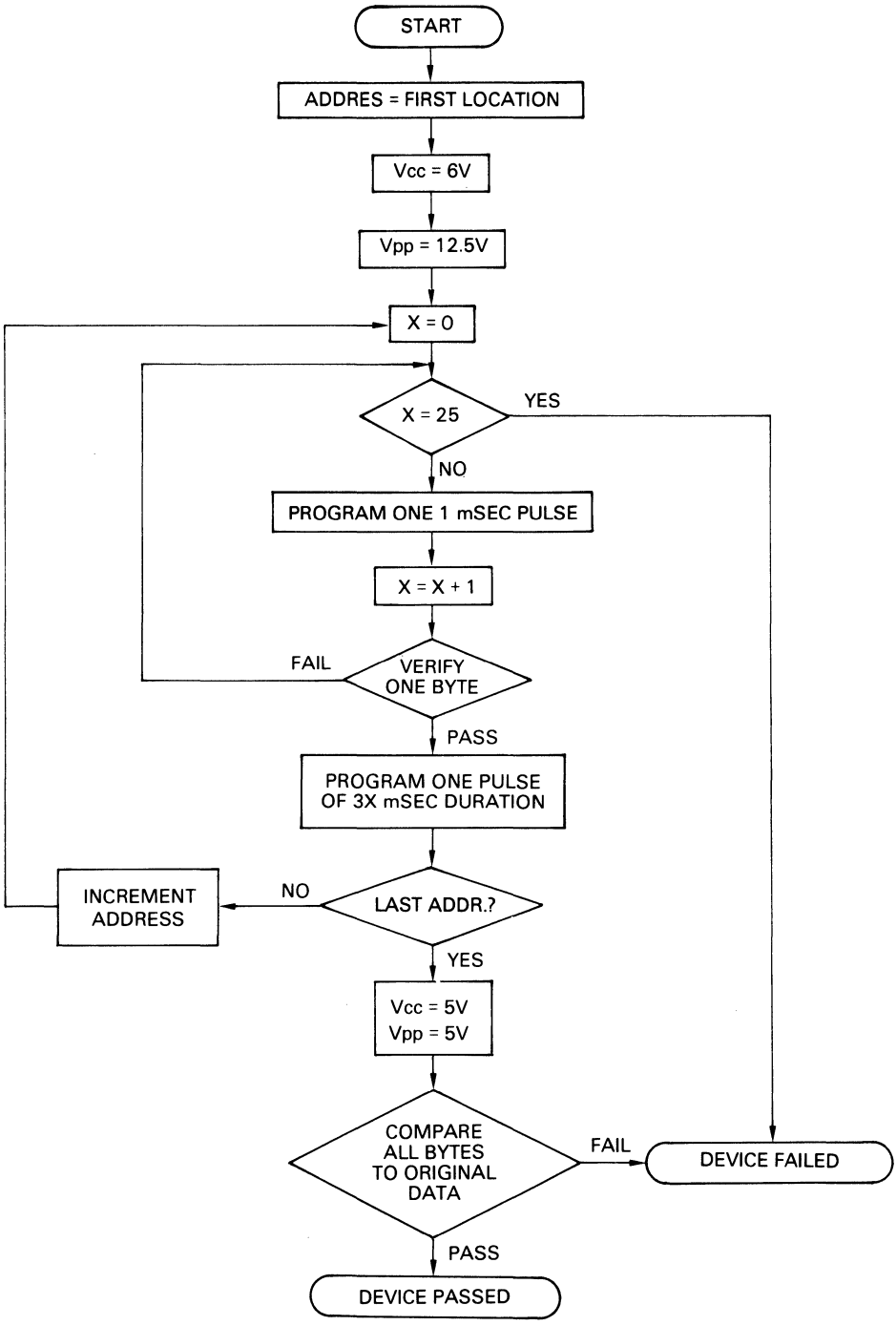
(Ta = 25°C, f = 1 MHz, V_{CC} = 5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	–	15	pF

7



Programming Flowchart Example (I)



Programming Flowchart Example (II)

MSM27C256H

32768 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

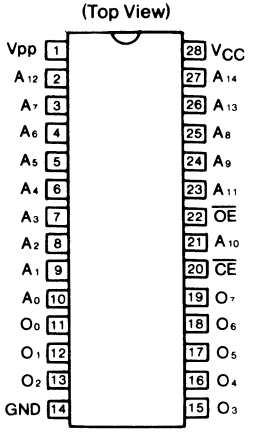
The MSM27C256H is a 32768 words x 8 bit ultraviolet erasable and electrically programmable read-only memory. The MSM27C256H is manufactured by the CMOS double silicon gate technology and is contained in the 28 pin package.

FEATURES

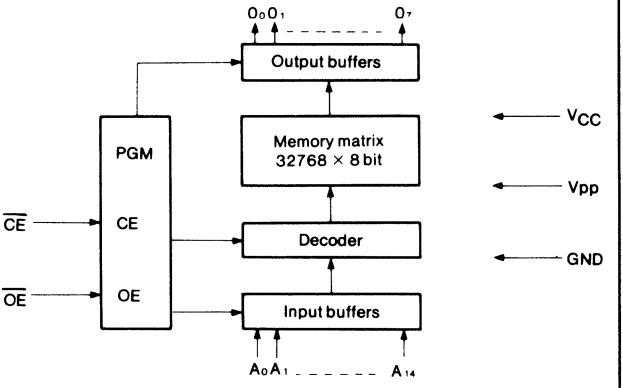
- +5V single power supply
- 32768 words × 8 bit configuration
- Access time:
  MAX 55 ns (MSM27C256H-55)
  MAX 70 ns (MSM27C256H-70)
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- OUTPUT TTL compatible
  (three state output)

7

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	+12.5V	+6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	V_{IH}	+12.5V	+6V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input Voltage	V_{IN}	−0.6V ~ 13V
All Output Voltage	V_{OUT}	−0.6V ~ V_{CC} + 0.5V
V_{CC} Suply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

7

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	3.0	–	V_{CC}+0.5			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.3			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$=V_{IH} f=10MHz	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$=V_{IL} f=10MHz	–	–	100	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+0.5	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −4 mA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 8 mA	–	–	0.45	V

AC CHARACTERISTICS

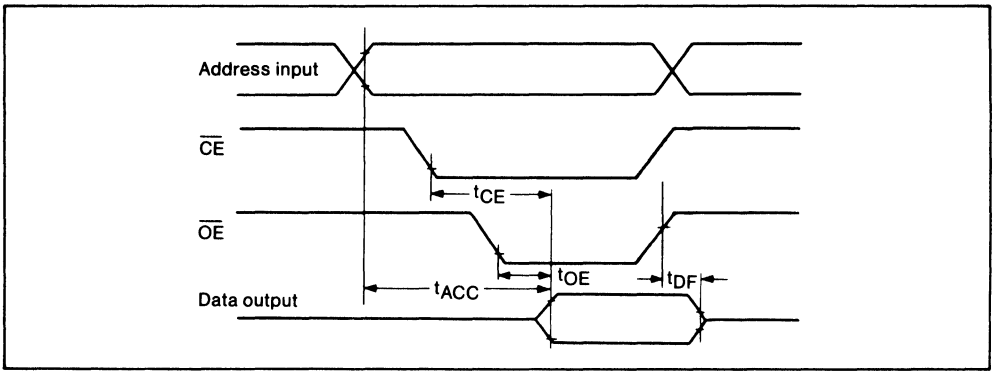
(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	27C256H-55		27C256H-70		Unit
			Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	55	–	70	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	55	–	70	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	25	–	30	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	20	0	25	ns

Measurement condition

Input pulse level ..... 0V and 3.0V
Input timing reference level ..... 0.8V and 2.0V
Output load ..... 1TTL GATE + 30pF
Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

< PROGRAMMING OPERATION >

DC CHARACTERISTICS

(V_{CC} = 5.75 ~ 6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

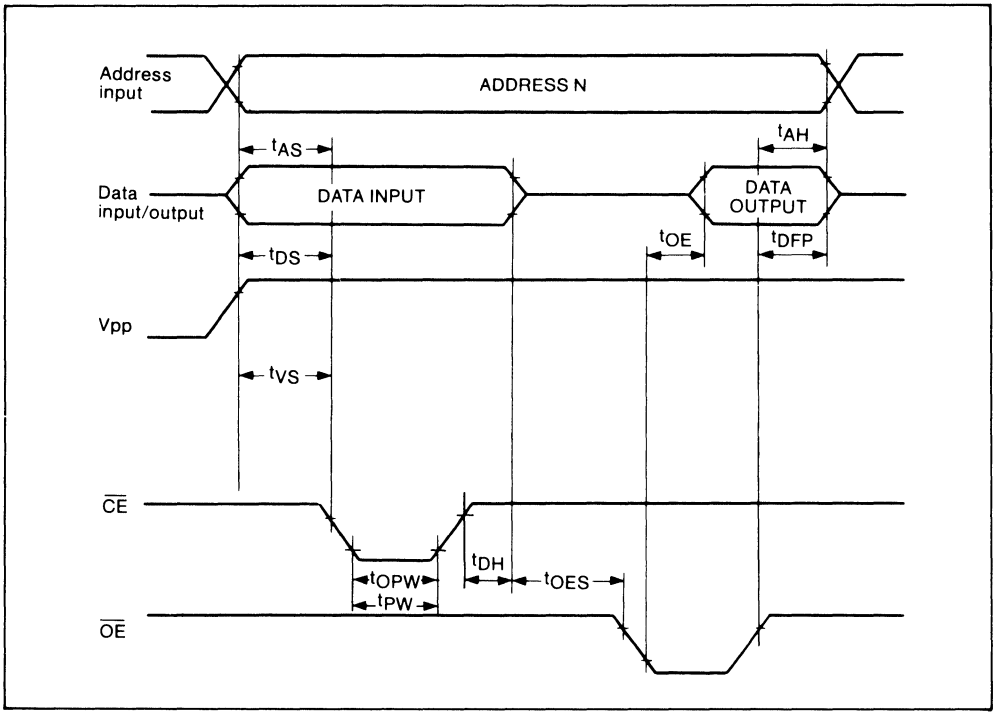
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC} + 0.5	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −4mA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 8mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	V_{CC} = 6V ± 0.25V	0.95	1.0	1.05	ms
$\overline{CE}$ Program Pulse Width	t_{PW}	V_{CC} = 6.25V ± 0.25V	95	100	105	μs
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	V_{CC} = 6V ± 0.25V	2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART

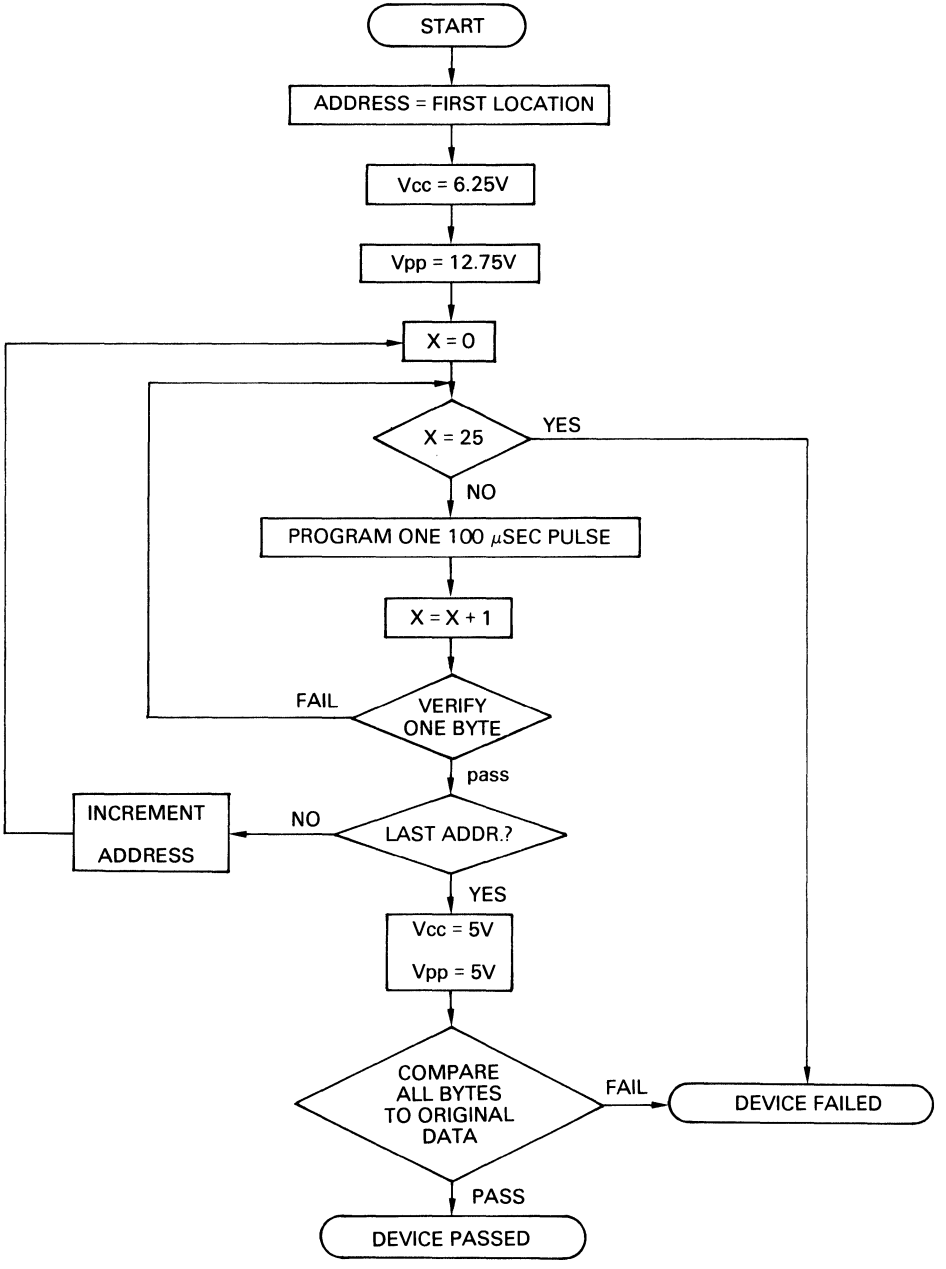


CAPACITANCE

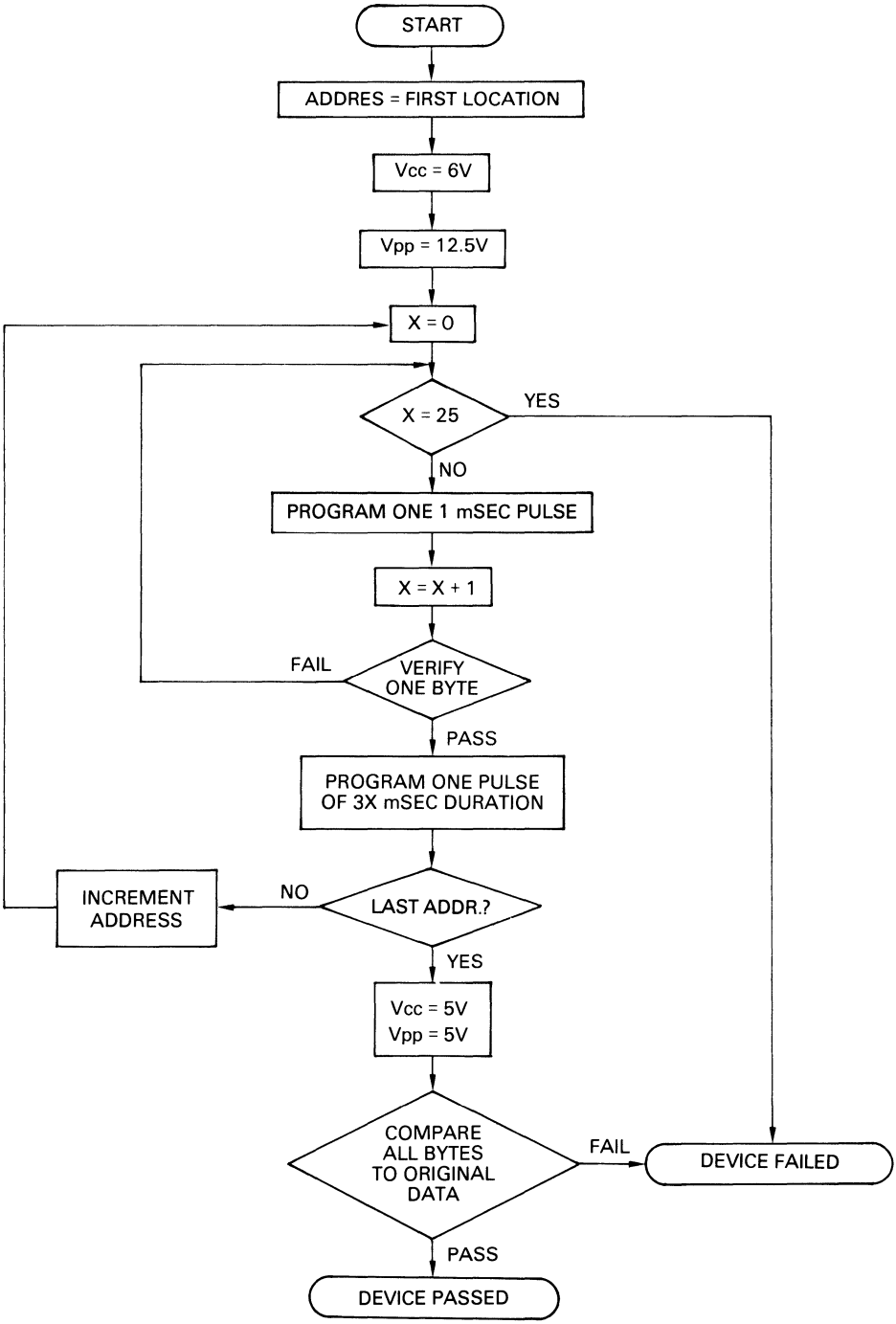
(Ta = 25°C, f = 1 MHz, V_{CC} = 5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	—	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	—	15	pF

7



Programming Flowchart Example (I)



Programming Flowchart Example (II)

MSM27C1024

65536 × 16 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

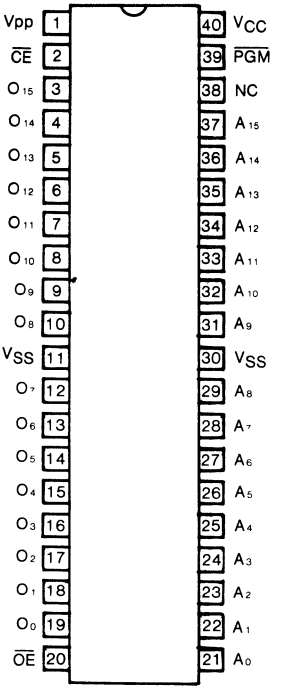
The MSM27C1024 is a 65536 words × 16 bit ultraviolet erasable and electrically programmable read-only memory. Users can freely prepare the memory content, which can be easily changed, so the MSM27C1024 is ideal for microprocessor programs, etc. The MSM27C1024 is manufactured by the CMOS double silicon gate technology and is contained in the 40 pin package.

FEATURES

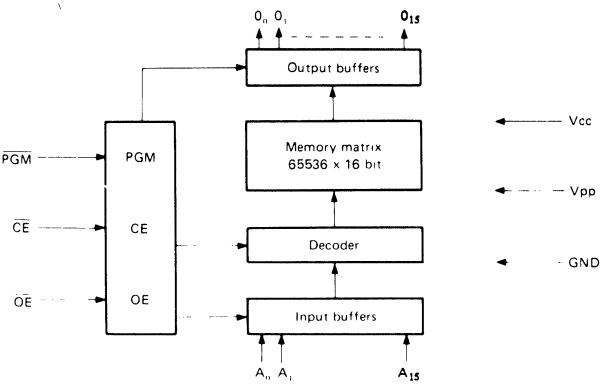
- +5V single power supply
- 65536 words × 16 bit configuration
- Access time:
  MAX120 ns (MSM27C1024-12)
  MAX150 ns (MSM27C1024-15)
  MAX200 ns (MSM27C1024-20)
- Power consumption:
  MAX 165 mW (during operation)
  MAX 5.5mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (three state output)

7

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (2)	$\overline{OE}$ (20)	$\overline{PGM}$ (39)	VPP (1)	VCC (40)	Outputs
Read	V_{IL}	V_{IL}	—	V_{CC}	+5V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	—	V_{CC}	+5V	High impedance
Stand-by	V_{IH}	—	—	V_{CC}	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.75V	+6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.75V	+6.25V	D_{OUT}
Program Inhibit	V_{IH}	—	—	+12.75V	+6.25V	High impedance

NOTES:
—; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	V_{IN} = −0.6V ~ 13V, V_{OUT} = −0.6V ~ V_{CC} + 0.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.5	5.0	5.5	0°C ~ 70°C	V_{CC}=5V±0.5V Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.5	5.0	5.5			V
"H" Level Input Voltage	V_{IH}	2.00	—	V_{CC}+0.5			V
"L" Level Input Voltage	V_{IL}	−0.1	—	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{CC}	–	–	1	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	30	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	10	μ
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+0.5	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

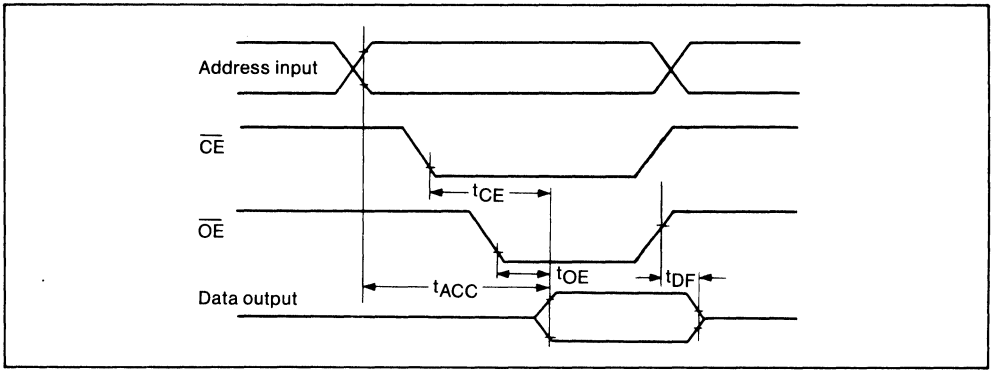
(V_{CC} = 5V±10%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	27C1000-12		27C1000-15		27C1000-20		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL},	–	120	–	150	–	200	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL},	–	120	–	150	–	200	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL},	–	50	–	60	–	70	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL},	0	40	0	50	0	55	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

DC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V±0.25V, Ta = 25°C±5°C)

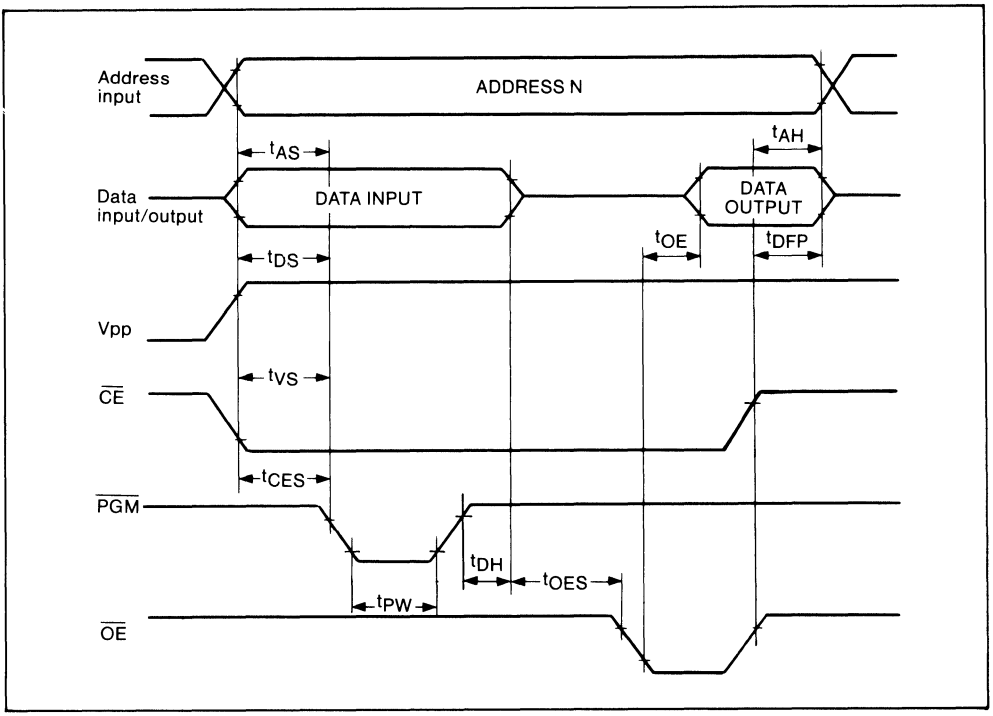
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	30	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+0.5	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V±0.25V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Program Pulse Width	t_{PW}	—	95	100	105	μs
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz, Vcc ≦ 5V)

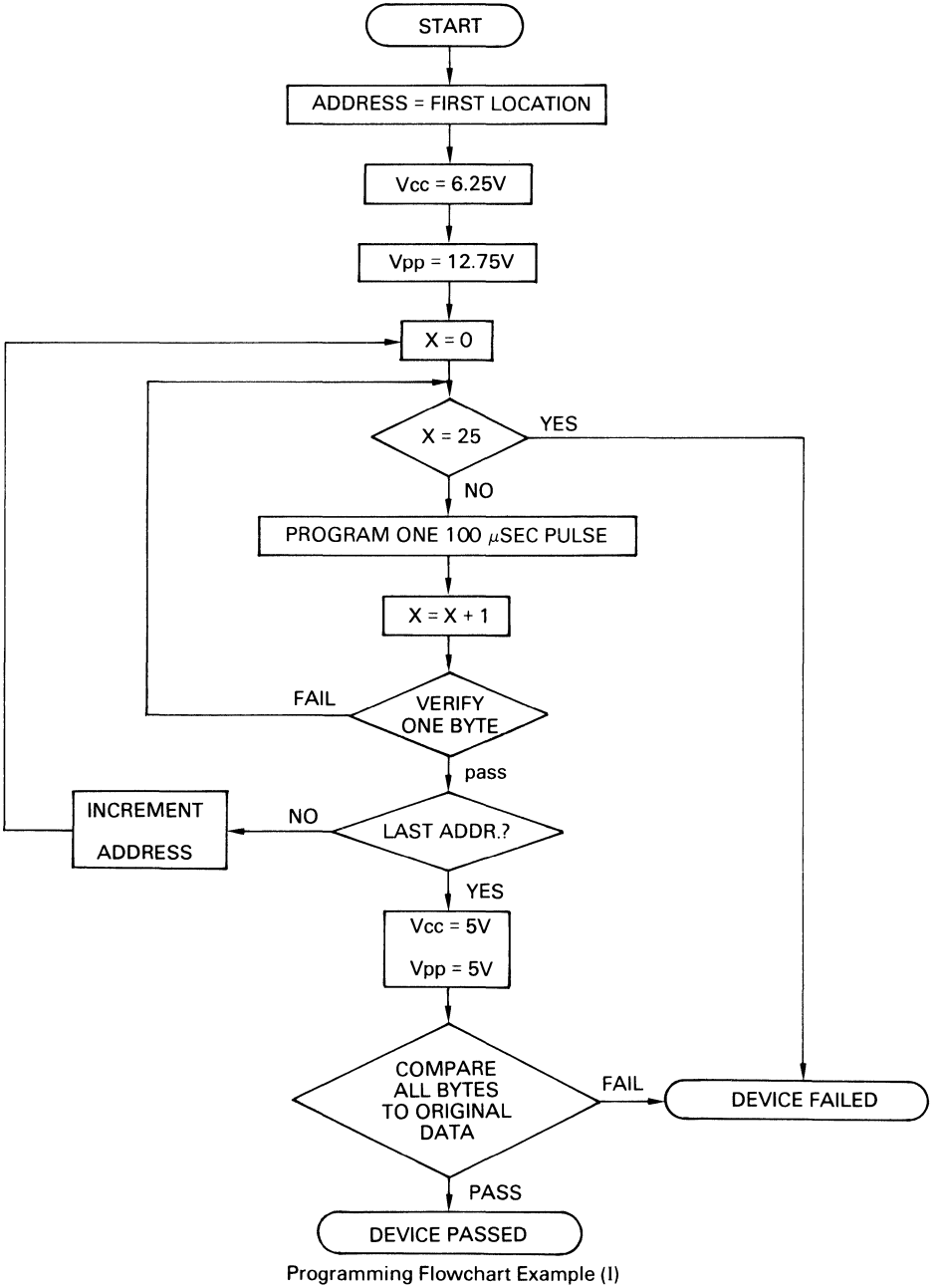
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	–	15	pF

MSM27C1024 **IDENTIFIER BYTES**

Code \ Pins	A_0 (21)	$D_{15} \sim D_8$ (3) ~ (10)	D_7 (12)	D_6 (13)	D_5 (14)	D_4 (15)	D_3 (16)	D_2 (17)	D_1 (18)	D_0 (19)	Hex Data
Manufacter Code	V_{IL}	0 ~ 0	1	0	1	0	1	1	1	0	00AE
Device Code	V_{IH}	0 ~ 0	0	0	0	0	0	1	1	1	0007

Notes: 1. $A_9 = 12.0 \pm 0.5V$

2. $A_1 \sim A_8$, $A_{10} \sim A_{15}$, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$ OR V_{IL}, Vpp = V_{CC}



Programming Flowchart Example (I)

OKI semiconductor

MSM27C2000

262144 × 8 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

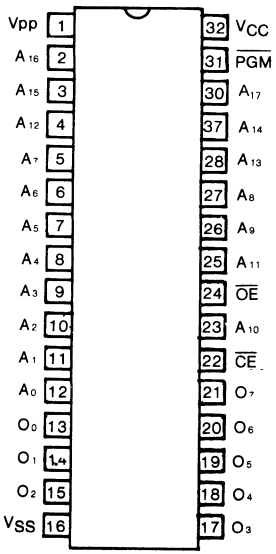
GENERAL DESCRIPTION

The MSM27C2000 is a 262144 words × 8 bit ultraviolet erasable and electrically programmable read-only memory. The MSM27C2000 is manufactured by CMOS double silicon gate technology and is contained in the 32 pin package.

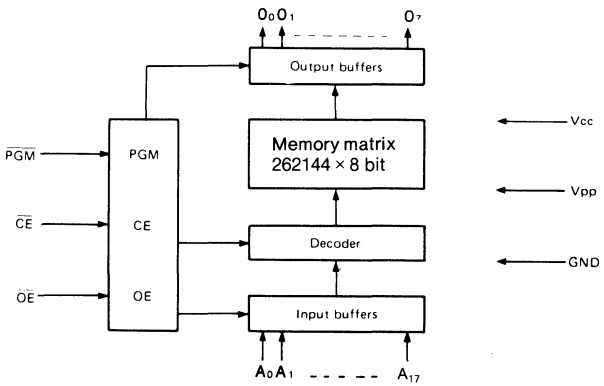
FEATURES

- +5V single power supply
- 262,144 words × 8 bit configuration
- Acces time:
  MAX100 ns (MSM27C2000-10)
  MAX120 ns (MSM27C2000-12)
  MAX150 ns (MSM27C2000-15)
- Power consumption:
  MAX385 mW (during operation)
  MAX28 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (three state output)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

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FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	VPP (1)	VCC (32)	Outputs
Read	V_{IL}	V_{IL}	—	+5V	+5V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	—	+5V	+5V	High impedance
Stand-by	V_{IH}	—	—	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.75V	+6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.75V	+6.25V	D_{OUT}
Program Inhibit	V_{IH}	—	—	+12.75V	+6.25V	High impedance

NOTES:
—; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}	−0.6V ~ 13.5V
	V_{OUT}	−0.6V ~ V_{CC}+0.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

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ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.5	5.0	5.5	0°C ~ 70°C	V_{CC}=5V± 5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.5	5.0	5.5			V
"H" Level Input Voltage	V_{IH}	2.0	–	V_{CC}+0.5			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE} = V_{IH}$	–	–	5	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE} = V_{IL}$	–	–	70	mA
Program Power Current	I_{PP_1}	$V_{PP}=V_{CC}$	–	–	100	μA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+0.5	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

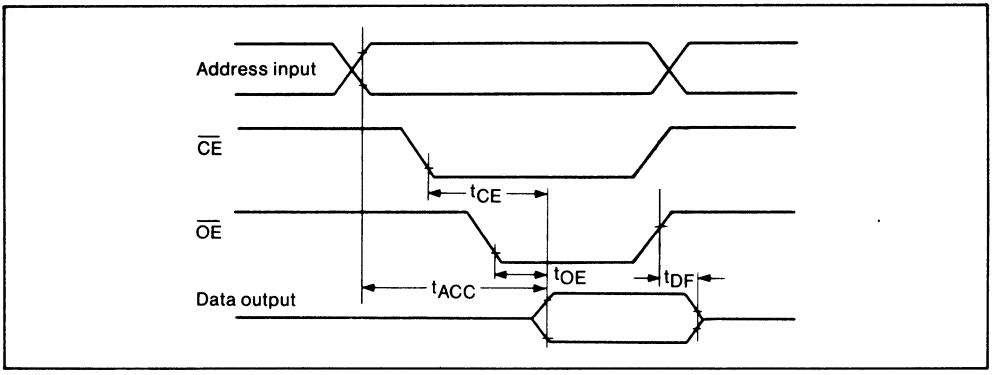
(V_{CC} = 5V±10%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	27C2000-10		27C200-12		27C2000-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$	–	100	–	120	–	150	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE} = V_{IL}$	–	100	–	120	–	150	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE} = V_{IL}$	–	50	–	50	–	60	ns
Output Disable Time	t_{DF}	$\overline{CE} = V_{IL}$	0	40	0	40	0	50	ns

Measurement condition

Input pulse level ..... 0.45V and 2.4V
Input timing reference level ..... 0.8V and 2.0V
Output load ..... 1TTL GATE + 100pF
Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
$\overline{OE}$
Data output
t_{CE}
t_{OE}
t_{DF}
t_{ACC}

7

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, V_{PP} = 12.75V±0.25V, Ta = 25°C±5°C)

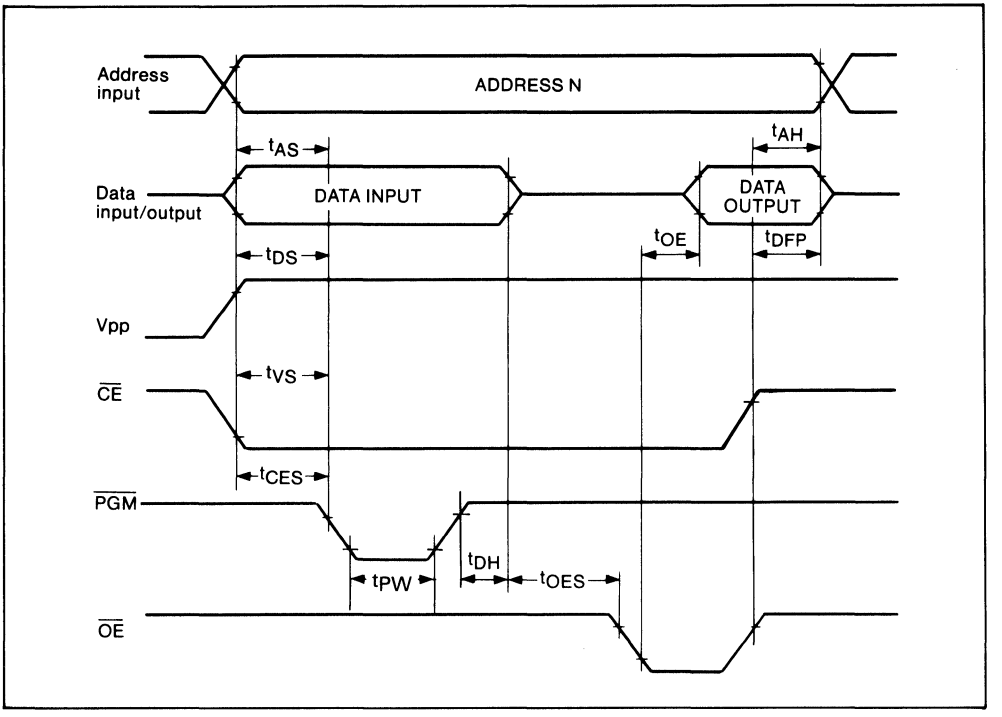
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	70	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+0.5	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V±0.25V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ program Pulse Width	t_{PW}	—	95	100	105	μs
$\overline{CE}$ Set-up Time	t_{CES}	—	2	—	–	μs
Data Valid from $\overline{OE}$	t_{OE}	—	—	–	150	ns

TIME CHART



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CAPACITANCE

(Ta = 25°C, f = 1 MHz, Vcc = 5V)

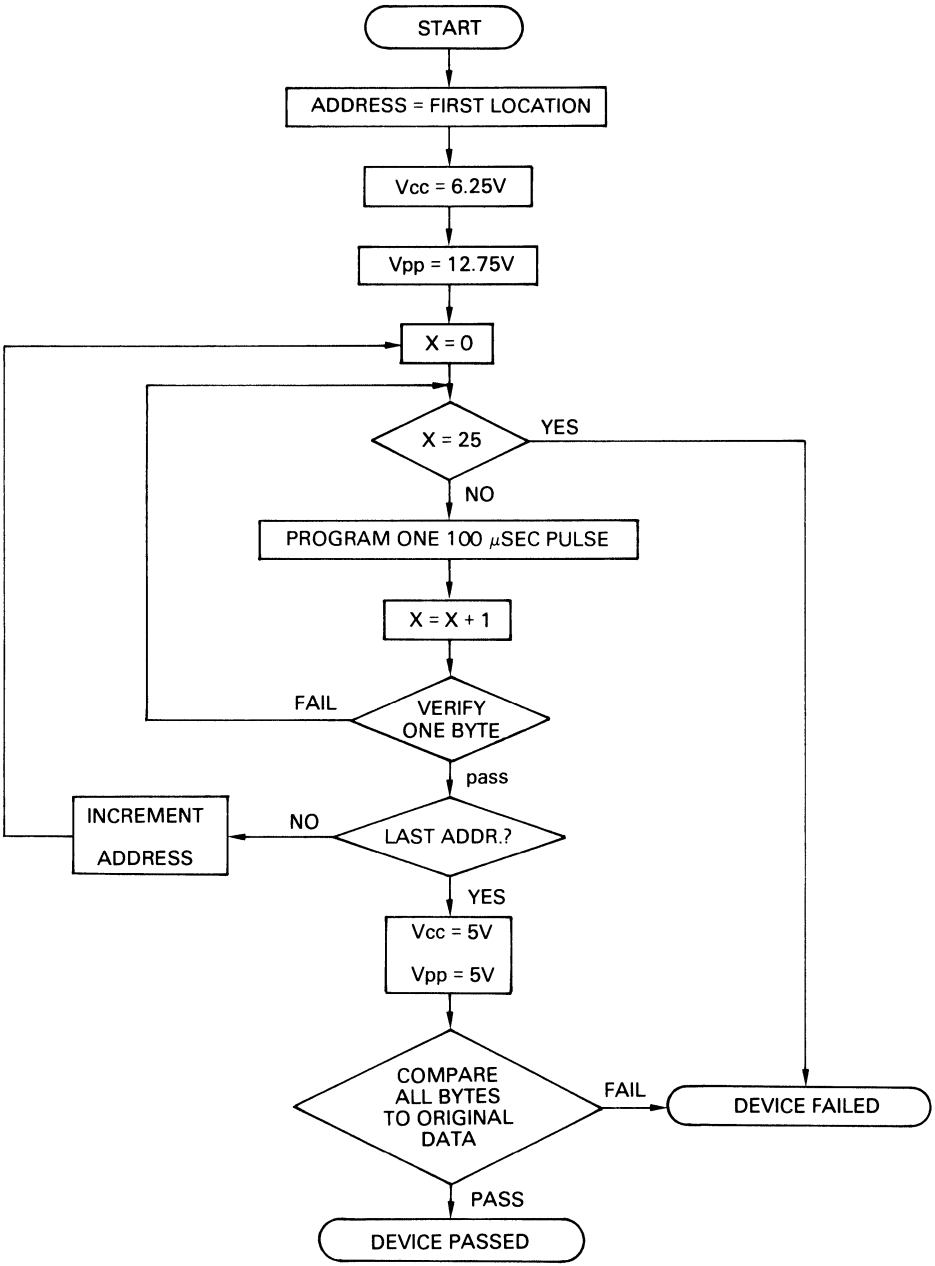
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	–	15	pF

MSM27C2000 **IDENTIFIER BYTES**

Pins / Code	A_0 (12)	D_7 (21)	D_6 (20)	D_5 (19)	D_4 (18)	D_3 (17)	D_2 (15)	D_1 (14)	D_0 (13)	Hex Data
Manufacter Code	V_{IL}	1	0	1	0	1	1	1	0	AE
Device Code	V_{IH}	1	0	0	0	1	0	0	1	89

Notes: 1. $A_9 = 12.0 \pm 0.5V$

2. $A_1 \sim A_8$, $A_{10} \sim A_{17}$, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$ OR V_{IL}, $Vpp = V_{CC}$



Programming Flowchart Example (I)

Preliminary

OKI semiconductor

MSM27C2048

131072 × 16 BIT UV ERASABLE ELECTRICALLY PROGRAMMABLE READ-ONLY MEMORY

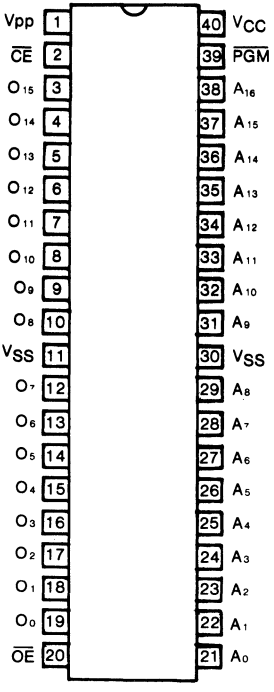
GENERAL DESCRIPTION

The MSM27C2048 is a 131072 words × 16 bit ultraviolet erasable and electrically programmable read-only memory. The MSM27C2048 is manufactured by CMOS double silicon gate technology and is contained in the 40 pin package.

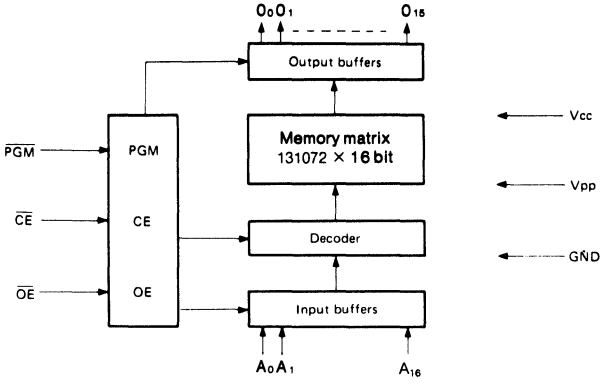
FEATURES

- +5V single power supply
- 131072 words × 16 bit configuration
- Acces time:
  MAX100 ns (MSM27C2048-10)
  MAX120 ns (MSM27C2048-12)
  MAX150 ns (MSM27C2048-15)
- Power consumption:
  MAX550 mW (during operation)
  MAX28 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (three state output)

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

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FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (2)	$\overline{OE}$ (20)	$\overline{PGM}$ (39)	VPP (1)	VCC (40)	Outputs
Read	V_{IL}	V_{IL}	—	+5V	+5V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	—	+5V	+5V	High impedance
Stand-by	V_{IH}	—	—	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.75V	+6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.75V	+6.25V	D_{OUT}
Program Inhibit	V_{IH}	—	—	+12.75V	+6.25V	High impedance

NOTES:
—; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}	−0.6V ~ 13.5V
	V_{OUT}	−0.6V ~ V_{CC} +0.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ **14V**

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.5	5.0	5.5	0°C ~ 70°C	V_{CC}=5V±10% V_{PP}=V_{CC}	V
Vpp Voltage	Vpp	4.5	5.0	5.5			V
"H" Level Input Voltage	V_{IH}	2.00	–	V_{CC}+0.5			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH}	–	–	5	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP_1}	Vpp = V_{CC}	–	–	100	μA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+0.5	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

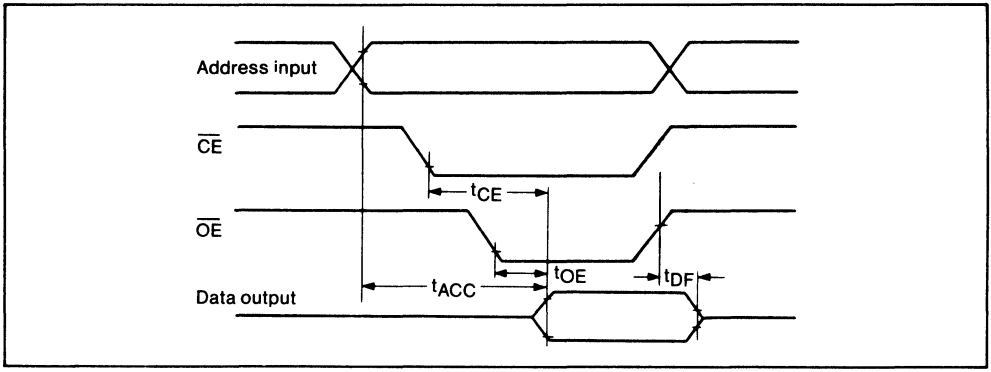
(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	27C2048-10		27C2048-12		27C2048-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL},	–	100	–	120	–	150	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL},	–	100	–	120	–	150	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL},	–	50	–	50	–	60	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL},	0	40	0	40	0	50	ns

Measurement condition

Input pulse level ..... 0.45V and 2.4V
Input timing reference level ..... 0.8V and 2.0V
Output load ..... 1TTL GATE + 100pF
Output timing reference level ..... 0.8V and 2.0V

TIME CHART


Address input
$\overline{CE}$
t_{CE}
$\overline{OE}$
t_{OE}
t_{DF}
t_{ACC}
Data output

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V±0.25V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+0.5	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V±0.25V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Program Pulse Width	t_{PW}	—	95	100	105	μs
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

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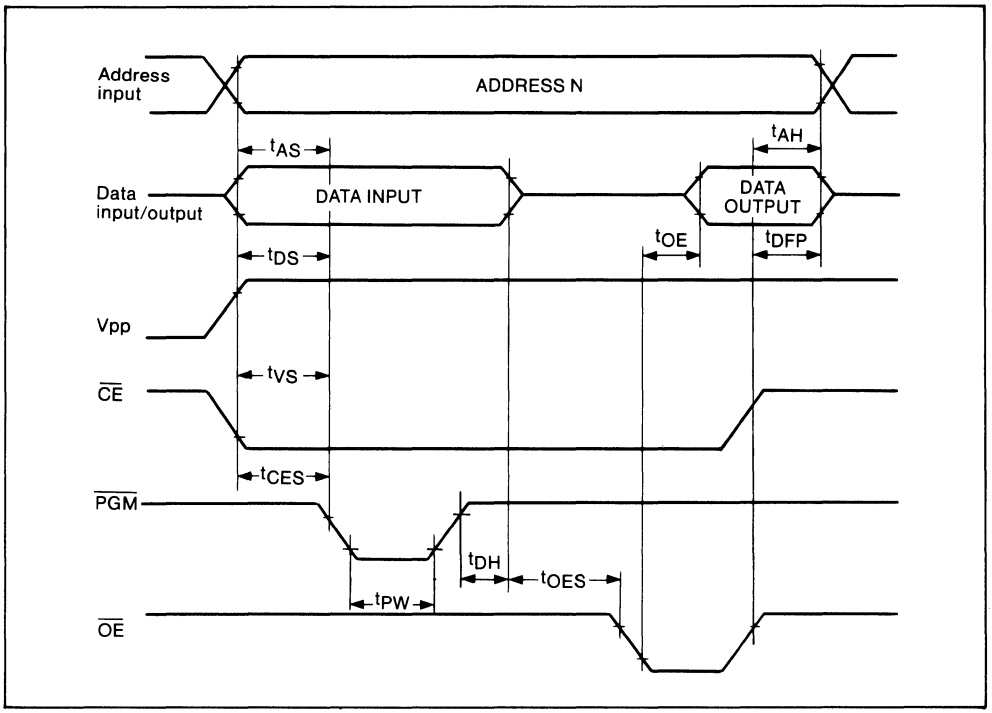
TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz, Vcc = 5V)

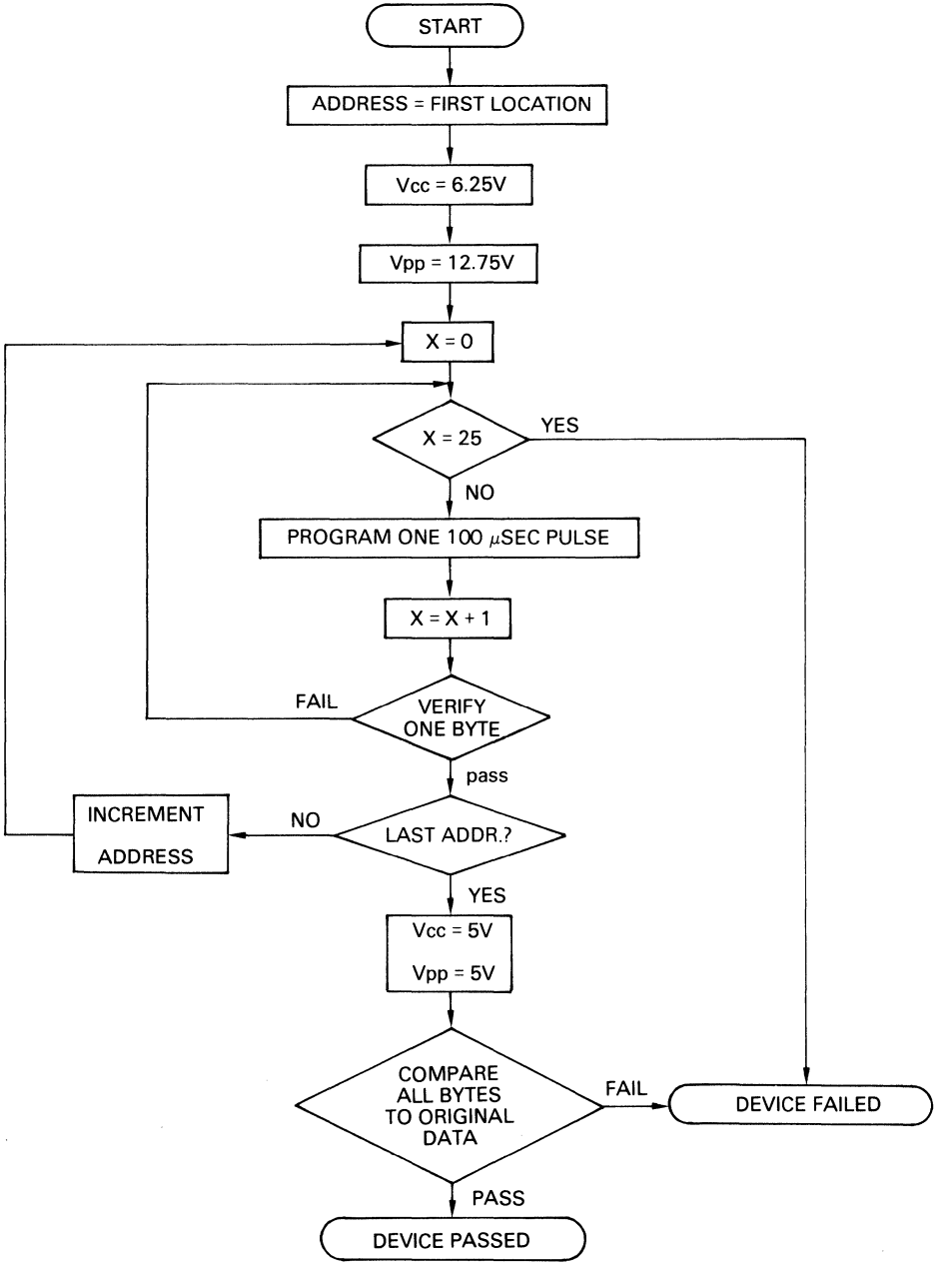
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	–	15	pF

MSM27C2048 **IDENTIFIER BYTES**

Pins / Code	A_0 (21)	$D_{15} \sim D_8$ (3) ~ (10)	D_7 (12)	D_6 (13)	D_5 (14)	D_4 (15)	D_3 (16)	D_2 (17)	D_1 (18)	D_0 (19)	Hex Data
Manufacter Code	V_{IL}	0 ~ 0	1	0	1	0	1	1	1	0	00AE
Device Code	V_{IH}	0 ~ 0	0	0	0	0	1	0	1	1	000B

Notes: 1. $A_9 = 12.0 \pm 0.5V$

2. $A_1 \sim A_8$, $A_{10} \sim A_{16}$, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$ OR V_{IL}, $Vpp = V_{CC}$



Programming Flowchart Example (I)

MSM2764AZB

8,192 × 8-BIT ONE TIME PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

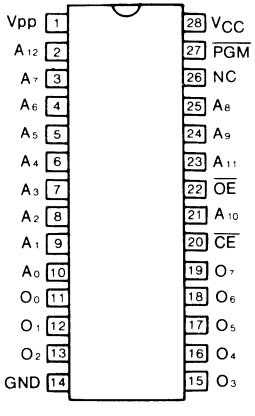
The MSM2764AZB is a 8,192 words × 8-bit electrically programmable read-only memory. The MSM2764AZB is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.
(OKI can provide programming service as per customer's request.)

FEATURES

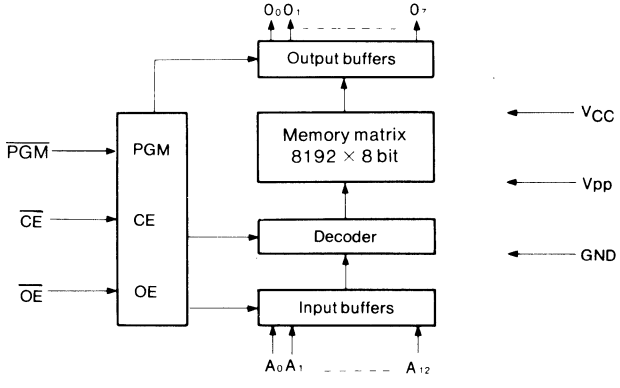
- +5V single power supply
- 8,192 words × 8-bit configuration
- Access time: MAX150 ns
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible
  (3-state output)
- 28-pin DIP

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

—; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

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ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Unit
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND.

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

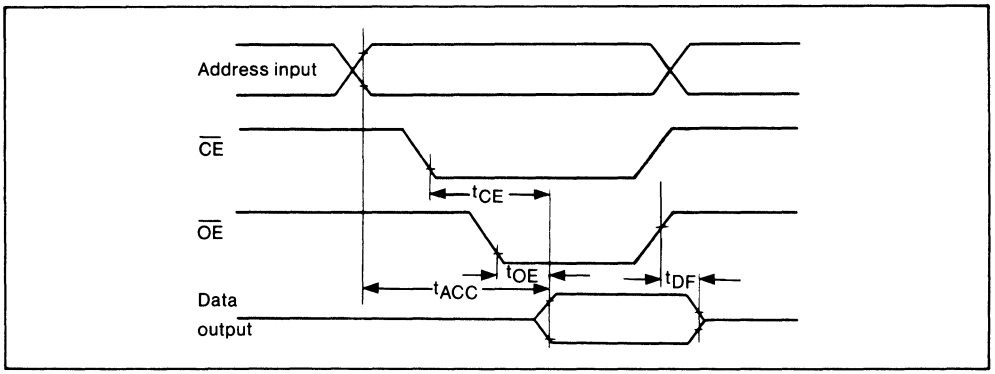
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	150	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	150	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	60	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	50	ns

TIME CHART



Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

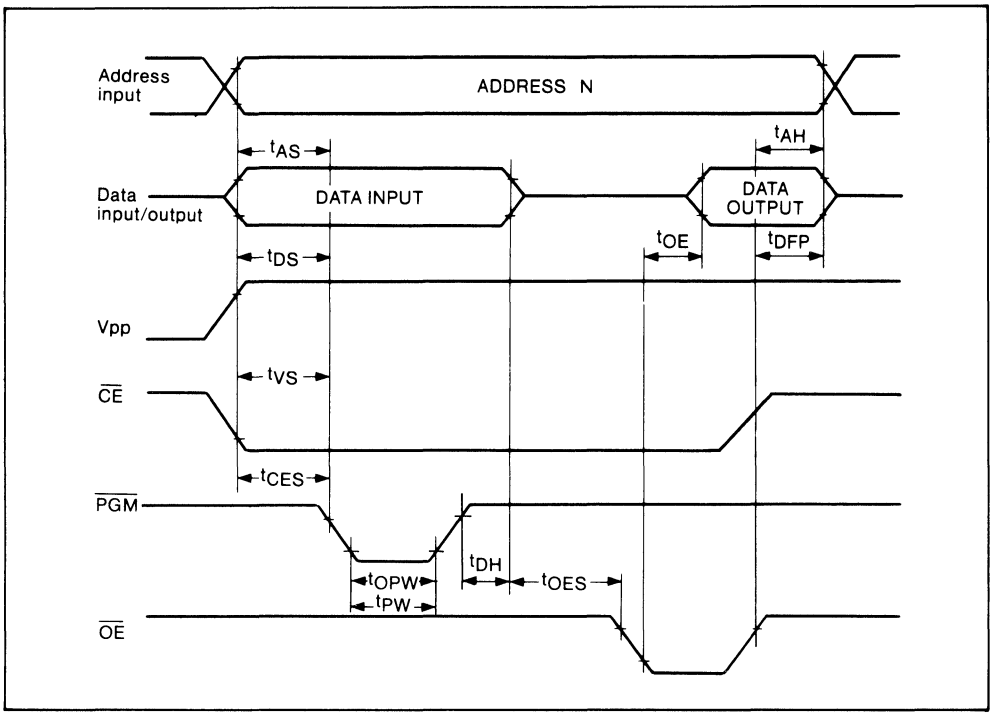
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	V_{CC} = 6V ± 0.25V	0.95	1.0	1.05	ms
$\overline{PGM}$ High Speed Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25V ± 0.25V	95	100	105	μs
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	V_{CC} = 6V ± 0.25V	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz, Vcc = 5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

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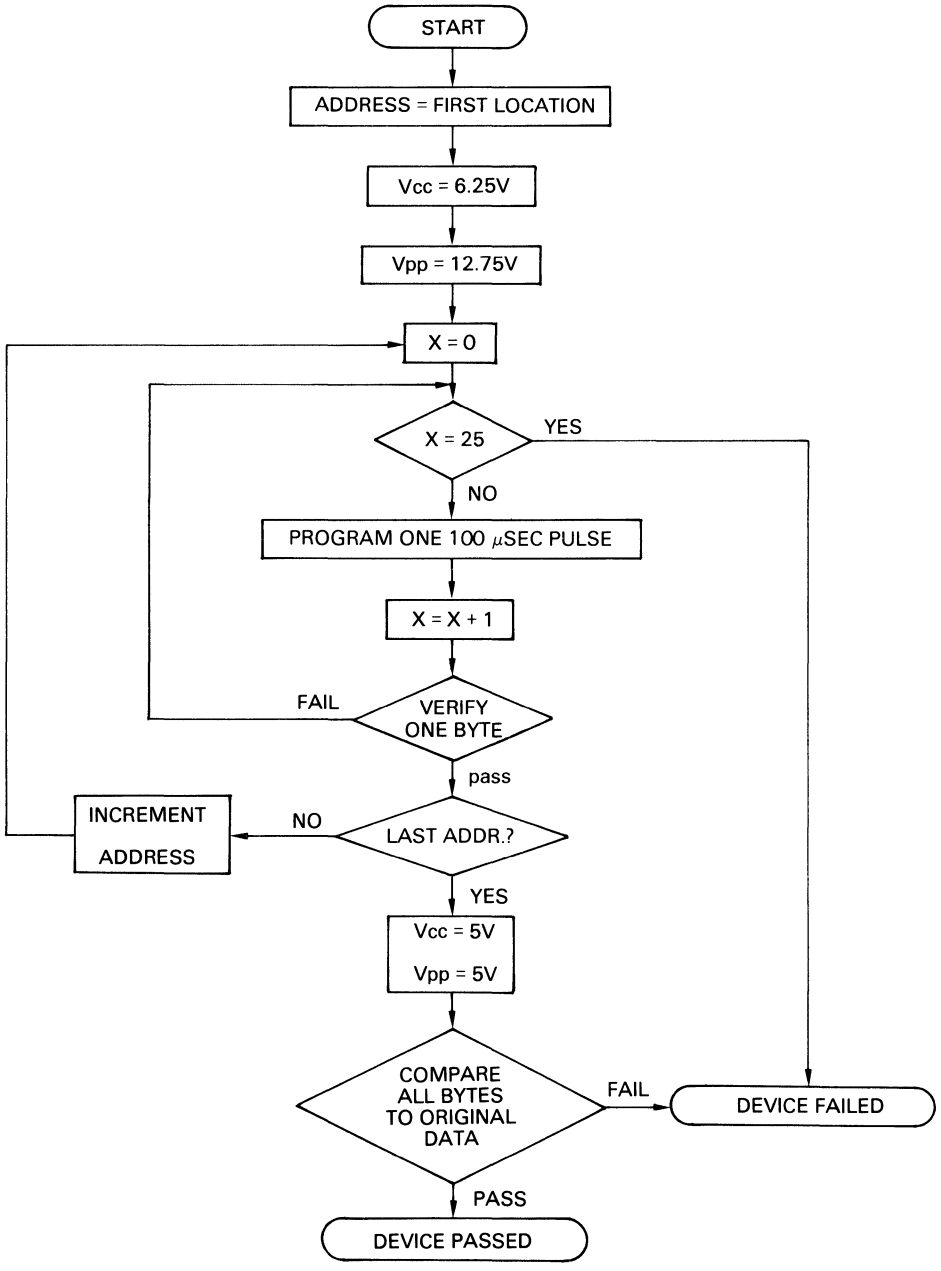
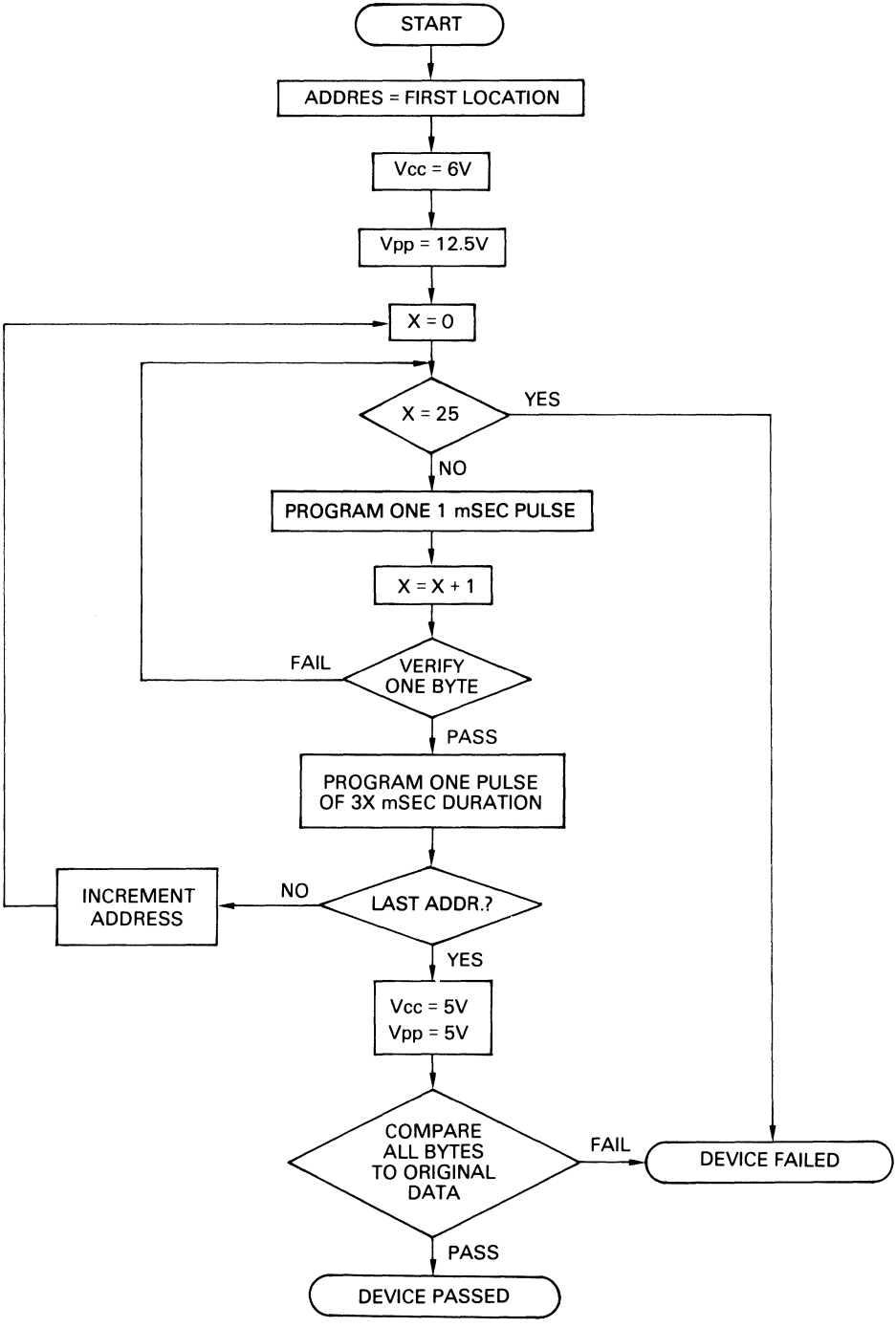


Programming Flowchart Example (I)



Programming Flowchart Example (II)

MSM27128AZB

16,384 × 8-BIT ONE TIME PROGRAMMABLE READ-ONLY MEMORY

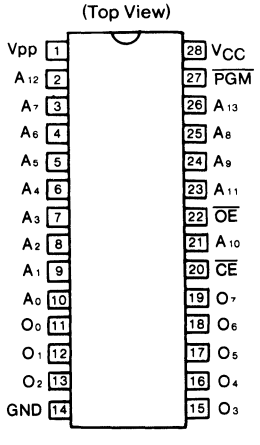
GENERAL DESCRIPTION

The MSM27128AZB is a 16,384 words × 8-bit electrically programmable read-only memory. The MSM27128AZB is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.
(OKI can provide programming service as per customer's request.)

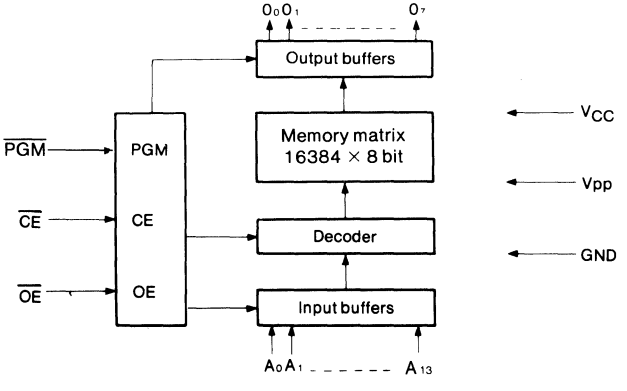
FEATURES

- +5V single power supply
- 16,384 words × 8-bit configuration
- Access time: MAX150 ns
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (three state output)
- 28-pin DIP

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	V_{IH}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.5V	+6V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	–	–	+12.5V	+6V	High impedance

—; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}, V_{OUT}	−0.6V ~ 13.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND.

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP_1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	150	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	150	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	–	60	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}, $\overline{PGM}$ = V_{IH}	0	50	ns

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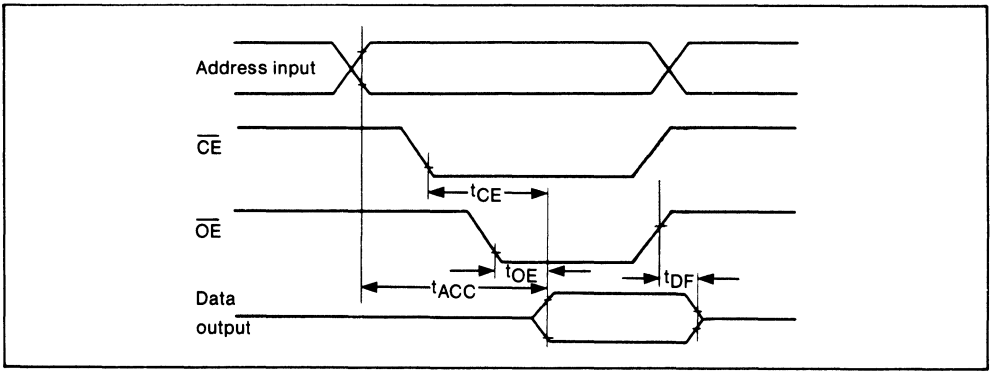
TIME CHART



Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

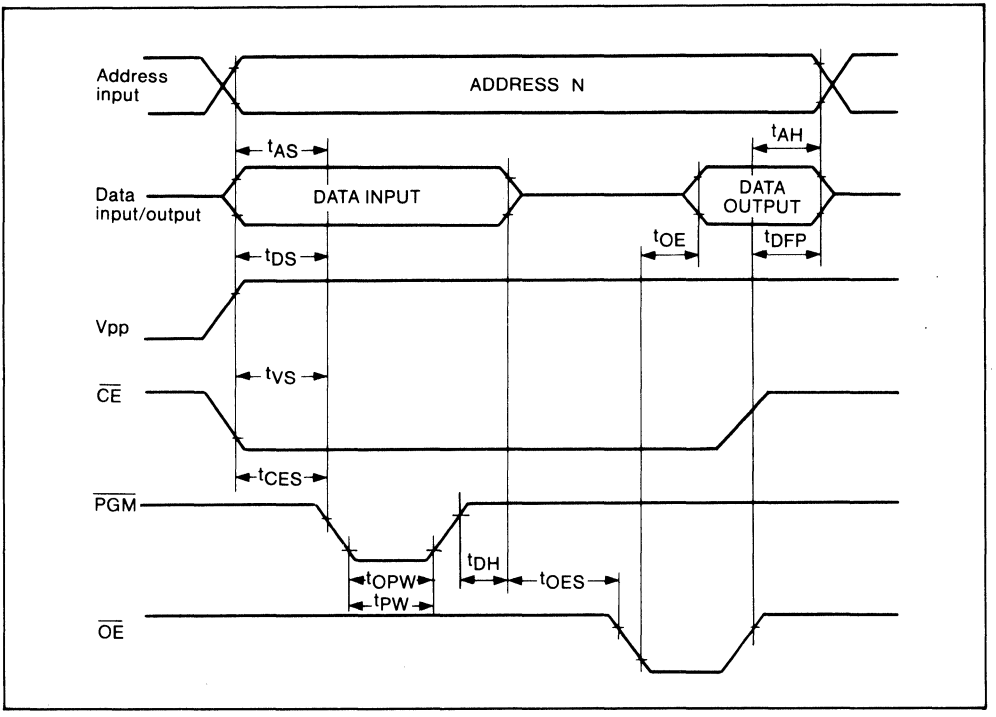
AC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Initial Program Pulse Width	t_{PW}	V_{CC} = 6V ± 0.25V	0.95	1.0	1.05	ms
$\overline{PGM}$ High Speed Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25V ± 0.25V	95	100	105	μs
$\overline{PGM}$ Overprogram Pulse Width	t_{OPW}	V_{CC} = 6V ± 0.25V	2.85	–	78.75	ms
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

7

TIME CHART

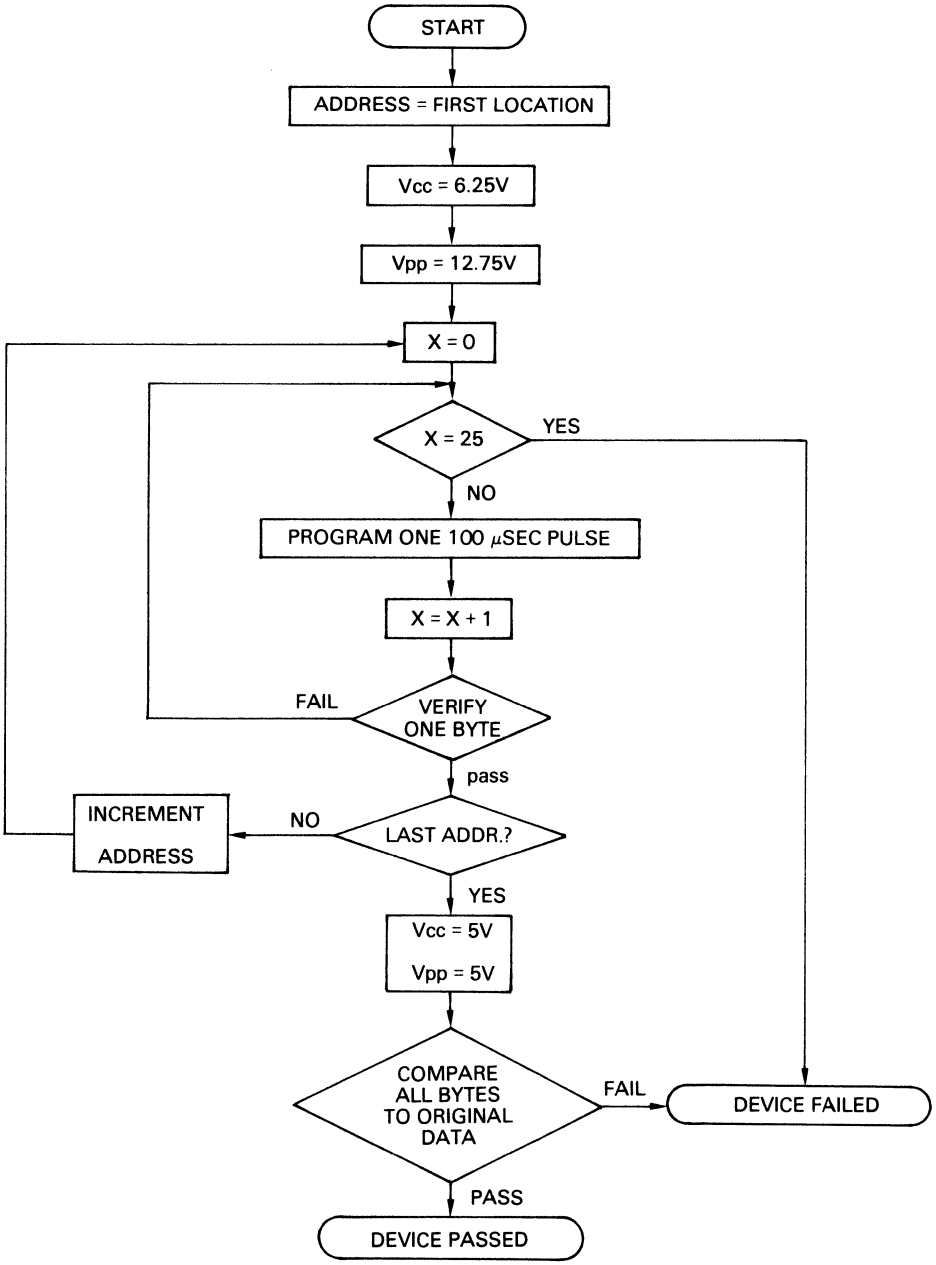


7

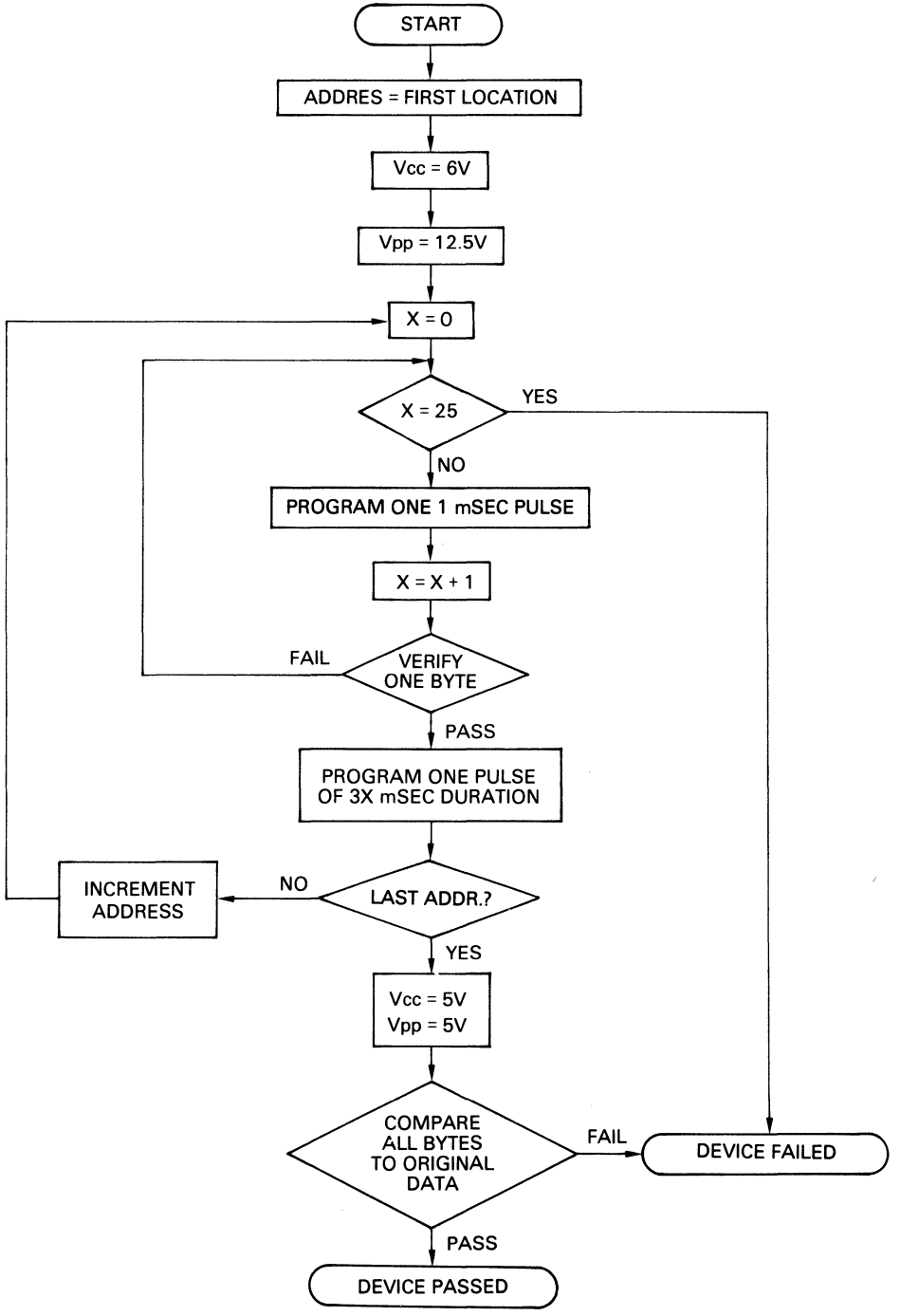
CAPACITANCE

(Ta = 25°C, f = 1 MHz, Vcc = 5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF



Programming Flowchart Example (I)



Programming Flowchart Example (II)

MSM27256

32,768 × 8-BIT ONE TIME PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

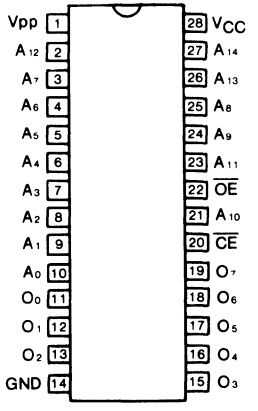
The MSM27256ZB is a 32768 words × 8-bit electrically programmable read-only memory. The MSM27256ZB is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.
(OKI can provide programming service as per customer's request.)

FEATURES

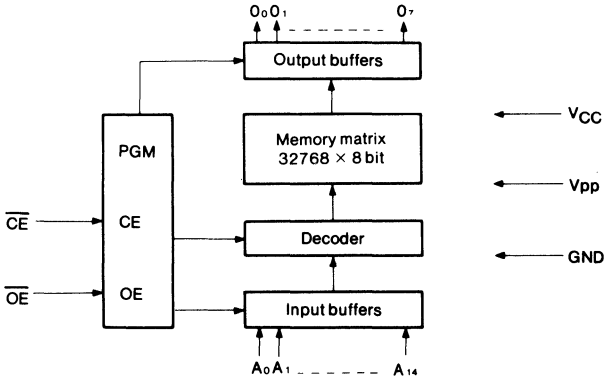
- +5V single power supply
- 32768 words × 8-bit configuration
- Access time: MAX170 ns
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (3-state output)
- 28-pin DIP

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	+12.5V	+6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	V_{IH}	+12.5V	+6V	High impedance

—; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}	−0.6V ~ 13.5V
	V_{OUT}	−0.6V ~ 7V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

7

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Unit
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

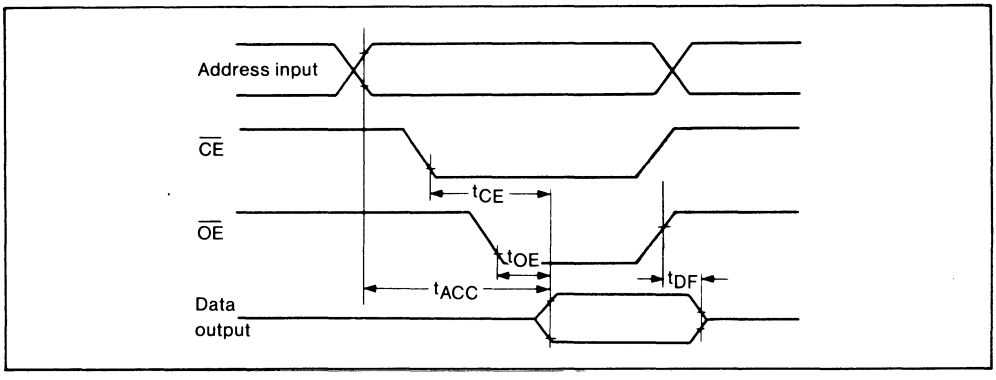
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	170	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	170	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	60	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	ns

TIME CHART



Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

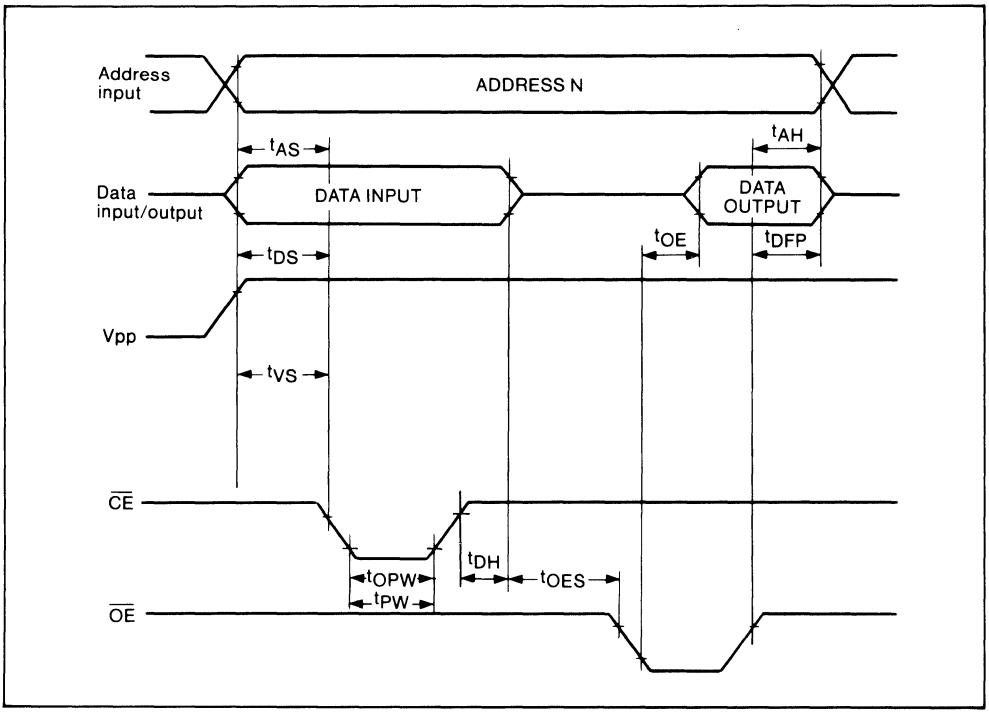
AC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	V_{CC} = 6V ± 0.25V	0.95	1.0	1.05	ms
$\overline{CE}$ High Speed Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25V ± 0.25V	95	100	105	μs
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	V_{CC} = 6V ± 0.25V	2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

7

TIME CHART

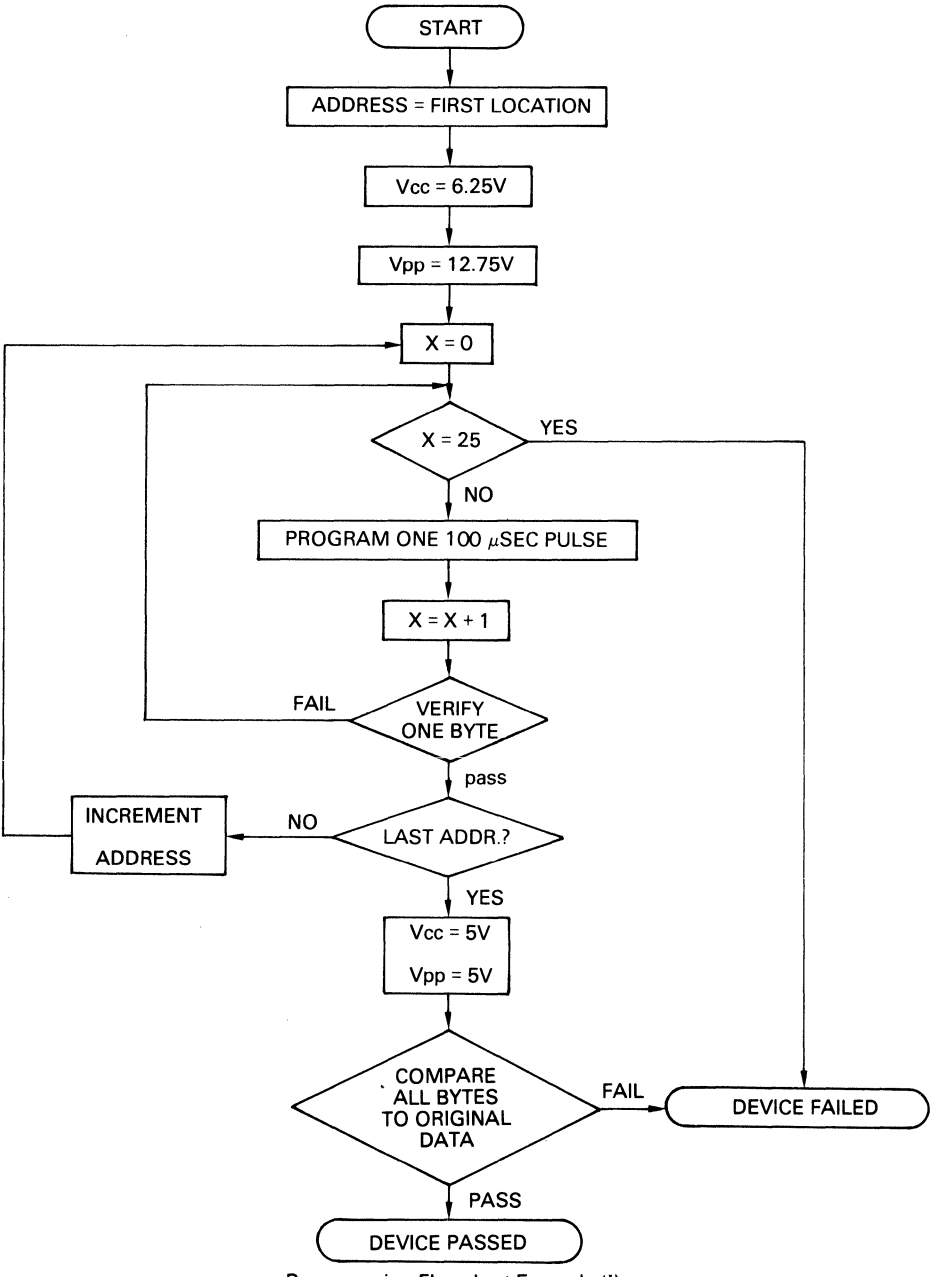


CAPACITANCE

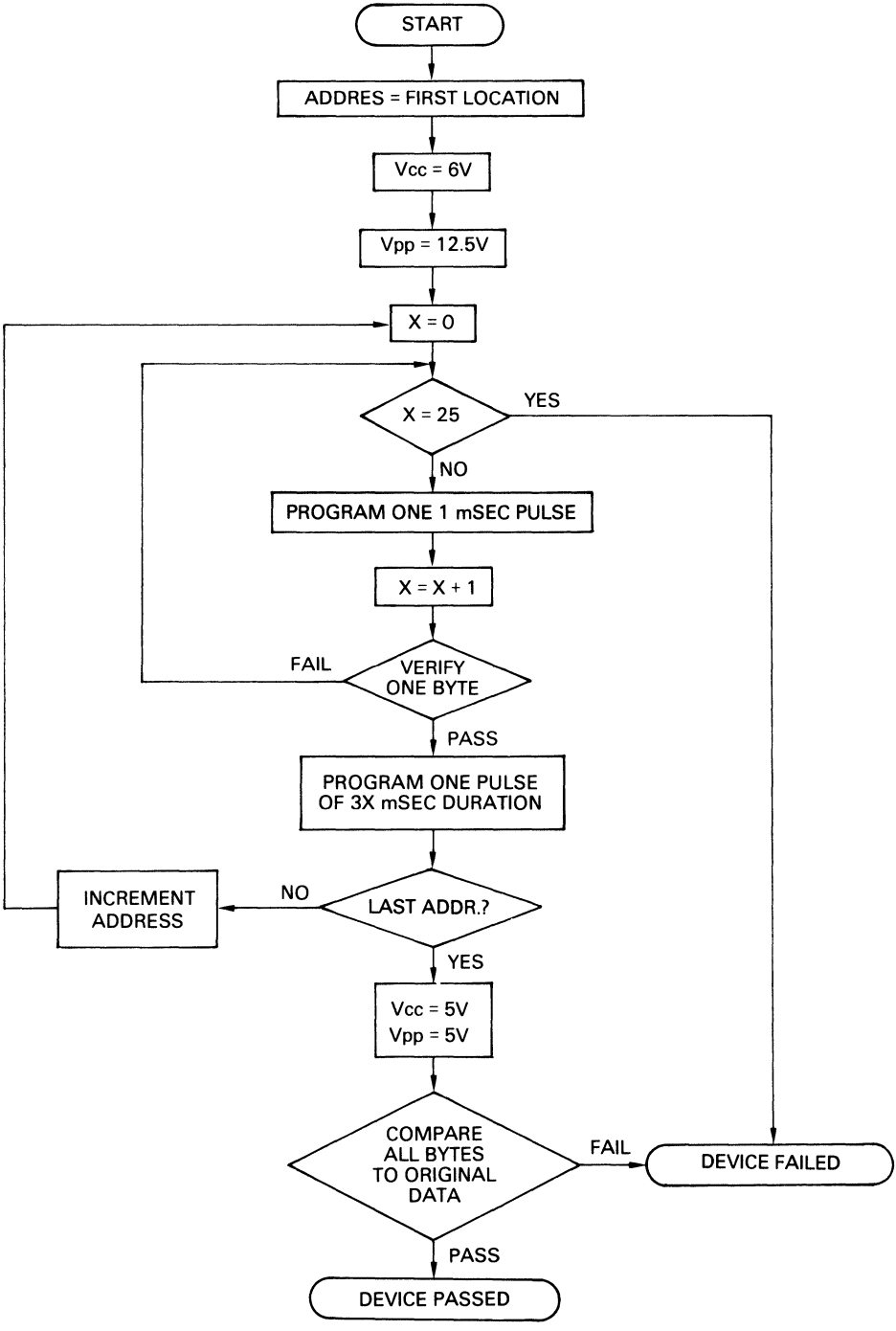
(Ta = 25°C, f = 1 MHz, Vcc = 5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF

7



Programming Flowchart Example (I)



Programming Flowchart Example (II)

MSM27512ZB

65536 × 8-BIT ONE TIME PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

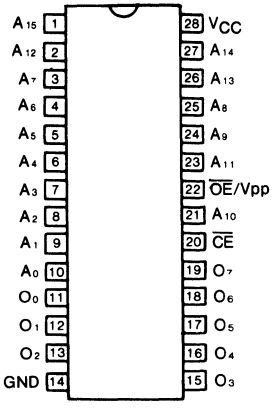
The MSM27512ZB is a 65536 words × 8-bit electrically programmable read-only memory. The MSM27512ZB is manufactured by the N channel double silicon gate MOS technology and is contained in the 28 pin package.
(OKI can provide programming service as per customer's request.)

FEATURES

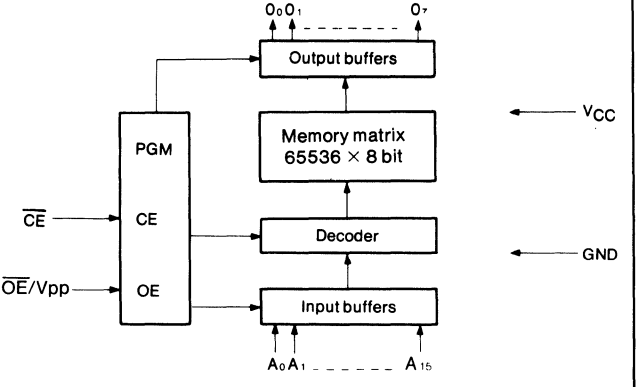
- +5V single power supply
- 65536 words × 8-bit configuration
- Access time: MAX200 ns
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (3-state output)
- 28-pin DIP

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$/Vpp (22)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	High impedance
Stand-by	V_{IH}	–	+5V	High impedance
Program	V_{IL}	12.5V	+6V	D_{IN}
Program Inhibit	V_{IH}	12.5V	+6V	High impedance

—; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}	−0.6V ~ 13.5V
	V_{OUT}	−0.6V ~ 7V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Unit
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5%	V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

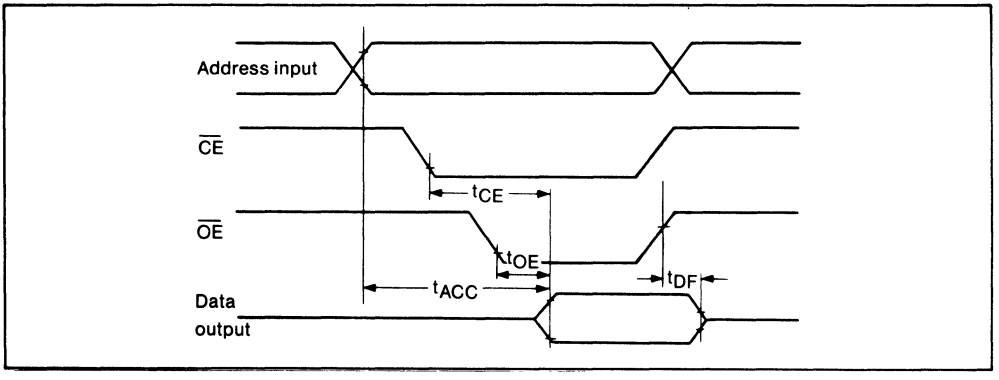
AC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	200	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	200	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	70	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	55	ns

7

TIME CHART



Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE}$ = V_{IL}	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

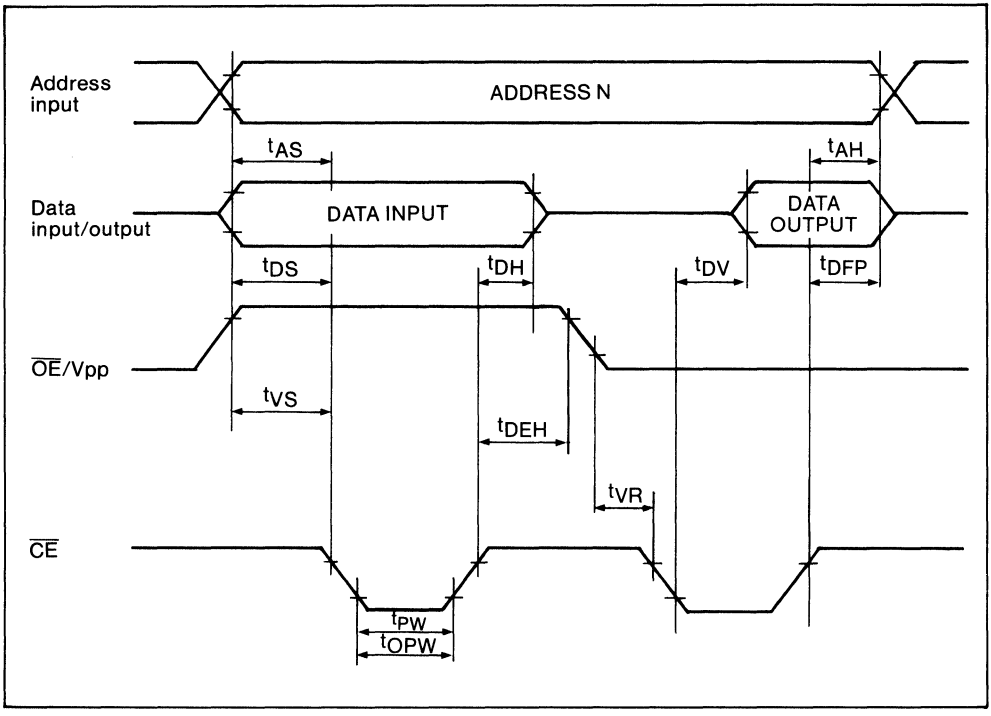
AC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$/Vpp Hold Time	t_{DEH}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	V_{CC} = 6V ± 0.25V	0.95	1.0	1.05	ms
$\overline{CE}$ High Speed Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25V ± 0.25V	95	100	105	μs
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	V_{CC} = 6V ± 0.25V	2.85	–	78.75	ms
Data Valid from $\overline{CE}$	t_{DV}	–	–	–	1	μs
$\overline{OE}$/Vpp Recovery Time	t_{VR}	–	2	–	–	μs

7

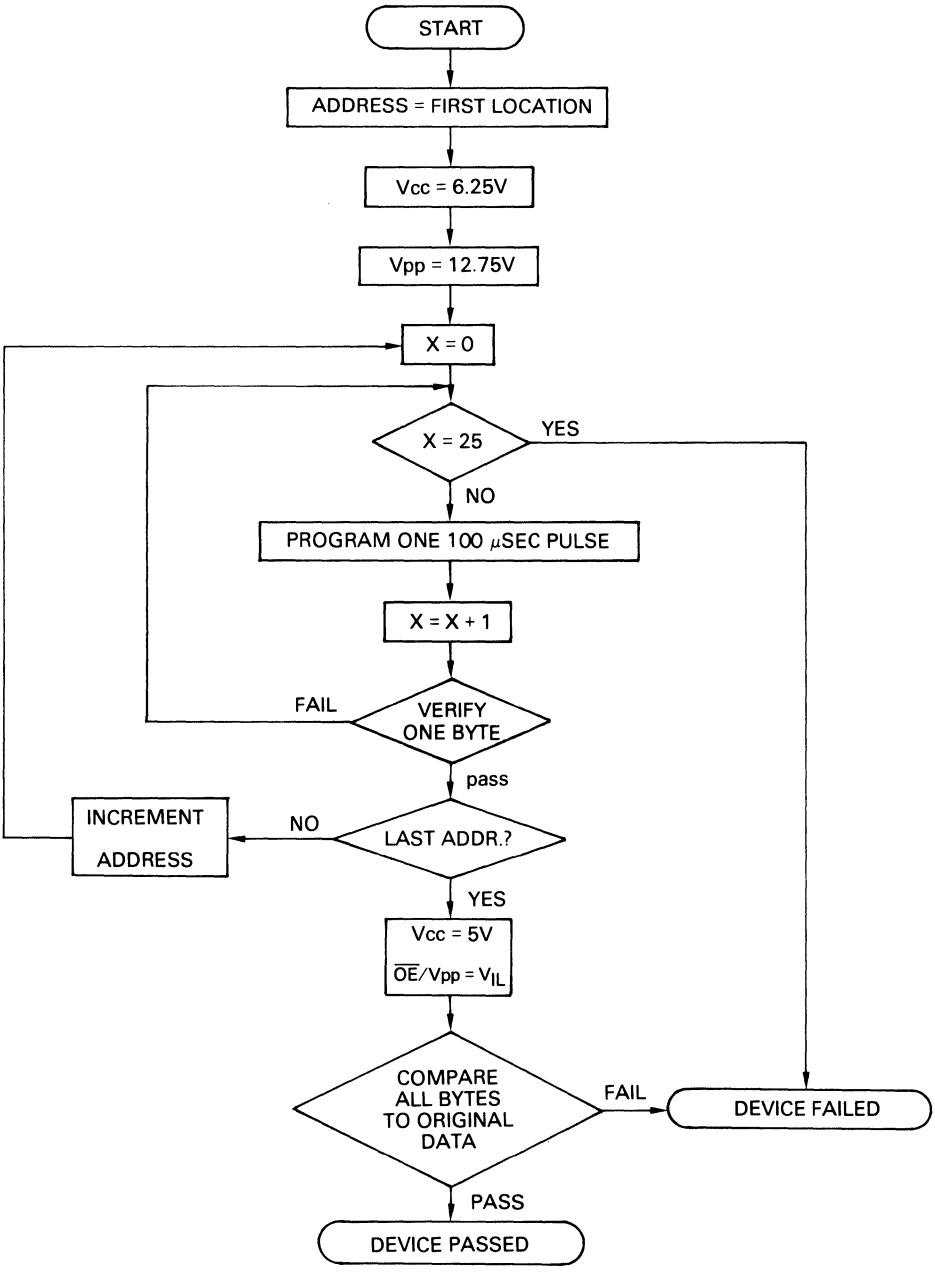
TIME CHART



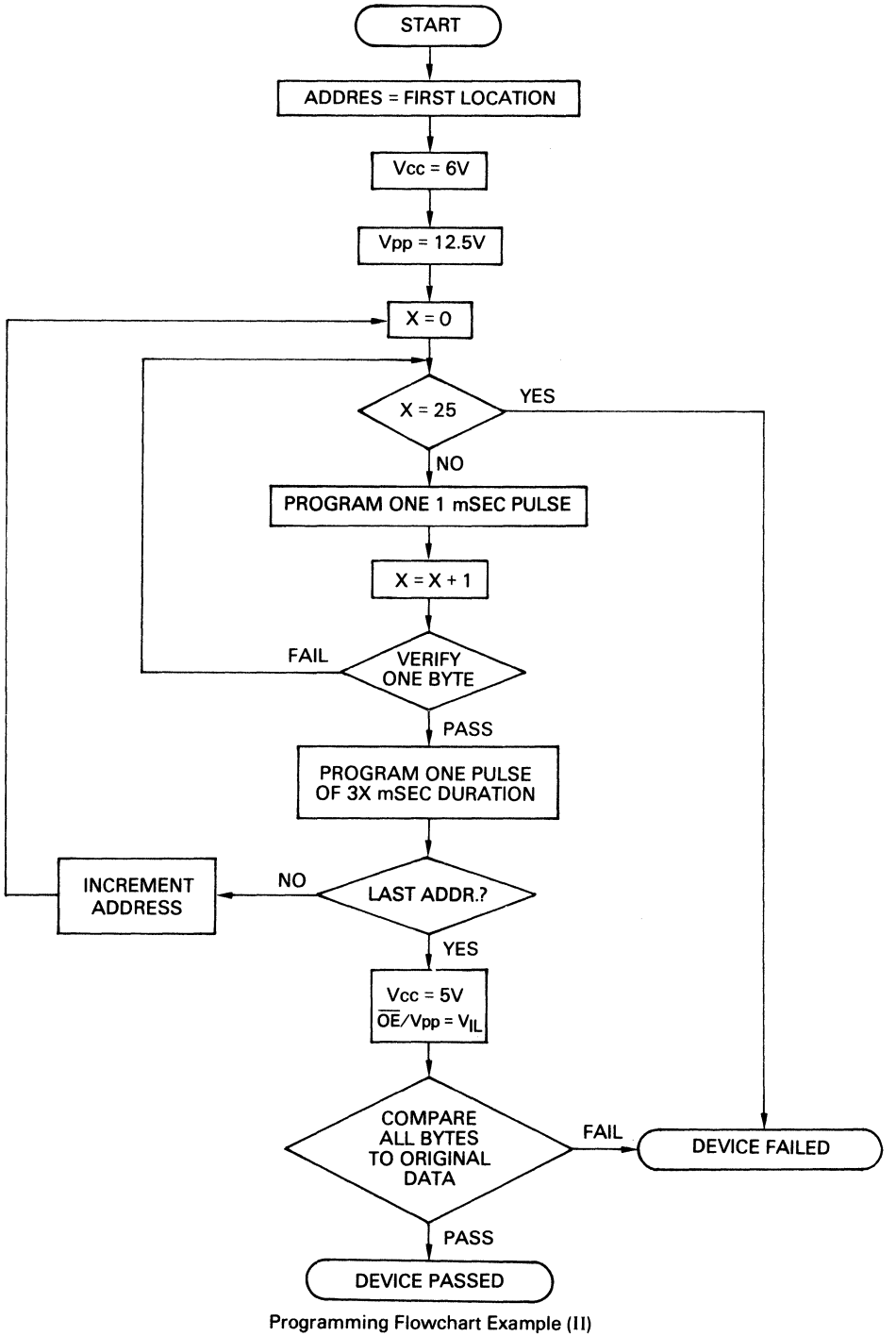
7

CAPACITANCE
(Ta = 25°C, f = 1 MHz, Vcc = 5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	4	6	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	8	12	pF



Programming Flowchart Example (I)



Programming Flowchart Example (II)

MSM271000ZB

131072 × 8-BIT ONE TIME PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

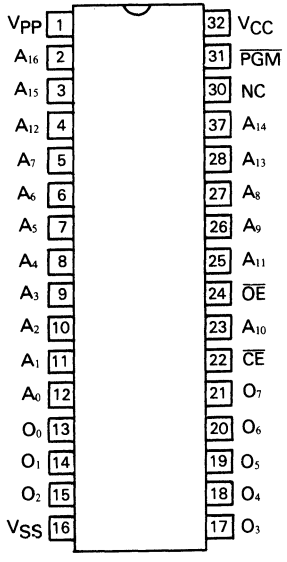
The MSM271000ZB is a 131072 words x 8 bit electrically programmable read-only memory. The MSM271000ZB is manufactured by N channel double silicon gate MOS technology and is contained in the 32 pin package.
(OKI can provide programming service as per customer's request.)

FEATURES

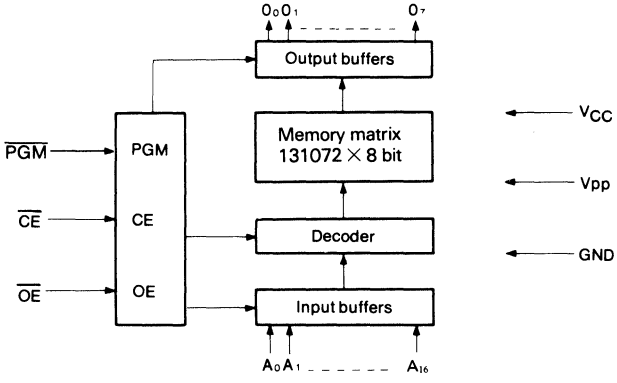
- +5V single power supply
- 131072 words × 8-bit configuration
- Access time: MAX200 ns
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (3-state output)
- 32-pin DIP

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (22)	$\overline{OE}$ (24)	$\overline{PGM}$ (31)	VPP (1)	VCC (32)	Outputs
Read	V_{IL}	V_{IL}	—	—	+5V	D_{OUT}
Output Disable	V_{IL}	V_{IH}	—	—	+5V	High impedance
Stand-by	V_{IH}	—	—	—	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.75V	+6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.75V	+6.25V	D_{OUT}
Program Inhibit	V_{IH}	—	—	+12.75V	+6.25V	High impedance

NOTES:
—; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input/Output Voltages	V_{IN}	−0.6V ~ 13.5V
	V_{OUT}	−0.6V ~ 7V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

7

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5%	V
V_{pp} Voltage	V_{pp}	−0.1	—	V_{cc}+1			V
"H" Level Input Voltage	V_{IH}	2.0	—	6.25			V
"L" Level Input Voltage	V_{IL}	−0.1	—	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

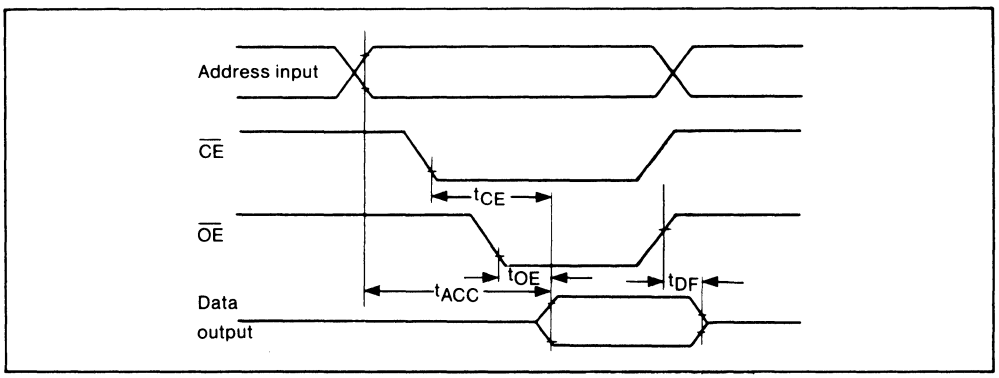
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{IH}	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	100	mA
Program Power Current	I_{PP1}	V_{PP}=V_{CC}	–	–	10	μA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	200	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	200	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	70	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	55	ns

TIME CHART



Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

7

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V ±0.25V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

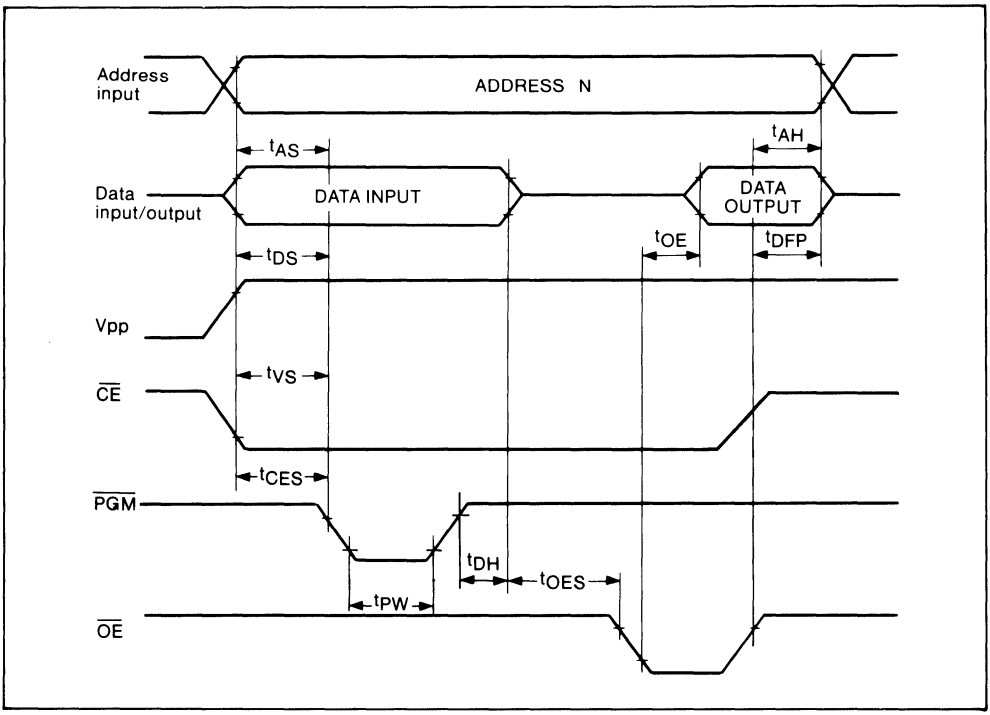
AC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V ±0.25V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
High Speed Initial Program Pulse Width	t_{PW}	–	95	100	105	μs
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

7

TIME CHART



CAPACITANCE

(Ta = 25°C, f = 1 MHz, Vcc = 5V)

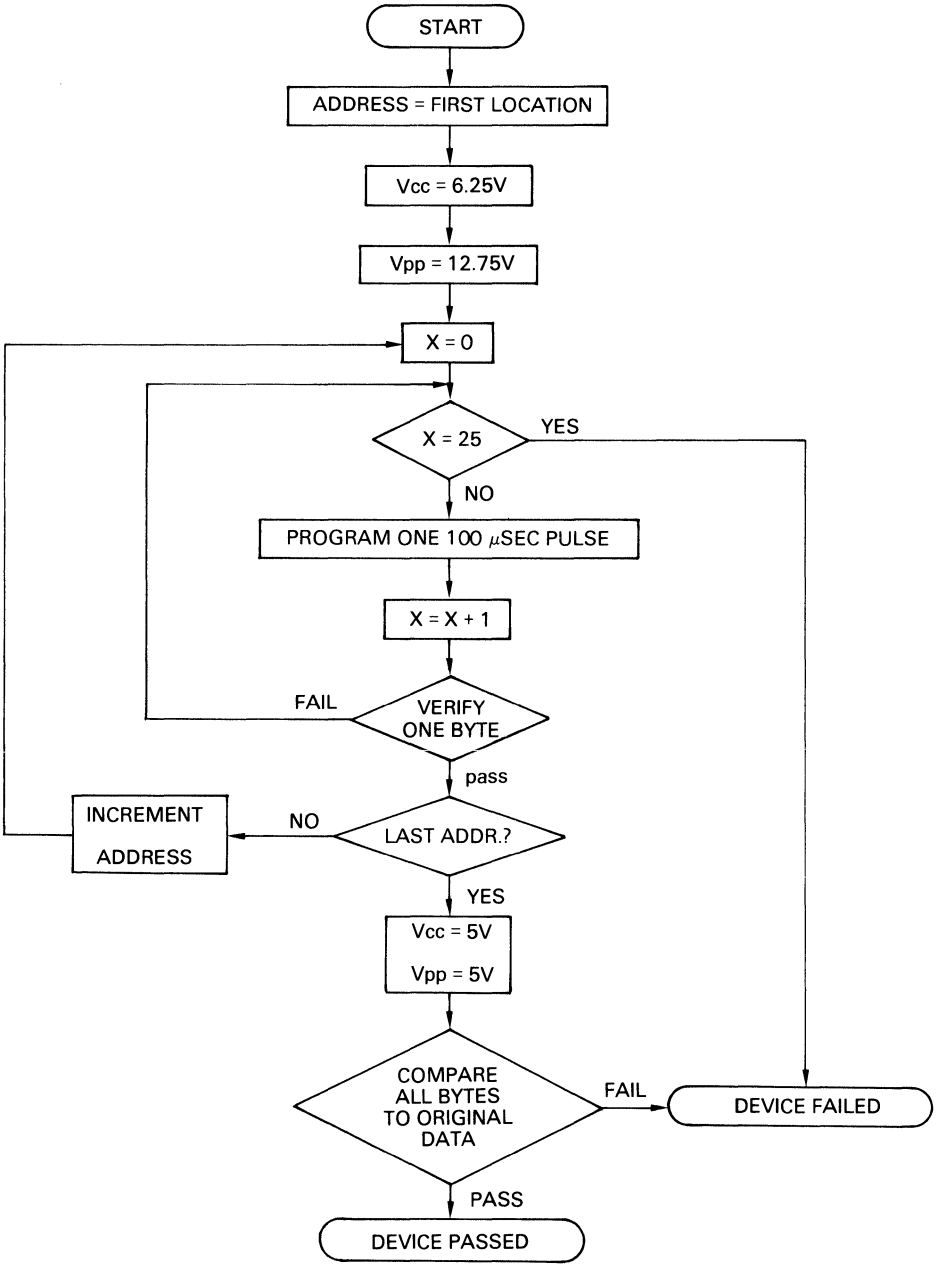
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	–	15	pF

MSM271000ZB-RS **IDENTIFIER BYTES**

Pins / Code	A_0 (12)	D_7 (21)	D_6 (20)	D_5 (19)	D_4 (18)	D_3 (17)	D_2 (15)	D_1 (14)	D_0 (13)	Hex Data
Manufacter Code	V_{IL}	1	0	1	0	1	1	1	0	AE
Device Code	V_{IH}	1	0	0	0	0	1	0	1	85

Notes: 1. $A_9 = 12.0 \pm 0.5V$

2. $A_1 \sim A_8$, $A_{10} \sim A_{16}$, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$ OR V_{IL}, $Vpp = V_{IH}$ OR V_{IL}



Programming Flowchart Example (I)

Preliminary

OKI semiconductor

MSM271024ZB

65536 × 16 BIT ONE TIME PROGRAMMABLE READ-ONLY MEMORY

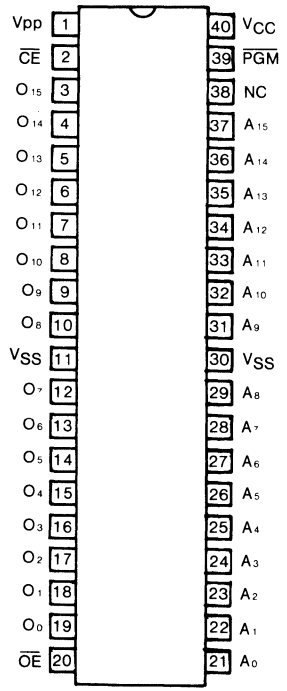
GENERAL DESCRIPTION

The MSM271024ZB is a 65536 words x 16 bit electrically programmable read-only memory. The MSM271024ZB is manufactured by the N channel double silicon gate MOS technology and is contained in the 40 pin package.
(OKI can provide programming service as per customer's request.)

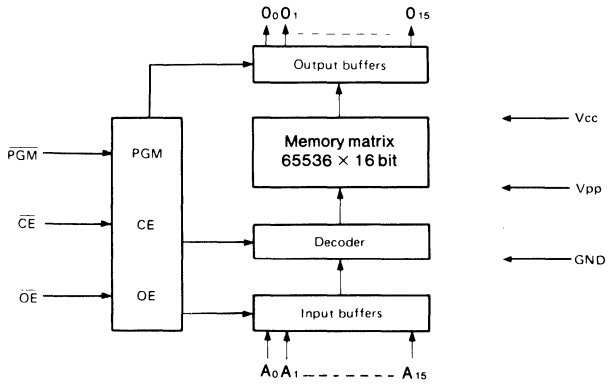
FEATURES

- +5V single power supply
- 65536 words × 16 bit configuration
- Access time:
  MAX170 ns
- Power consumption:
  MAX630 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation operation
- INPUT/OUTPUT TTL compatible (three state output)
- 40-pin DIP

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification

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FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (2)	$\overline{OE}$ (20)	$\overline{PGM}$ (39)	Vpp (1)	V_{CC} (40)	Outputs
Read	V_{IL}	V_{IL}	–	–	+5V	Dout
Output Disable	V_{IL}	V_{IH}	–	–	+5V	High impedance
Stand-by	V_{IH}	–	–	–	+5V	High impedance
Program	V_{IL}	V_{IH}	V_{IL}	+12.75V	+6.25V	D_{IN}
Program Verify	V_{IL}	V_{IL}	V_{IH}	+12.75V	+6.25V	Dout
Program Inhibit	V_{IH}	–	–	+12.75V	+6.25V	High impedance

–; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	–55°C ~ 125°C
All Input/Output Voltages	V_{IN}	–0.6V ~ 13.5V
	V_{OUT}	–0.6V ~ 7V
V_{CC} Supply Voltage	V_{CC}	–0.6V ~ 7V
Program Voltage	Vpp	–0.6V ~ 14V

The voltage with respect to GND.

7

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Symbol
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±0.25V	V
Vpp Voltage	Vpp	–0.1V	–	V_{CC} +1			V
"H" Level Input Voltage	V_{IH}	2.00	–	6.25			V
"L" Level Input Voltage	V_{IL}	–0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE} = V_{IH}$	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE} = V_{IL}$	–	–	120	mA
Program Power Current	I_{PP1}	$V_{PP}=V_{CC}$	–	–	10	μA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±5%, Ta = 0°C ~ 70°C)

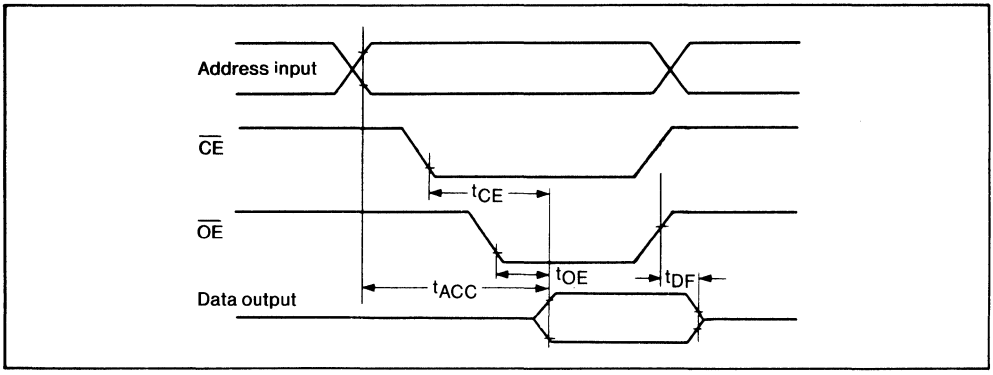
Parameter	Symbol	Conditions	Min.	Max.	Unit
Address Access Time	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$,	–	170	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE} = V_{IL}$,	–	170	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE} = V_{IL}$,	–	60	ns
Output Disable Time	t_{DF}	$\overline{CE} = V_{IL}$,	0	50	ns

Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

7

TIME CHART


Address input
$\overline{CE}$
$\overline{OE}$
Data output
t_{CE}
t_{OE}
t_{DF}
t_{ACC}

7

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V±0.25V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE} = \overline{PGM} = V_{IL}$	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	120	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+1	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 6.25V±0.25V, Vpp = 12.75V±0.25V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{PGM}$ Program Pulse Width	t_{PW}	V_{CC} =6.25V±0.25V	95	100	105	μs
$\overline{CE}$ Set-up Time	t_{CES}	–	2	–	–	μs
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

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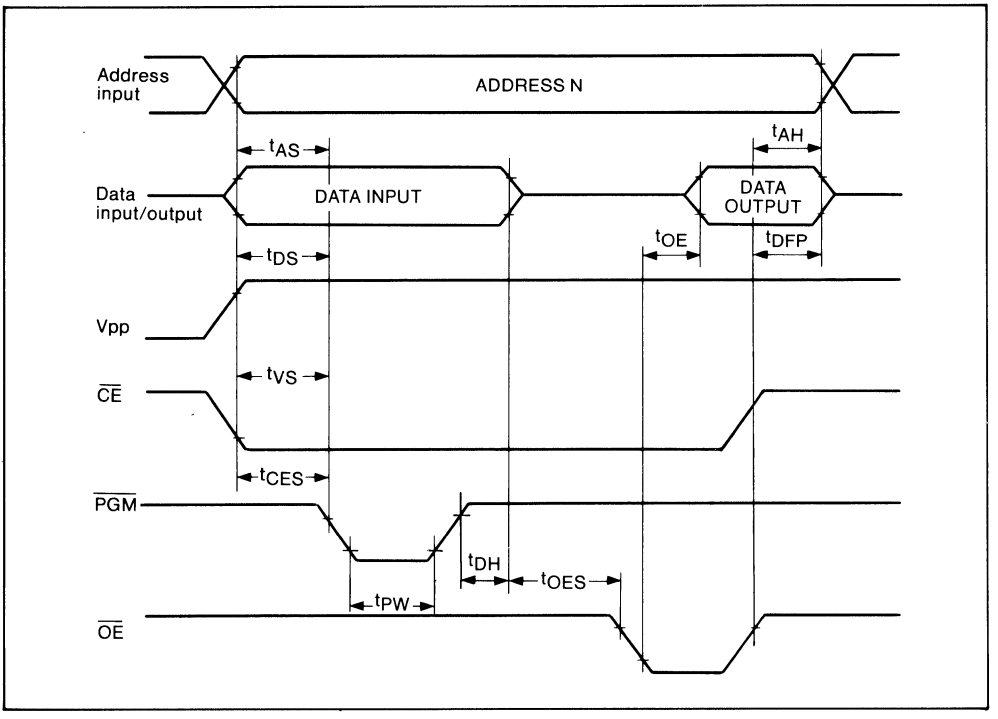
TIME CHART



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CAPACITANCE

(Ta = 25°C, f = 1 MHz, Vcc = 5V)

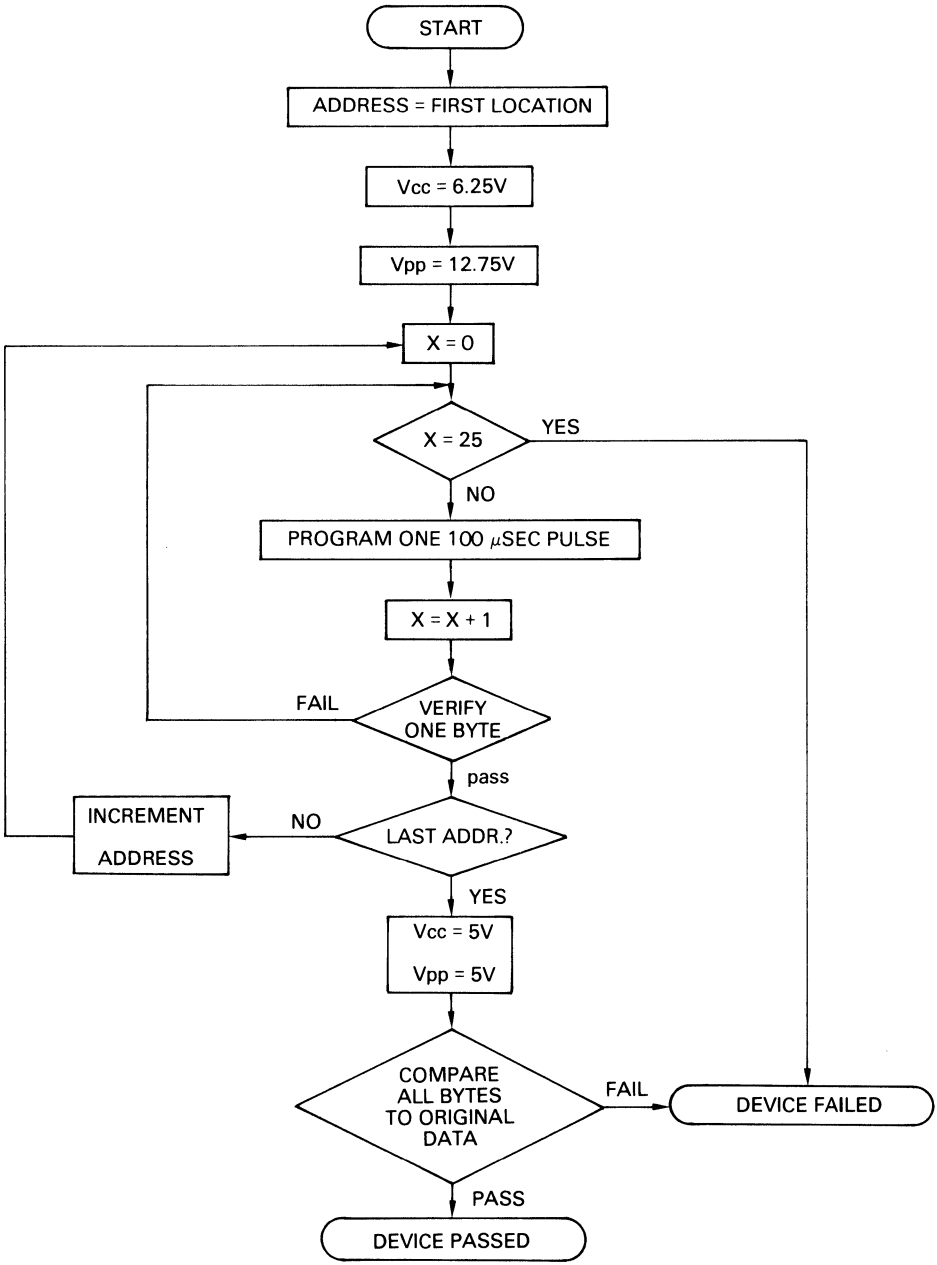
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	–	15	pF

MSM271024ZB-RS **IDENTIFIER BYTES**

Pins / Code	A_0 (21)	$D_{15} \sim D_8$ (3) ~ (10)	D_7 (12)	D_6 (13)	D_5 (14)	D_4 (15)	D_3 (16)	D_2 (17)	D_1 (18)	D_0 (19)	Hex Data
Manufacter Code	V_{IL}	0 ~ 0	1	0	1	0	1	1	1	0	00AE
Device Code	V_{IH}	0 ~ 0	1	0	0	0	0	1	1	0	0086

Notes: 1. $A_9 = 12.0 \pm 0.5V$

2. $A_1 \sim A_8$, $A_{10} \sim A_{15}$, $\overline{CE}$, $\overline{OE} = V_{IL}$, $\overline{PGM} = V_{IH}$ OR V_{IL}, $Vpp = V_{IH}$ OR V_{IL}



Programming Flowchart Example (I)

MSM27C256ZB

32,768 × 8-BIT ONE TIME PROGRAMMABLE READ-ONLY MEMORY

GENERAL DESCRIPTION

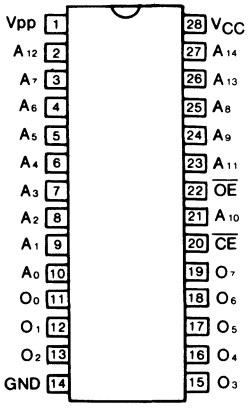
The MSM27C256ZB is a 32,768 words x 8 bit electrically programmable read-only memory. The MSM27C256ZB is manufactured by the CMOS double silicon gate technology and is contained in the 28 pin package.
(OKI can provide programming service as per customer's request.)

FEATURES

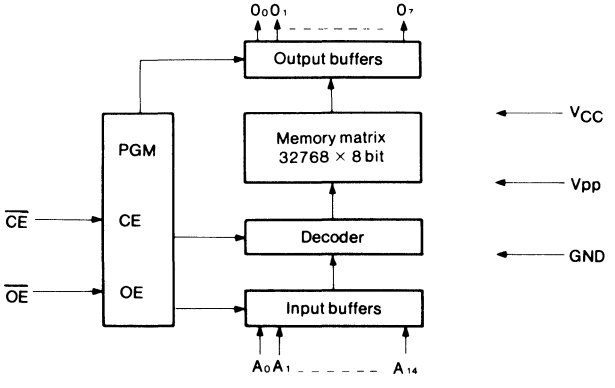
- +5V single power supply
- 32,768 words × 8-bit configuration
- Access time: MAX150 ns
- Power consumption:
  MAX165 mW (during operation)
  MAX0.55 mW (during stand-by)
- Completely static operation
- INPUT/OUTPUT TTL compatible (3-state output)
- 28-pin DIP

PIN CONFIGURATION

(Top View)



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	+12.5V	+6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	V_{IH}	+12.5V	+6V	High impedance

—; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input Voltage	V_{IN}	−0.6V ~ 13V
All Output Voltage	V_{OUT}	−0.6V ~ V_{CC} +0.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

7

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Unit
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.5	5.0	5.5	0°C ~ 70°C	V_{CC}=5V ±10% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.5	5.0	5.5			V
"H" Level Input Voltage	V_{IH}	2.0	–	V_{CC} +0.5			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.8			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±10%, Vpp = V_{CC}, Ta = 0°C±70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	1	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.5V	–	–	1	μA
V_{CC} Power Current (Stand-by)	I_{CC1}	$\overline{CE}$ = V_{CC}	–	–	100	μA
V_{CC} Power Current (Operation)	I_{CC2}	$\overline{CE}$ = V_{IL}	–	–	30	mA
Program Power Current	I_{PP1}	Vpp = V_{CC}	–	–	100	μA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC} +0.5	V
Input Voltage "L" Level	V_{IL}	–	-0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5V±10%, Vpp = V_{CC}, Ta = 0°C±70°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	150	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	150	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	60	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	50	ns

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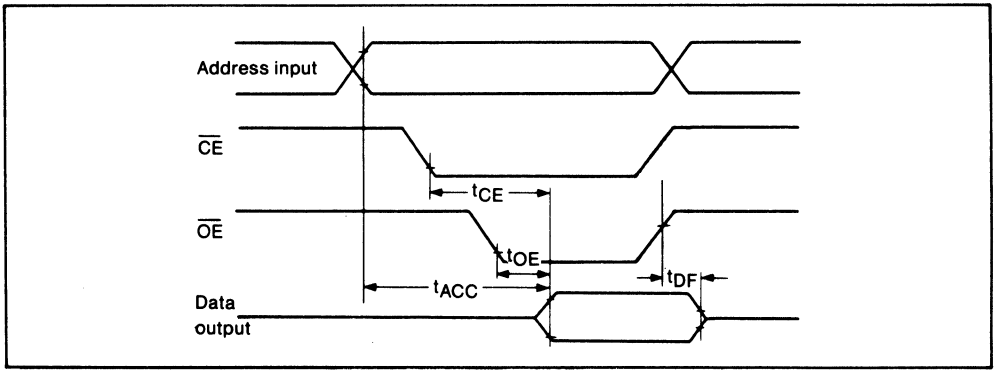
TIME CHART



Measurement condition

- Input pulse level ..... 0.45V and 2.4V
- Input timing reference level ..... 0.8V and 2.0V
- Output load ..... 1TTL GATE + 100pF
- Output timing reference level ..... 0.8V and 2.0V

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.5V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC} +0.5	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −400 μA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 2.1 mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	V_{CC} = 6V ± 0.25V	0.95	1.0	1.05	ms
$\overline{CE}$ High Speed Initial Program Pulse Width	t_{PW}	V_{CC} = 6.25V ± 0.25V	95	100	105	μs
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	V_{CC} = 6V ± 0.25V	2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

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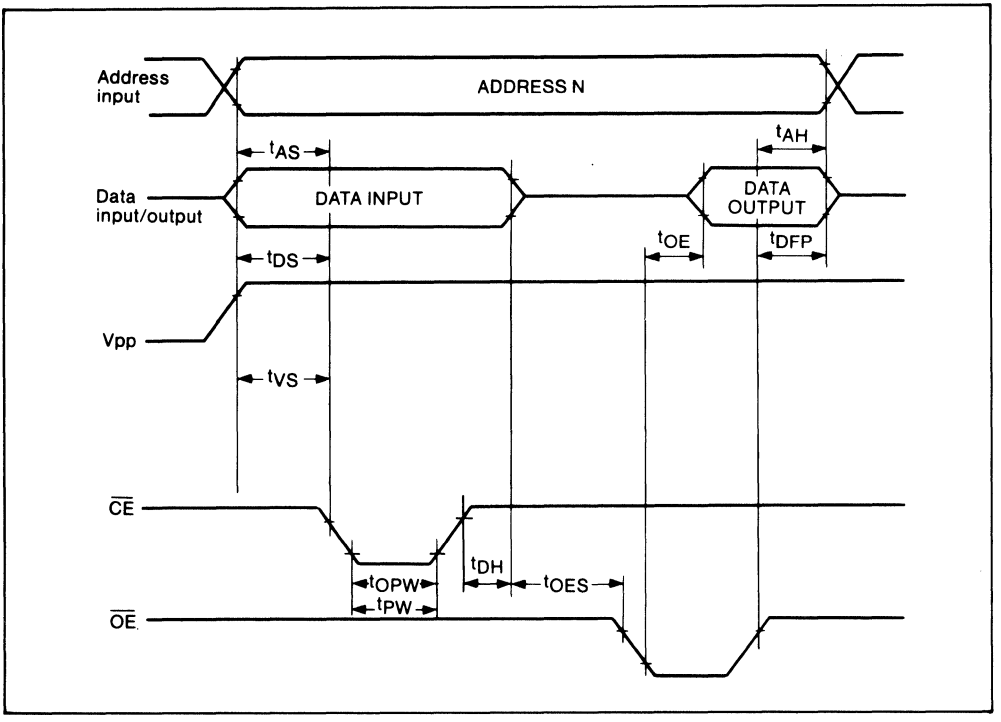
TIME CHART



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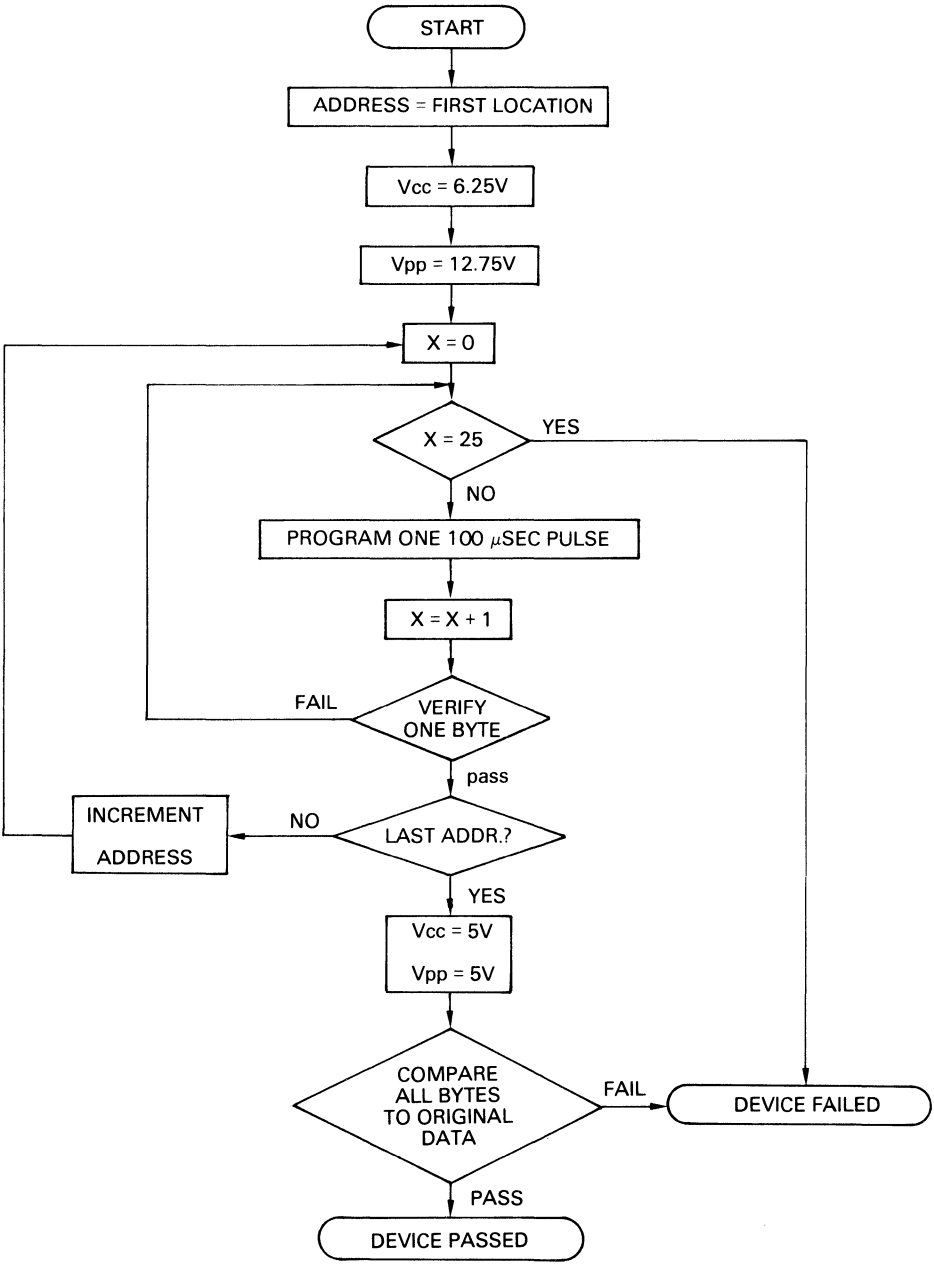
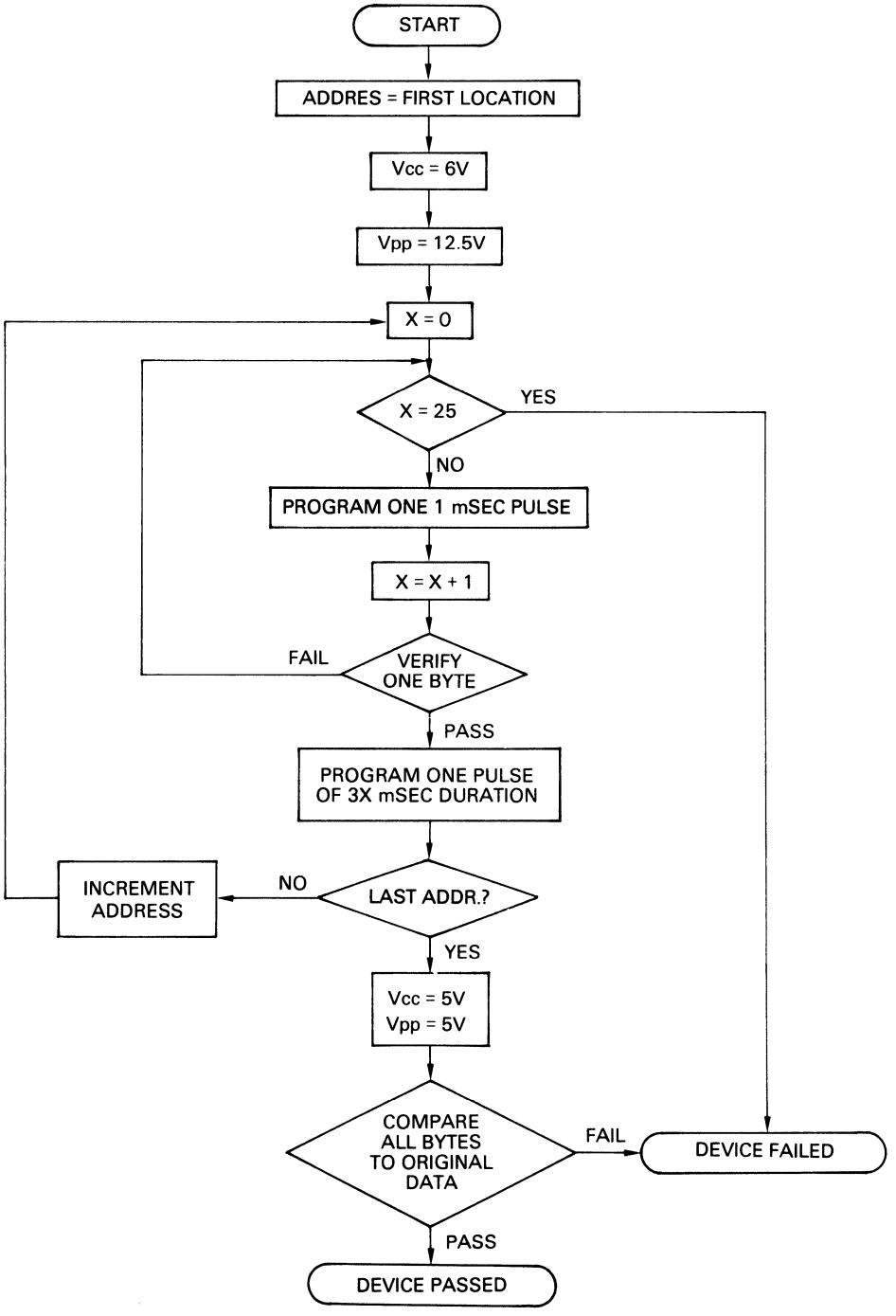
CAPACITANCE

(Ta = 25°C, f = 1 MHz, Vcc = 5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	—	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	—	15	pF



Programming Flowchart Example (I)



Programming Flowchart Example (II)

MSM27C256HZB

32,768 × 8-BIT ONE TIME PROGRAMMABLE READ-ONLY MEMORY

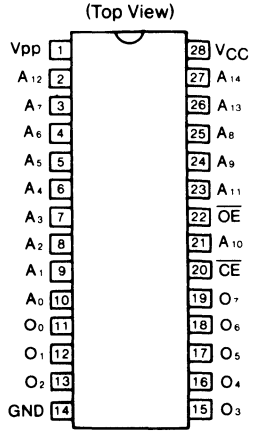
GENERAL DESCRIPTION

The MSM27C256HZB is a 32,768 words x 8 bit electrically programmable read-only memory. The MSM27C256HZB is manufactured by the CMOS double silicon gate technology and is contained in the 28 pin package.
(OKI can provide programming service as per customer's request.)

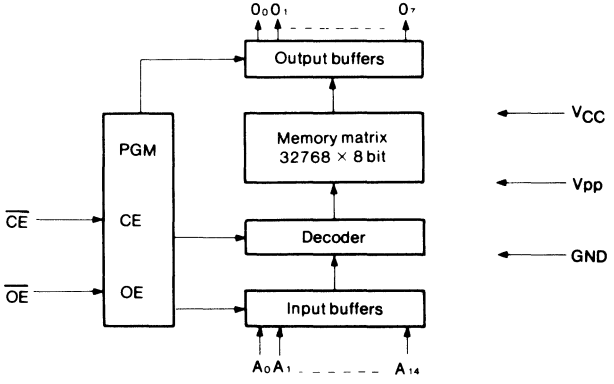
FEATURES

- +5V single power supply
- 32,768 words × 8-bit configuration
- Access time: MAX70 ns
- Power consumption:
  MAX525 mW (during operation)
  MAX184 mW (during stand-by)
- Completely static operation
- OUTPUT TTL compatible
  (3-state output)
- 28-pin DIP

PIN CONFIGURATION



FUNCTIONAL BLOCK DIAGRAM



This specification may be changed without notification.

7

FUNCTION TABLE

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	Vpp (1)	V_{CC} (28)	Outputs
Read	V_{IL}	V_{IL}	+5V	+5V	Dout
Output Disable	V_{IL}	V_{IH}	+5V	+5V	High impedance
Stand-by	V_{IH}	–	+5V	+5V	High impedance
Program	V_{IL}	V_{IH}	+12.5V	+6V	D_{IN}
Program Verify	V_{IH}	V_{IL}	+12.5V	+6V	Dout
Program Inhibit	V_{IH}	V_{IH}	+12.5V	+6V	High impedance

—; Can be either V_{IL} or V_{IH}

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	Ta	0°C ~ 70°C
Storage Temperature	Tstg	−55°C ~ 125°C
All Input Voltage	V_{IN}	−0.6V ~ 13.5V
All Output Voltage	V_{OUT}	−0.6V ~ V_{CC} +0.5V
V_{CC} Supply Voltage	V_{CC}	−0.6V ~ 7V
Program Voltage	Vpp	−0.6V ~ 14V

The voltage with respect to GND.

7

ELECTRICAL CHARACTERISTICS

<READ OPERATION>

RECOMMENDED OPERATION CONDITION

Parameter	Symbol	Limit			Operating Temperature	Remarks	Unit
		Min.	Typ.	Max.			
V_{CC} Power Supply Voltage	V_{CC}	4.75	5.0	5.25	0°C ~ 70°C	V_{CC}=5V±5% Vpp=V_{CC}	V
Vpp Voltage	Vpp	4.75	5.0	5.25			V
"H" Level Input Voltage	V_{IH}	3.0	–	V_{CC}+0.5			V
"L" Level Input Voltage	V_{IL}	−0.1	–	0.3			V

The voltage with respect to GND

DC CHARACTERISTICS

(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 5.25V	–	–	10	μA
V_{CC} Power Current (Stand-by)	I_{CC_1}	$\overline{CE}$ = V_{IH} f=10MHz	–	–	35	mA
V_{CC} Power Current (Operation)	I_{CC_2}	$\overline{CE}$ = V_{IL} f=10MHz	–	–	100	mA
Program Power Current	I_{PP_1}	Vpp = V_{CC}	–	–	5	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+0.5	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −4 mA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 8 mA	–	–	0.45	V

AC CHARACTERISTICS

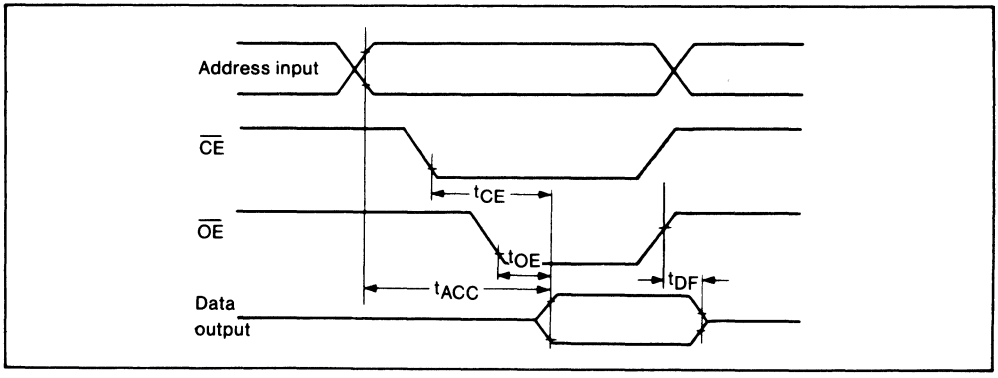
(V_{CC} = 5V±5%, Vpp = V_{CC}, Ta = 0°C ~ 70°C)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Address Access Time	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	–	70	ns
$\overline{CE}$ Access Time	t_{CE}	$\overline{OE}$ = V_{IL}	–	70	ns
$\overline{OE}$ Access Time	t_{OE}	$\overline{CE}$ = V_{IL}	–	30	ns
Output Disable Time	t_{DF}	$\overline{CE}$ = V_{IL}	0	25	ns

MEASUREMENT CONDITION

Input pulse level ..... 0V and 3.0V
Input timing reference level ..... 0.8V and 2.0V
Output load ..... 1TTL GATE + 30pF
Output timing reference level ..... 0.8V and 2.0V

TIME CHART



7

<PROGRAMMING OPERATION>

DC CHARACTERISTICS

(V_{CC} = 5.75~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

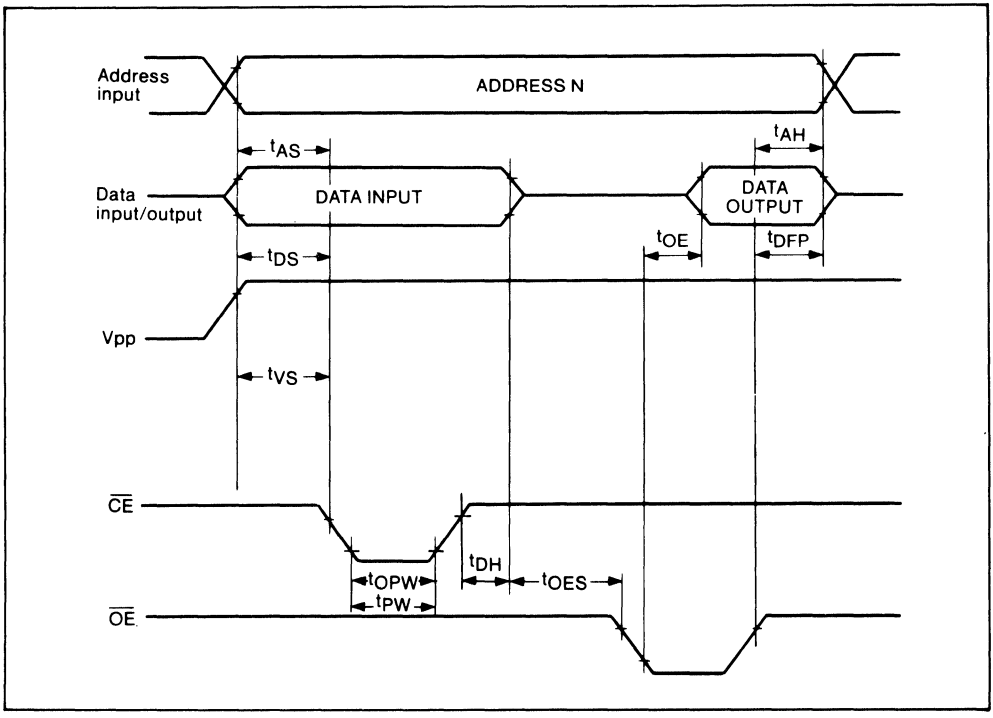
Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Input Leakage Current	I_{LI}	V_{IN} = 5.25V	–	–	10	μA
Vpp Power Current	I_{PP2}	$\overline{CE}$ = V_{IL}	–	–	50	mA
V_{CC} Power Current	I_{CC}	–	–	–	100	mA
Input Voltage "H" Level	V_{IH}	–	2.0	–	V_{CC}+0.5	V
Input Voltage "L" Level	V_{IL}	–	−0.1	–	0.8	V
Output Voltage "H" Level	V_{OH}	I_{OH} = −4mA	2.4	–	–	V
Output Voltage "L" Level	V_{OL}	I_{OL} = 8mA	–	–	0.45	V

AC CHARACTERISTICS

(V_{CC} = 5.75V~6.5V, Vpp = 12.5V±0.5V, Ta = 25°C±5°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Address Set-up Time	t_{AS}	–	2	–	–	μs
$\overline{OE}$ Set-up Time	t_{OES}	–	2	–	–	μs
Data Set-up Time	t_{DS}	–	2	–	–	μs
Address Hold Time	t_{AH}	–	0	–	–	μs
Data Hold Time	t_{DH}	–	2	–	–	μs
Output Enable to Output Float Delay	t_{DFP}	–	0	–	130	ns
Vpp Power Set-up Time	t_{VS}	–	2	–	–	μs
$\overline{CE}$ Initial Program Pulse Width	t_{PW}	V_{CC} = 6V ± 0.25V	0.95	1.0	1.05	ms
$\overline{CE}$ Program Pulse Width	t_{PW}	V_{CC} = 6.25V ± 0.25V	95	100	105	μs
$\overline{CE}$ Overprogram Pulse Width	t_{OPW}	V_{CC} = 6V ± 0.25V	2.85	–	78.75	ms
Data Valid from $\overline{OE}$	t_{OE}	–	–	–	150	ns

TIME CHART

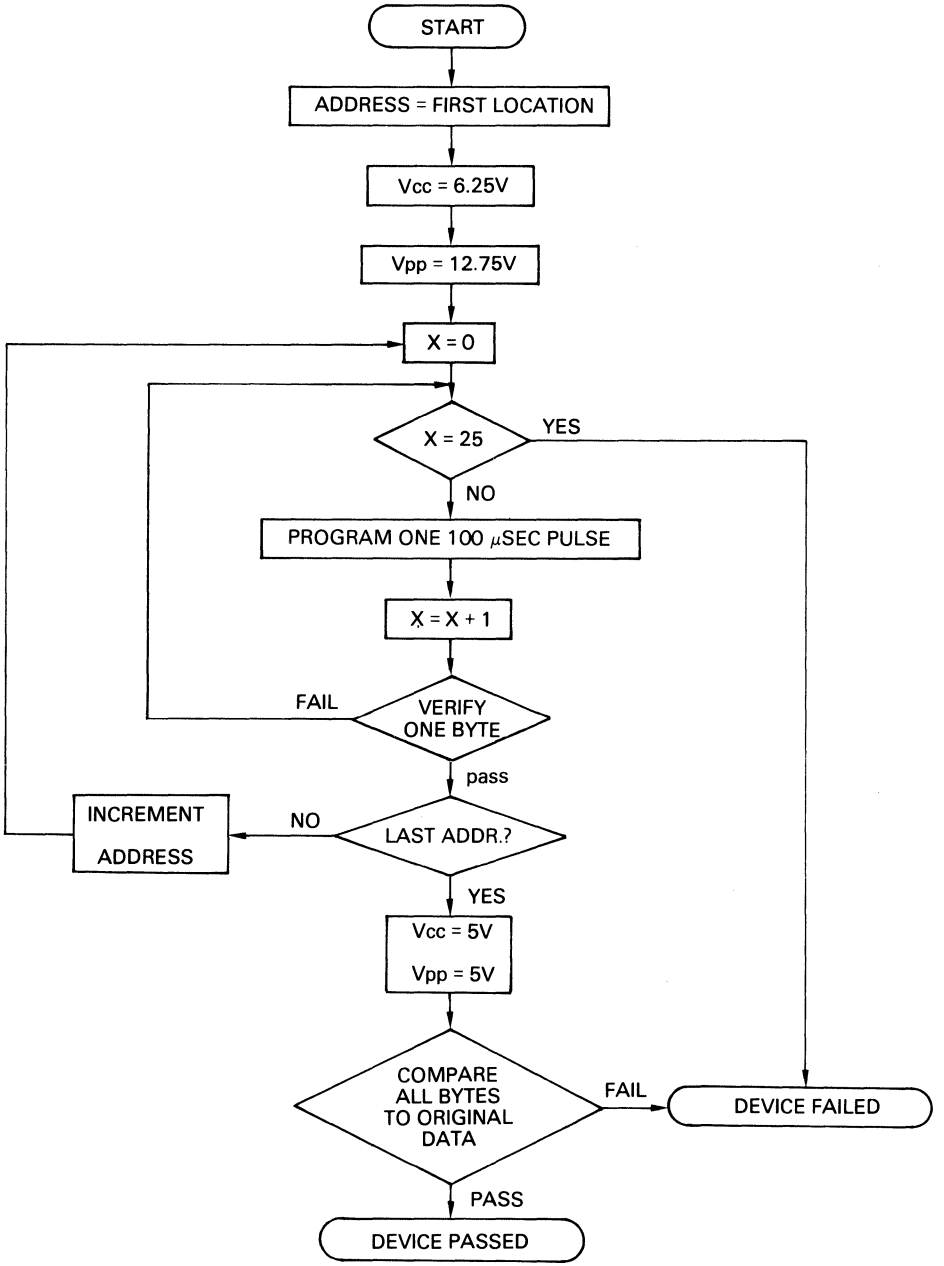


CAPACITANCE

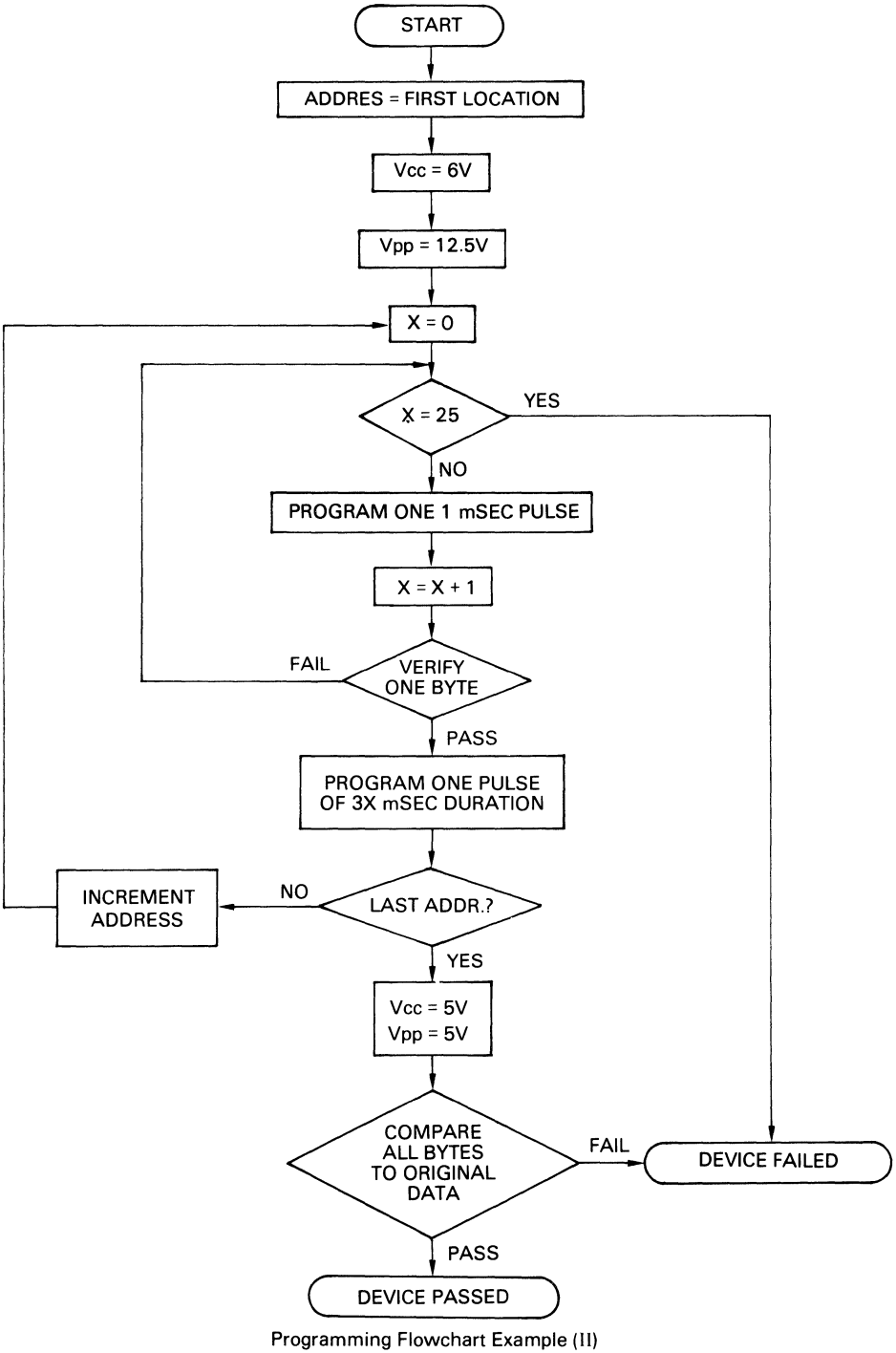
(Ta = 25°C, f = 1 MHz, Vcc = 5V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{IN}	V_{IN} = 0V	–	–	12	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0V	–	–	15	pF

7



Programming Flowchart Example (I)



Programming Flowchart Example (II)

7

MOS E^2 PROMS

8 MOS E^2 PROMS

MSM16811	1,024-Word x 1-Bit E^2 PROM	615
MSM16811P	1,024-Word x 1-Bit E^2 PROM	622
MSM16911	1,024-Word x 1-Bit E^2 PROM	629
MSM16911P	1,024-Word x 1-Bit E^2 PROM	638
MSM16812	2,048-Word x 1-Bit E^2 PROM	647
MSM16912	2,048-Word x 1-Bit E^2 PROM	654
MSM28C16A	2,048-Word x 8-Bits E^2 PROM	663
MSM28C64A	8,192-Word x 8-Bits E^2 PROM	670
MSM28C256	32k x 8-Bits CMOS E^2 PROM	678

MSM16811

1,024 BIT SERIAL E²PROM

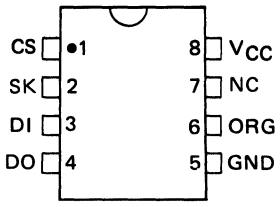
FEATURES:

- CMOS Floating Gate Technology
- Single +5-volt supply
- Eight pin plastic package
- 64 x 16 or 128 x 8 user selectable serial memory
- Compatible with NS9346
- Self timed programming cycle with Auto erase
- Word and chip erasable
- Operating Range 0°C to 70°C
- 10,000 erase/write cylces
- 10 year data retention

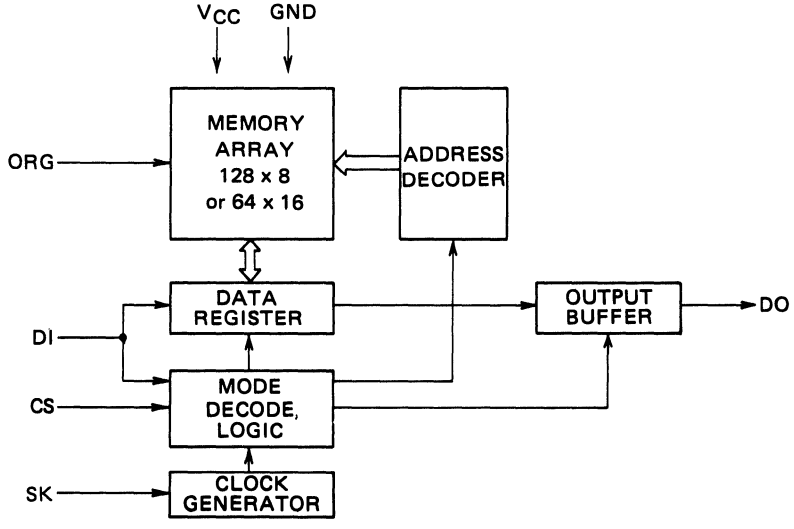
PIN CONFIGURATION

8 Pin Dual-In-Line
8 Pin S.O. Package

TOP VIEW



BLOCK DIAGRAM



8

PIN FUNCTIONS			
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 64 x 16 organization.
SK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5 V Power Supply		
NC	Non Connection		
GND	Ground		

			INSTRUCTION SET				
			Address		Data		
Instruction	Start Bit	Opcode	128 x 8	64 x 16	128 x 8	64 x 16	Comments
READ	1	1 0	A_6–A_0	A_5–A_0			Read Address A_N–A_0
ERASE	1	1 1	A_6–A_0	A_5–A_0			ERASE Address A_N–A_0
WRITE	1	0 1	A_6–A_0	A_5–A_0	D_7–D_0	D_{15}–D_0	WRITE Address A_N–A_0
EWEN	1	0 0	11XXXXX	11XXXX			Program Enable
EWDS	1	0 0	00XXXXX	00XXXX			Program Disable
ERAL	1	0 0	10XXXXX	10XXXX			Erase All Addresses
WRAL	1	0 0	01XXXXX	01XXXX	D_7–D_0	D_{15}–D_0	Program All Addresses

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

8

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25 °C	−0.3 ~ 7	V
Input Voltage	V_i		−0.3 ~ V_{CC} + 0.3	V
Output Voltage	V_o		−0.3 ~ V_{CC} + 0.3	V
Storage Temperature	T_{STG}		−55 ~ + 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Range	Unit
Supply Voltage	V_{CC}	5 ± 10%	V
Temperature Range	Ta	0 ~ 70	°C
Data Hold Temperature	Ta	0 ~ 70	°C

DC CHARACTERISTICS

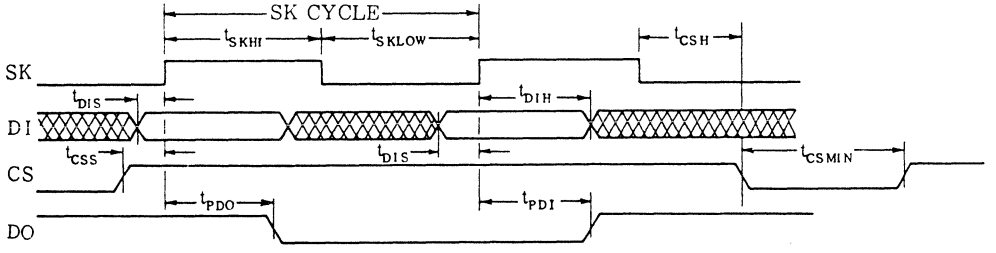
(V_{CC} = 4.5V to 5.5V, Ta = −0 ~ 70°C, unless otherwise specified.)

Parameter	Symbol	Condition	MIN	MAX	Unit
Supply Voltage	V_{CC}		4.5	5.5	V
Power Supply Current	I_{CC1}	V_{CC} = 5.5 V CS = 1		3	mA
	I_{CC2}	V_{CC} = 5.5 V CS = 0 DI = 0 or V_{CC}		100	μA
"L" Input Voltage	V_{IL}		−0.1	0.8	V
"H" Input Voltage	V_{IH}		2.0	V_{CC} + 1	V
"L" Output Voltage	V_{OL}	TTL I_{OL} = 2.1 mA		0.4	V
		CMOS I_{OL} = 100 μA		0.1	V
"H" Output Voltage	V_{OH}	TTL I_{OH} = −400 μA	2.4		V
		CMOS I_{OH} = −100 μA	V_{CC}−0.5		V
Input Leakage Current	I_{LI}	V_{in} = 5.5 V		10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.5 V CS = 0		10	μA

8

AC CHARACTERISTICS

Parameter	Description	Test Condition	Min	Typ	Max	Units
t_{CSS}	CS Setup Time		0.2			μs
t_{CSH}	CS Hold Time		0			μs
t_{DIS}	DI Setup Time		0.4			μs
t_{DIH}	DI Hold Time		0.4			μs
t_{PD1}	Output Delay to 1	CL = 100pF			2	μs
t_{PD0}	Output Delay to 0	V_{OL} = 0.8V, V_{OH} = 2.0			2	μs
t_{HZ}	Output Delay to HiZ	V_{IL} = 0.45V, V_{IH} = 2.4			0.4	μs
t_{EW}	Erase / Write Pulse Width				10	ms
t_{CSMIN}	Min CS Low Time		1			μs
t_{SKHI}	Min SK High Time		1			μs
t_{SKLOW}	Min SK Low Time		1			μs
t_{SV}	Output Delay to Status Valid	C_L = 100 pF			1	μs
SK_{MAX}	Maximum Frequency		0		250	kHz



Synchronous Timings

8

DEVICE OPERATION

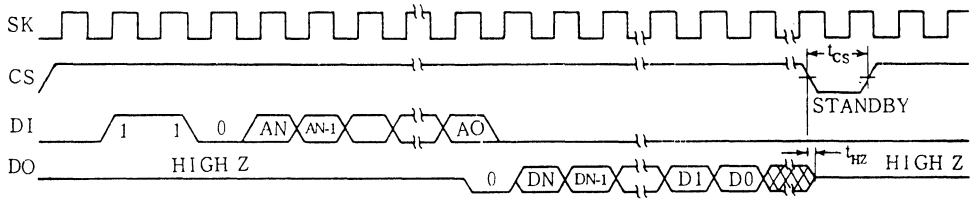
The MSM 16811 has 7 instructions that allow it to read, erase, or write. Each instruction consists of a start bit logical '1', an opcode field (2 bits or 4 bits) and an address field (6 or 7 bits).

The DO pin is a multiplexed pin. It is used as Data Out during the Read mode. It can also be used as a Ready Busy status indicator in programming mode. In all the other modes DO is tri-stated.

During power-up, all modes of operation are disabled and the device comes up in a program disabled state. An EWEN instruction has to be issued before starting to program.

At power-down, when V_{CC} falls below a level of approximately 3V, the data protection circuitry inhibits all modes of operation and an EWDS instruction is executed internally.

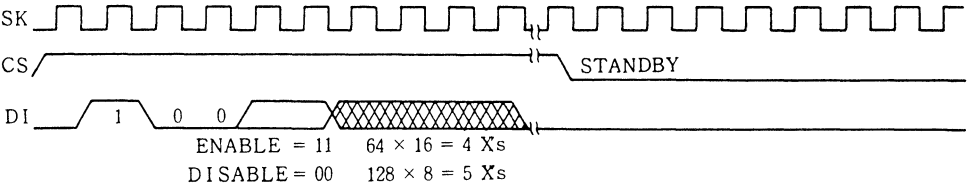
READ MODE



Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

The READ instruction reads the contents of the addressed register. It outputs data serially on the DO pin. After the instruction is decoded, a dummy bit (logical "0") precedes the output data string.

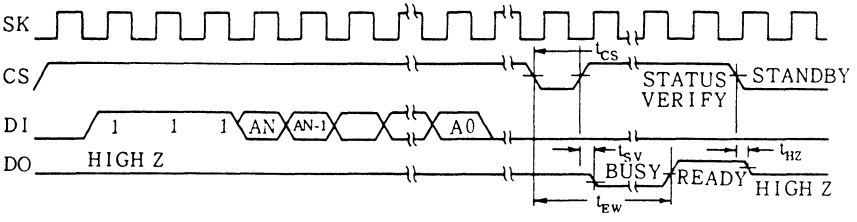
ERASE/WRITE ENABLE AND DISABLE



After power-up and before starting any programming instruction the EWEN instruction has to be issued. Once it has been issued, it will remain active until an EWDS instruction takes place. The EWDS instruction is provided to avoid any accidental programming of the part. The READ instruction is independent from the EWEN and EWDS instructions.

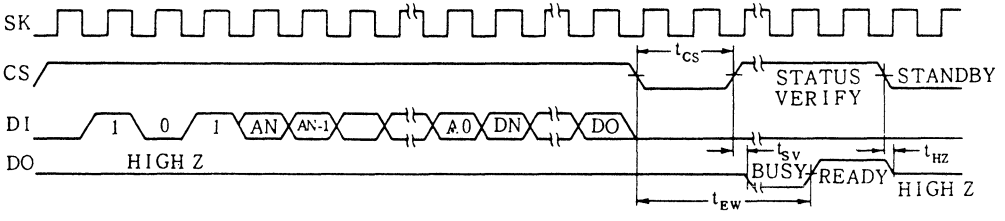
8

ERASE MODE



After an ERASE instruction has been shifted in. CS is dropped low. This will set the beginning of the self timed erase sequence. If CS is then brought high (after observing t_{CS} spec) the DO pin will act as a status indicator. It will remain low as long as the chip is programming. It will go high after all the bits of the addressed register have been set to a logical '1'.

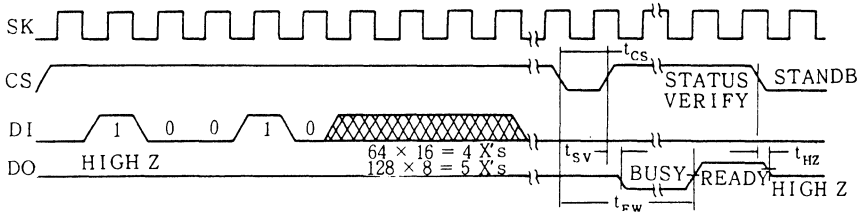
WRITE MODE



After a WRITE instruction has been shifted in with the corresponding 8 bits or 16 bits of data, CS is dropped low. This will set the beginning of the self timed programming sequence. If CS is brought high during the programming time (after observing the t_{CS} specification), the DO pin will act as a status indicator — it will remain low as long as the chip is programming. It will go high after all the bits of the addressed register have been set to their proper value. With the MSM16811 it is NOT neccessary to erase a memory location before the WRITE instruction.

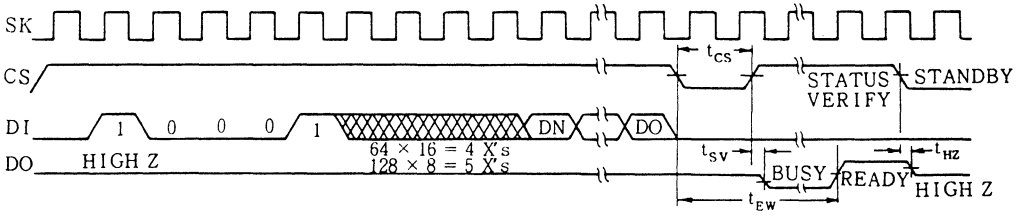
Configuration	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

ERASE ALL



This instruction is provided to erase the whole chip. Besides its different opcode, the ERAL instruction is identical to the ERASE instruction.

WRITE ALL



This instruction is provided to write simultaneously all the registers. All the registers must be erased before doing a WRAL operation. Besided its different opcode, the WRAL instruction is identical to the WRITE instruction.

8

OKI semiconductor

MSM16811P

1,024 BIT SERIAL E²PROM

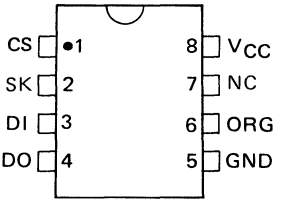
FEATURES:

- CMOS Floating Gate Technology
- Single +5-volt supply
- Eight pin plastic package
- 64 x 16 or 128 x 8 user selectable serial memory
- Compatible with NS9346
- Self timed programming cycle with Auto erase
- Word and chip erasable
- Operating Range −40°C to 85°C
- 10,000 erase/write cylces
- 10 year data retention

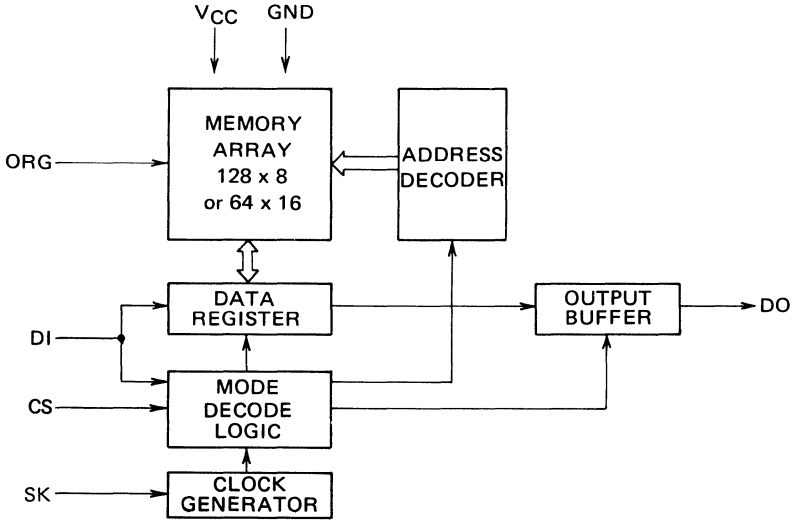
PIN CONFIGURATION

8 Pin Dual-In-Line
8 Pin S.O. Package

TOP VIEW



BLOCK DIAGRAM



8

PIN FUNCTIONS			
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 64 x 16 organization.
SK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5 V Power Supply		
NC	Non Connection		
GND	Ground		

			INSTRUCTION SET				
			Address		Data		
Instruction	Start Bit	Opcode	128 x 8	64 x 16	128 x 8	64 x 16	Comments
READ	1	1 0	A_6–A_0	A_5–A_0			Read Address A_N–A_0
ERASE	1	1 1	A_6–A_0	A_5–A_0			ERASE Address A_N–A_0
WRITE	1	0 1	A_6–A_0	A_5–A_0	D_7–D_0	D_{15}–D_0	WRITE Address A_N–A_0
EWEN	1	0 0	11XXXXX	11XXXX			Program Enable
EWDS	1	0 0	00XXXXX	00XXXX			Program Disable
ERAL	1	0 0	10XXXXX	10XXXX			Erase All Addresses
WRAL	1	0 0	01XXXXX	01XXXX	D_7–D_0	D_{15}–D_0	Program All Addresses

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

8

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25 °C	−0.3 ~ 7	V
Input Voltage	V_i		−0.3 ~ V_{CC} + 0.3	V
Output Voltage	V_o		−0.3 ~ V_{CC} + 0.3	V
Storage Temperature	T_{STG}		−55 ~ + 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Range	Unit
Supply Voltage	V_{CC}	5 ± 10 %	V
Temperature Range	Ta	−40 ~ 85	°C
Data Hold Temperature	Ta	−40 ~ 85	°C

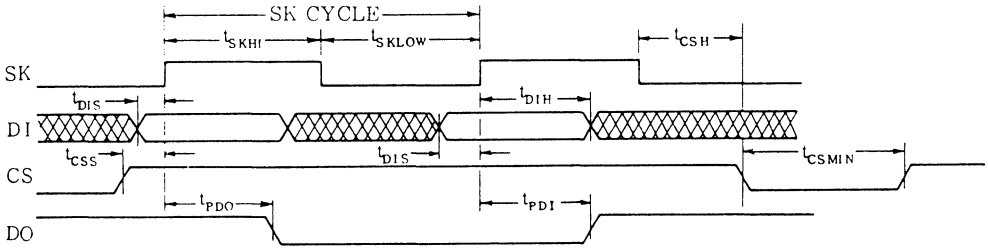
DC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Ta = −40 ~ 85°C, unless otherwise specified.)

Parameter	Symbol	Condition	MIN	MAX	Unit
Supply Voltage	V_{CC}		4.5	5.5	V
Power Supply Current	I_{CC1}	V_{CC} = 5.5 V CS = 1		5	mA
	I_{CC2}	V_{CC} = 5.5 V CS = 0 DI = 0 or V_{CC}		100	μA
"L" Input Voltage	V_{IL}		−0.1	0.8	V
"H" Input Voltage	V_{IH}		2.0	V_{CC} + 1	V
"L" Output Voltage	V_{OL}	TTL I_{OL} = 2.1 mA		0.4	V
		CMOS I_{OL} = 100 μA		0.1	V
"H" Output Voltage	V_{OH}	TTL I_{OH} = −400 μA	2.4		V
		CMOS I_{OH} = −40μA	V_{CC}−0.5		V
Input Leakage Current	I_{LI}	$0 \leqq V_{IN} \leqq V_{CC}$	−15	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.5 V CS = 0		10	μA

AC CHARACTERISTICS (Vcc = 4.5V to 5.5V, Ta = —40 ~ 85°C, unless otherwise specified)

Parameter	Description	Test Condition	Min	Typ	Max	Units
t_{CSS}	CS Setup Time		0.2			μs
t_{CSH}	CS Hold Time		0			μs
t_{DIS}	DI Setup Time		0.4			μs
t_{DIH}	DI Hold Time		0.4			μs
t_{PD1}	Output Delay to 1	CL = 100pF			2	μs
t_{PD0}	Output Delay to 0	V_{OL} = 0.8V, V_{OH} = 2.0			2	μs
t_{HZ}	Output Delay to HiZ	V_{IL} = 0.45V, V_{IH} = 2.4			0.4	μs
t_{EW}	Erase / Write Pulse Width				10	ms
t_{CSMIN}	Min CS Low Time		1			μs
t_{SKHI}	Min SK High Time		1			μs
t_{SKLOW}	Min SK Low Time		1			μs
t_{SV}	Output Delay to Status Valid	C_L = 100 pF			1	μs
SK_{MAX}	Maximum Frequency		0		250	kHz



Synchronous Timings

8

DEVICE OPERATION

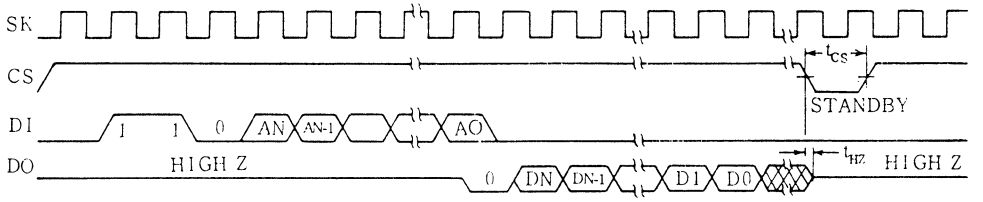
The MSM 16811 has 7 instructions that allow it to read, erase, or write. Each instruction consists of a start bit logical '1', an opcode field (2 bits or 4 bits) and an address field (6 or 7 bits).

The DO pin is a multiplexed pin. It is used as Data Out during the Read mode. It can also be used as a Ready Busy status indicator in programming mode. In all the other modes DO is tri-stated.

During power-up, all modes of operation are disabled and the device comes up in a program disabled state. An EWEN instruction has to be issued before starting to program.

At power-down, when V_{CC} falls below a level of approximately 3V, the data protection circuitry inhibits all modes of operation and an EWDS instruction is executed internally.

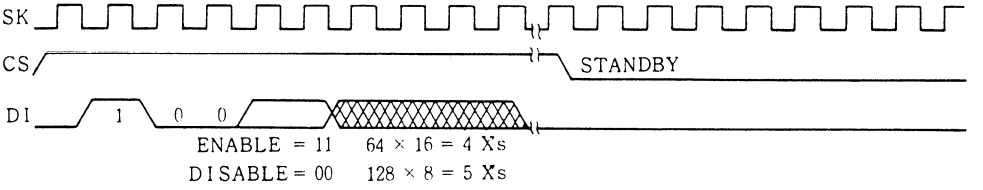
READ MODE



Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

The READ instruction reads the contents of the addressed register. It outputs data serially on the DO pin. After the instruction is decoded, a dummy bit (logical "0") precedes the output data string.

ERASE/WRITE ENABLE AND DISABLE



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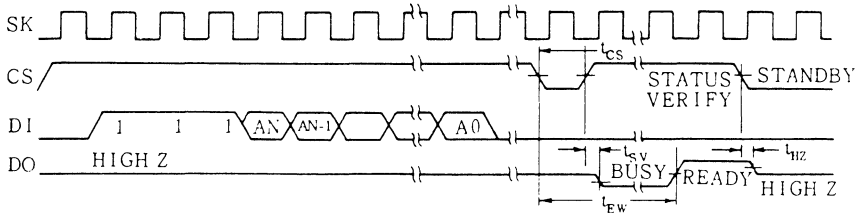
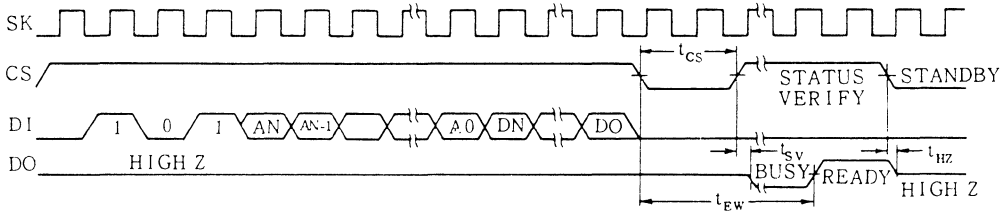
After power-up and before starting any programming instruction the EWEN instruction has to be issued. Once it has been issued, it will remain active until an EWDS instruction takes place. The EWDS instruction is provided to avoid any accidental programming of the part. The READ instruction is independent from the EWEN and EWDS instructions.

ERASE MODE



After an ERASE instruction has been shifted in. CS is dropped low. This will set the beginning of the self timed erase sequence. If CS is then brought high (after observing t_{CS} spec) the DO pin will act as a status indicator. It will remain low as long as the chip is programming. It will go high after all the bits of the addressed register have been set to a logical '1'.

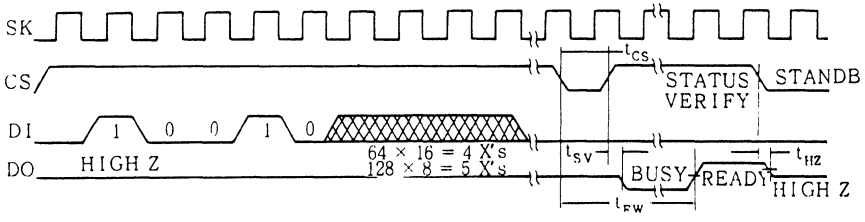
WRITE MODE



After a WRITE instruction has been shifted in with the corresponding 8 bits or 16 bits of data, CS is dropped low. This will set the beginning of the self timed programming sequence. The addressed register will first be erased and then the previously shifted data will be written in the register. If CS is brought high during the programming time (after observing the t_{CS} specification), the DO pin will act as a status indicator — it will remain low as long as the chip is programming. It will go high after all the bits of the addressed register have been set to their proper value.

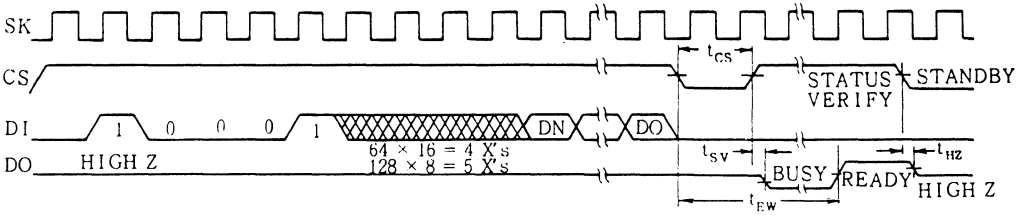
Configuration	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

ERASE ALL



This instruction is provided to erase the whole chip. Besides its different opcode, the ERAL instruction is identical to the ERASE instruction.

WRITE ALL



This instruction is provided to write simultaneously all the registers. All the registers must be erased before doing a WRAL operation. Besided its different opcode, the WRAL instruction is identical to the WRITE instruction.

8

OKI semiconductor

MSM16911

1,024 BIT SERIAL E²PROM

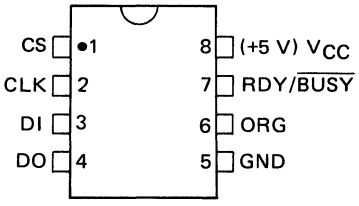
FEATURES:

- CMOS Floating Gate Technology
- Single +5-volt supply
- Eight pin plastic package
- 64 x 16 or 128 x 8 user selectable serial memory
- Compatible with GI5911
- Self timed programming cycle with Auto erase
- Word and chip erasable
- Operating Range 0° C to 70° C
- 10,000 erase/write cylces
- 10 year data retention

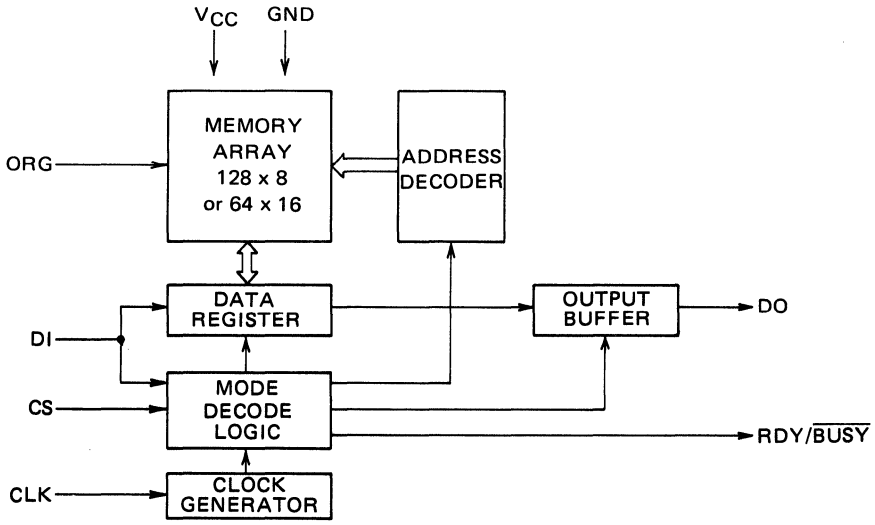
PIN CONFIGURATION

8 Pin Dual-In-Line
8 Pin S.O. Package

TOP VIEW



BLOCK DIAGRAM



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PIN FUNCTIONS			
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 64 x 16 organization.
CLK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5 V Power Supply		
RDY/$\overline{BUSY}$	Status Output		
GND	Ground		

			INSTRUCTION SET				
Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A_6-A_0	A_5-A_0			Read Address A_N-A_O
PROGRAM	1	x100	A_6-A_0	A_5-A_0	D_7-D_0	$D_{15}-D_0$	Program Address A_N-A_O
PEN	1	0011	0000000	000000			Program Enable
PDS	1	0000	0000000	000000			Program Disable
ERAL	1	0010	0000000	000000			Erase All Addresses
WRAL	1	0001	0000000	000000	D_7-D_0	$D_{15}-D_0$	Write All Addresses

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25 °C	−0.3 ~ 7	V
Input Voltage	V		−0.3 ~ V_{CC} + 0.3	V
Output Voltage	V_o		−0.3 ~ V_{CC} + 0.3	V
Storage Temperature	T_{STG}		−55 ~ + 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Range	Unit
Supply Voltage	V_{CC}	5 ± 10%	V
Temperature Range	Ta	0 ~ 70	°C
Data Hold Temperature	Ta	0 ~ 70	°C

DC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Ta = 0 ~ 70°C, unless otherwise specified.)

Parameter	Symbol	Condition	MIN	MAX	Unit
Supply Voltage	V_{CC}		4.5	5.5	V
Power Supply Current	I_{CC1}	V_{CC} = 5.5 V CS = 1		3	mA
	I_{CC2}	V_{CC} = 5.5 V CS = 0 DI = 0 or V_{CC}		100	μA
"L" Input Voltage	V_{IL}		−0.1	0.8	V
"H" Input Voltage	V_{IH}		2.0	V_{CC} + 1	V
"L" Output Voltage	V_{OL}	TTL I_{OL} = 2.1 mA		0.4	V
		CMOS I_{OL} = 100 μA		0.1	V
"H" Output Voltage	V_{OH}	TTL I_{OH} = −400 μA	2.4		V
		CMOS I_{OH} = −100 μA	V_{CC}−0.5		V
Input Leakage Current	I_{LI}	V_{in} = 5.5 V		10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.5 V CS = 0		10	μA

8

AC CHARACTERISTICS

(V_{CC} = 4.5 V to 5.5 V, Ta = 0 ~ 70°C, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{CLK}	CLK Frequency	0		250	kHz	
t_{CSS}	CS Setup Time with respect to CLK Falling	0.2			μs	
t_{CSH}	CS Hold Time with respect to CLK Rising	100			ns	
t_{DIS}	DI Setup Time with respect to CLK Rising	0.4			μs	
t_{DIH}	DI Hold Time with respect to CLK Rising	0.4			μs	
t_{CPH}	CLK Pulse High Time	1.0			μs	
t_{CPL}	CLK Pulse Low Time	1.0			μs	
t_{PD1}	Delay Time of DO Rising with respect to CLK Rising			2.0	μs	1
t_{PDO}	Delay Time of DO Falling with respect to CLK Rising			2.0	μs	1
t_P	"L" Time of Status (Programming Time)			10	ms	

Note 1: Condition: C_L = 100pF and V_{OL}/OH = 0.8/2.0

Figure 1. Synchronous Data Timing

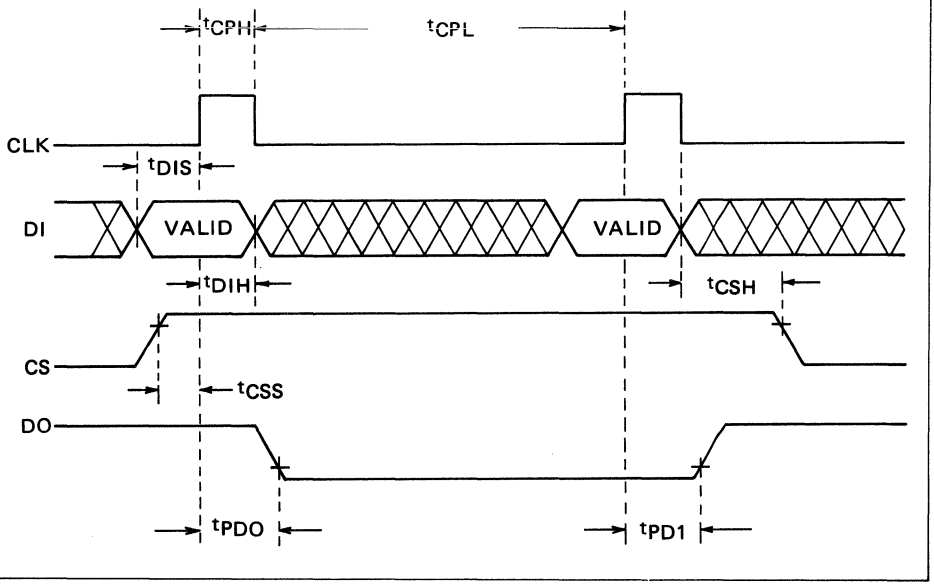

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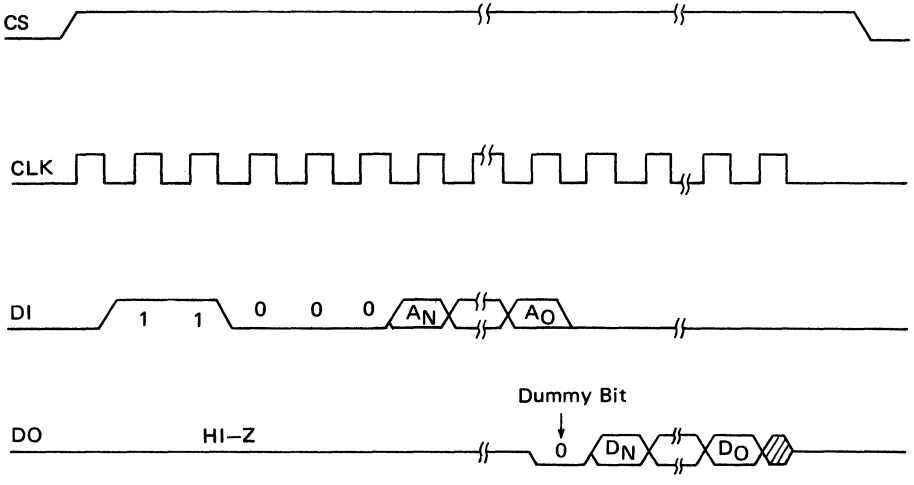
Figure 2. READ Mode



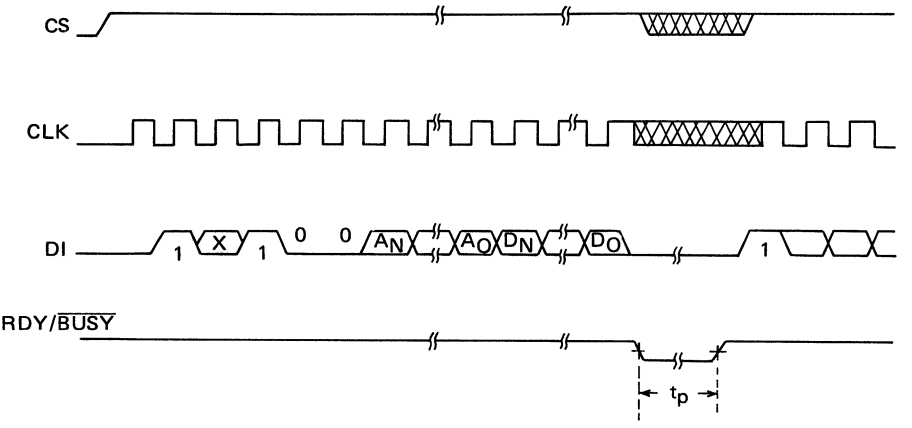
Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

Read Mode

The READ instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a serial-out shift register. A dummy bit (logical "0") procedes the data output string. The output data changes during the high states of the system clock.

8

Figure 3. PROGRAM Mode



Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

8

Program Mode

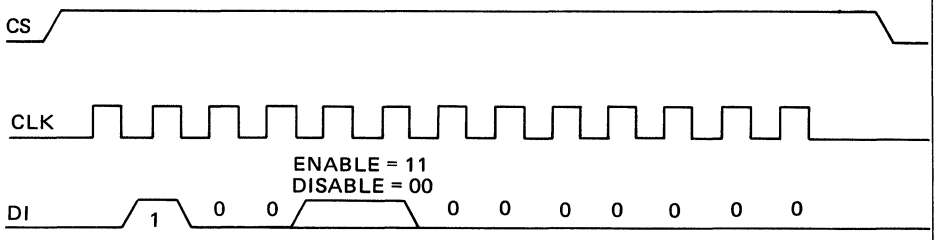
The program instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

After the last data bit (DO) has been shifted into the data register the contents of the specified address will be erased and the new data written to the same address.

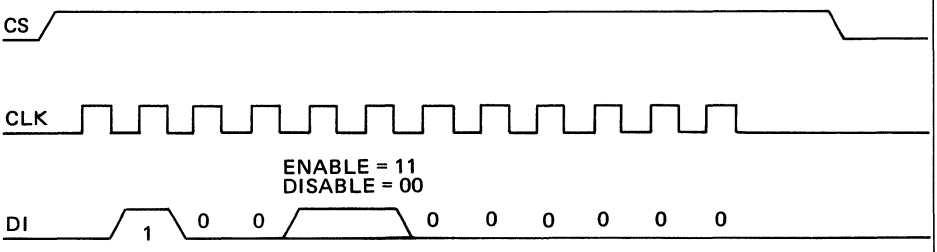
During the automatic erase/write sequence the RDY/$\overline{\text{BUSY}}$ output will go low for the duration of the automatic programming cycle as indicated by tp.

During a program cycle the internal erase and write operations occur automatically and are self-timed on the device. A single memory location may also be erased by programming that address with all "1's".

Figure 4. PEN (Program Enable) and PDS (Program Disable)



PEN AND PDS FOR 128 x 8 ORGANIZATION



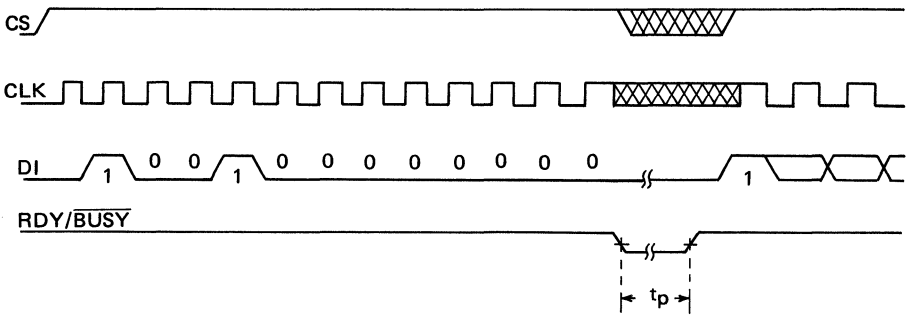
PEN AND PDS FOR 64 x 16 ORGANIZATION

Program Enable and Program Disable

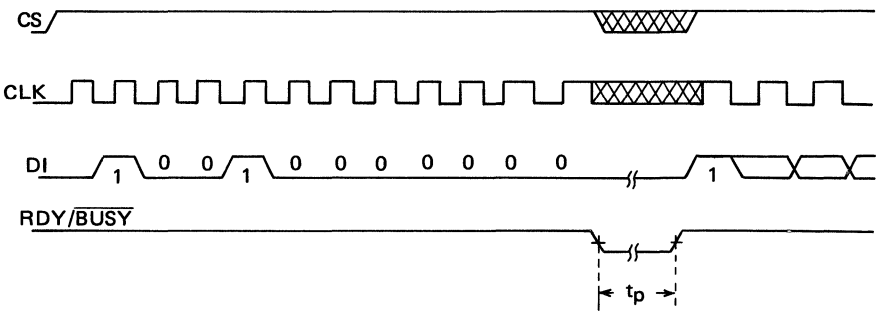
Programming must be preceded once by a programming enable (PEN) instruction. Programming remains enabled until a programming disable (PDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both PEN and PDS instructions.

8

Figure 5. ERAL (Erase All) Mode (128 x 8)



ERAL (Erase All) Mode (64 x 16)



Chip Erase

Entire chip erasing is provided for ease of programming and is implemented with the ERAL (erase all registers) instruction. Erasing the chip means that all registers in the memory array have each bit set to a "1".

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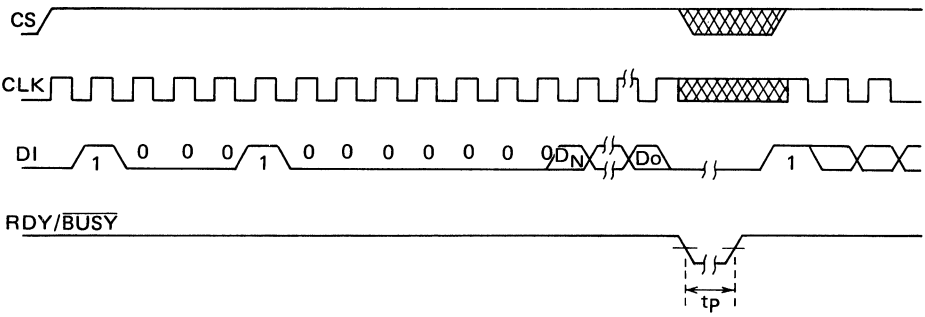
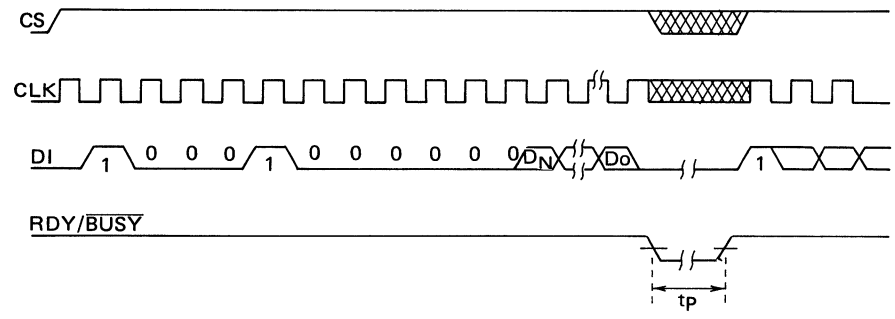
All specifications and details published are subject to change without notice.

Figure 6. WRITE ALL

WRAL (Write All) Mode (128 x 8)



WRAL (Write All) Mode (64 x 16)



	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

Write All

This instruction is provided to write simultaneously all the registers. All the registers must be erased before doing a WRAL operation. After a WRAL instruction has been shifted in, the RDY/BUSY pin goes low and the self timed write sequence starts. The RDY/BUSY pin will act as a status indicator. It will remain low as long as the chip is programming. It will go high after all the bits of the array have been set to their proper value.

8

OKI semiconductor

MSM16911P

1,024 BIT SERIAL E²PROM

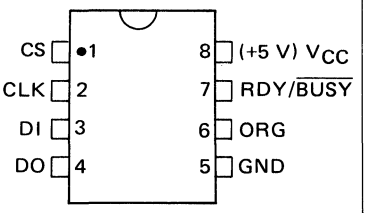
FEATURES:

- CMOS Floating Gate Technology
- Single +5-volt supply
- Eight pin plastic package
- 64 x 16 or 128 x 8 user selectable serial memory
- Compatible with GI5911
- Self timed programming cycle with auto erase
- Word and chip erasable
- Operating Range −40°C ~ 85°C
- 10,000 erase/write cylces
- 10 year data retention

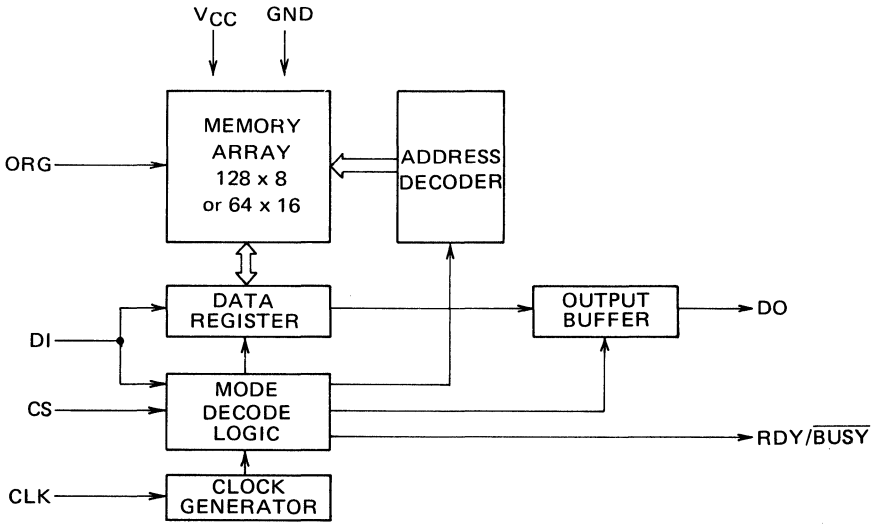
PIN CONFIGURATION

8 Pin Dual-In-Line
8 Pin S.O. Package

TOP VIEW



BLOCK DIAGRAM



8

PIN FUNCTIONS			
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5 V the 64 x 16 organization is selected. When it is connected to ground the 128 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 64 x 16 organization.
CLK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5 V Power Supply		
RDY/$\overline{BUSY}$	Status Output		
GND	Ground		

			INSTRUCTION SET				
Instruction	Start Bit	Opcode	Address		Data		Comments
			128 x 8	64 x 16	128 x 8	64 x 16	
READ	1	1000	A_6-A_0	A_5-A_0			Read Address A_N-A_O
PROGRAM	1	x100	A_6-A_0	A_5-A_0	D_7-D_0	$D_{15}-D_0$	Program Address A_N-A_O
PEN	1	0011	0000000	000000			Program Enable
PDS	1	0000	0000000	000000			Program Disable
ERAL	1	0010	0000000	000000			Erase All Addresses
WRAL	1	0001	0000000	000000	D_7-D_0	$D_{15}-D_0$	Write All Addresses

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25 °C	−0.3 ~ 7	V
Input Voltage	V		−0.3 ~ V_{CC} + 0.3	V
Output Voltage	V_o		−0.3 ~ V_{CC} + 0.3	V
Storage Temperature	T_{STG}		−55 ~ + 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Range	Unit
Supply Voltage	V_{CC}	5 ± 10%	V
Temperature Range	Ta	−40~85	°C
Data Hold Temperature	Ta	−40~85	°C

DC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Ta = −40 ~ 85°C, unless otherwise specified.)

Parameter	Symbol	Condition	MIN	MAX	Unit
Supply Voltage	V_{CC}		4.5	5.5	V
Power Supply Current	I_{CC1}	V_{CC} = 5.5 V CS = 1		5	mA
	I_{CC2}	V_{CC} = 5.5 V CS = 0 DI = 0 or V_{CC}		100	μA
"L" Input Voltage	V_{IL}		−0.1	0.8	V
"H" Input Voltage	V_{IH}		2.0	V_{CC} + 1	V
"L" Output Voltage	V_{OL}	TTL I_{OL} = 2.1 mA		0.4	V
		CMOS I_{OL} = 100 μA		0.1	V
"H" Output Voltage	V_{OH}	TTL I_{OH} = −400 μA	2.4		V
		CMOS I_{OH} = −40μA	V_{CC}−0.5		V
Input Leakage Current	I_{LI}	$0 \leqq V_{IN} \leqq V_{CC}$	−15	10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.5 V CS = 0		10	μA

8

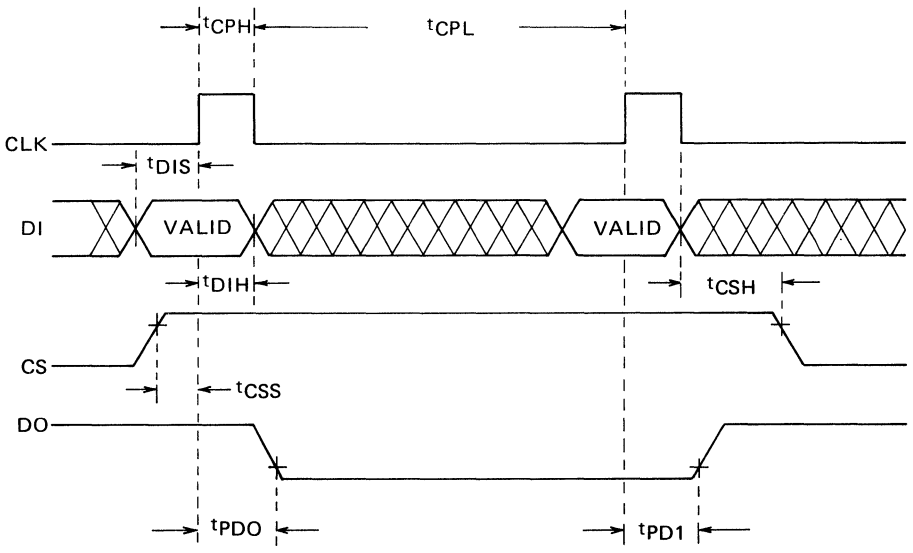
AC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Ta = −40 ~ 85°C, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{CLK}	CLK Frequency	0		250	kHz	
t_{CSS}	CS Setup Time with respect to CLK Falling	0.2			μs	
t_{CSH}	CS Hold Time with respect to CLK Rising	0			μs	
t_{DIST}	DI Setup Time with respect to CLK Rising	0.4			μs	
t_{DIH}	DI Hold Time with respect to CLK Rising	0.4			μs	
t_{CPH}	CLK Pulse High Time	1.0			μs	
t_{CPL}	CLK Pulse Low Time	1.0			μs	
t_{PD1}	Delay Time of DO Rising with respect to CLK Rising			2.0	μs	1
t_{PDO}	Delay Time of DO Falling with respect to CLK Rising			2.0	μs	1
t_P	"L" Time of Status (Programming Time)			10	ms	

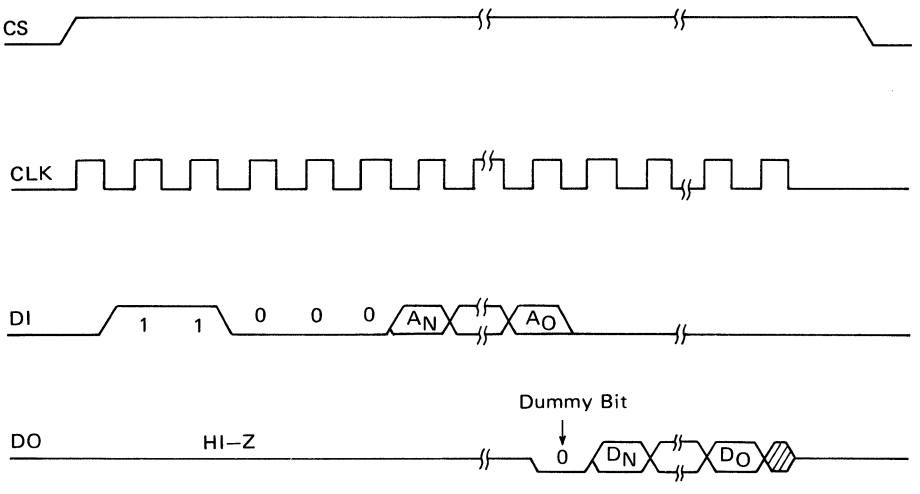
Note 1: Condition: C_L = 100pF and V_{OL}/OH = 0.8/2.0

Figure 1. Synchronous Data Timing



8

Figure 2. READ Mode



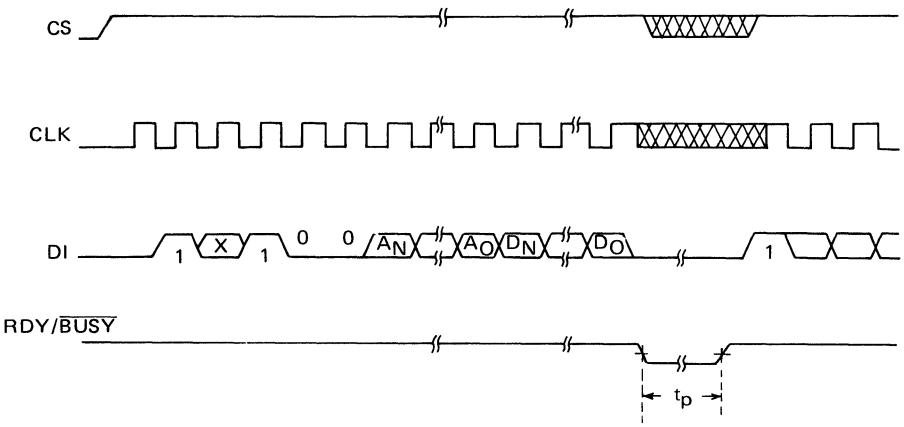
Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

8

Read Mode

The READ instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a serial-out shift register. A dummy bit (logical "0") procedes the data output string. The output data changes during the high states of the system clock.

Figure 3. PROGRAM Mode



Organization	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

Program Mode

The program instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

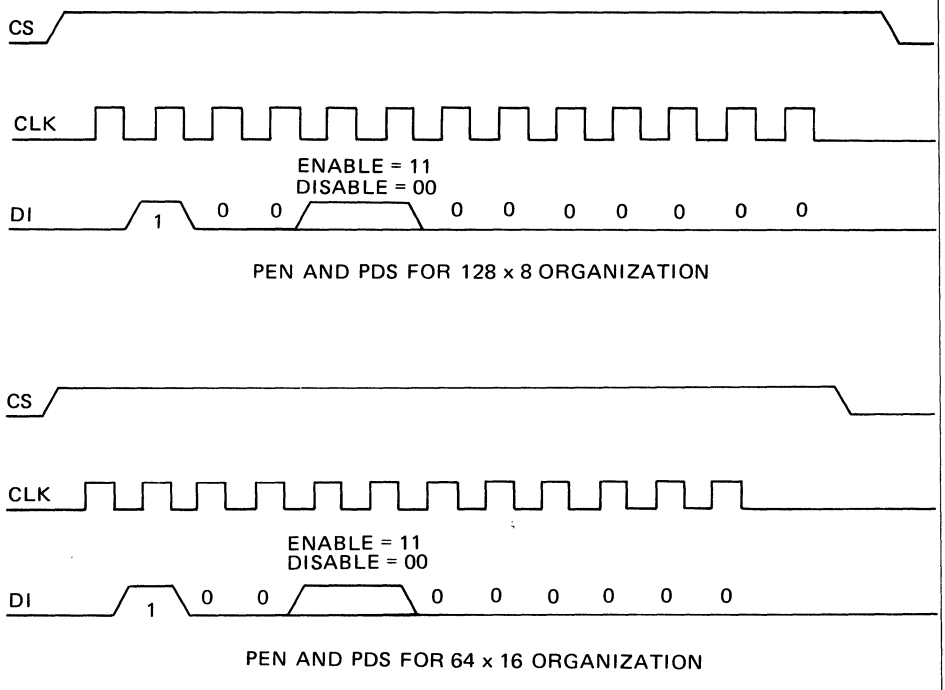
After the last data bit (DO) has been shifted into the data register the contents of the specified address will be erased and the new data written to the same address.

During the automatic erase/write sequence the RDY/$\overline{\text{BUSY}}$ output will go low for the duration of the automatic programming cycle as indicated by tp.

During a program cycle the internal erase and write operations occur automatically and are self-timed on the device. A single memory location may also be erased by programming that address with all "1's".

8

Figure 4. PEN (Program Enable) and PDS (Program Disable)



PEN AND PDS FOR 128 x 8 ORGANIZATION

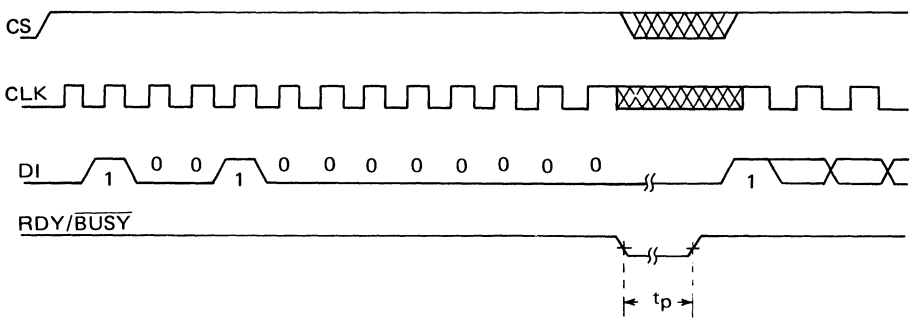
PEN AND PDS FOR 64 x 16 ORGANIZATION

8

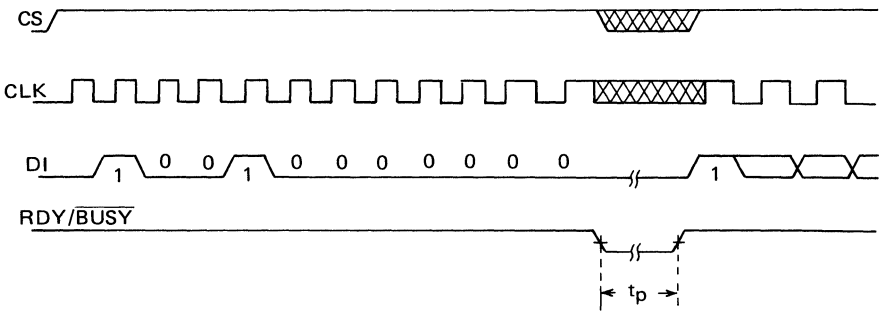
Program Enable and Program Disable

Programming must be preceded once by a programming enable (PEN) instruction. Programming remains enabled until a programming disable (PDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both PEN and PDS instructions.

Figure 5. ERAL (Erase All) Mode (128 x 8)



ERAL (Erase All) Mode (64 x 16)



Chip Erase

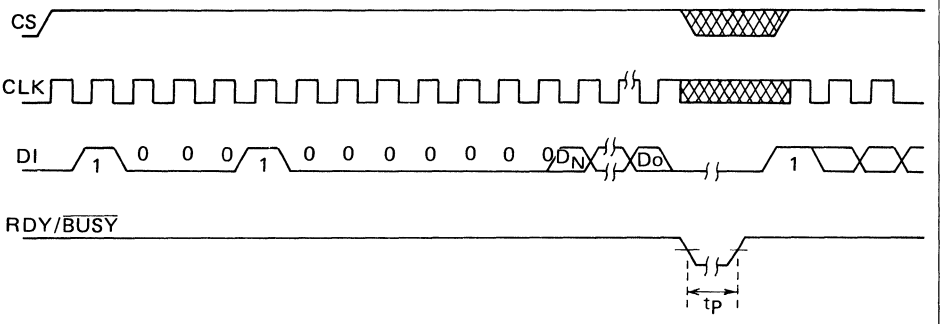
Entire chip erasing is provided for ease of programming and is implemented with the ERAL (erase all registers) instruction. Erasing the chip means that all registers in the memory array have each bit set to a "1".

All specifications and details published are subject to change without notice.

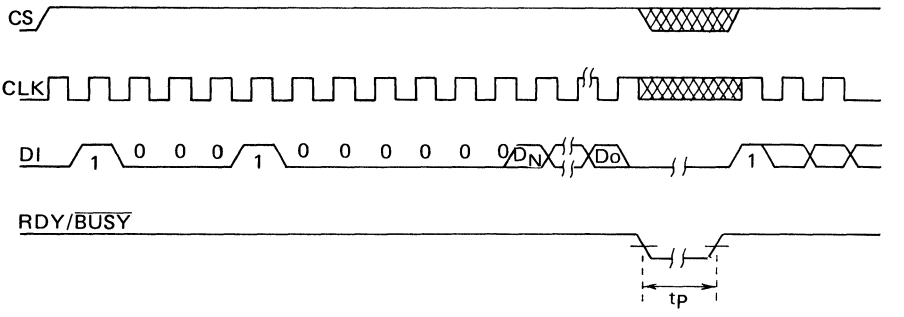
8

Figure 6. WRITE ALL

WRAL (Write All) Mode (128 x 8)



WRAL (Write All) Mode (64 x 16)



	A_N	D_N
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

Write All

This instruction is provided to write simultaneously all the registers. All the registers must be erased before doing a WRAL operation. After a WRAL instruction has been shifted in, the RDY/BUSY pin goes low and the self timed write sequence starts. The RDY/BUSY pin will act as a status indicator. It will remain low as long as the chip is programming. It will go high after all the bits of the array have been set to their proper value.

Preliminary

OKI semiconductor

MSM16812

2,048 BIT SERIAL E²PROM

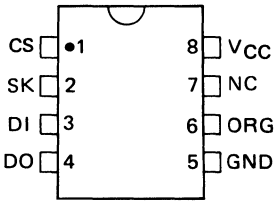
FEATURES:

- CMOS Floating Gate Technology
- Single +5-volt supply
- Eight pin plastic package
- 128 x 16 or 256 x 8 user selectable serial memory
- Microwire™ compatible
- Self timed programming cycle with Auto erase
- Word and chip erasable
- Operating Range 0°C to 70°C
- 10,000 erase/write cylces
- 10 year data retention

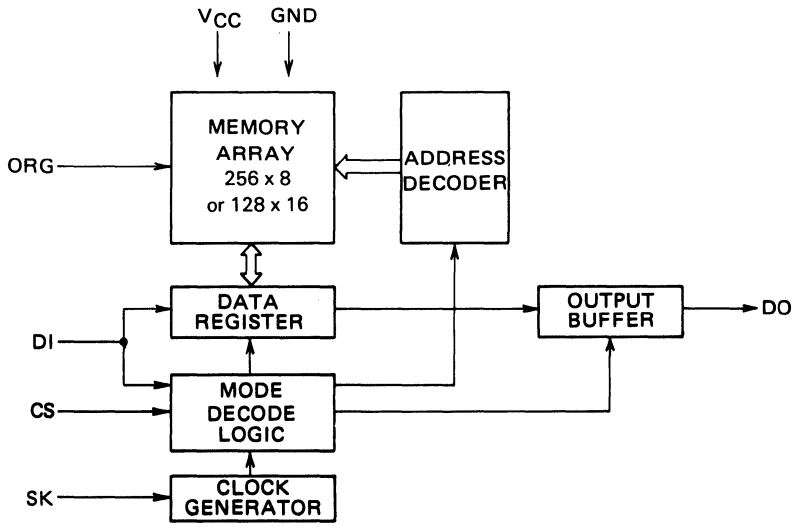
PIN CONFIGURATION

8 Pin Dual-In-Line

TOP VIEW



BLOCK DIAGRAM



8

PIN FUNCTIONS			
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5 V the 128 x 16 organization is selected. When it is connected to ground the 256 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 128 x 16 organization.
SK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5 V Power Supply		
NC	Non Connection		
GND	Ground		

			INSTRUCTION SET				
			Address		Data		
Instruction	Start Bit	Opcode	256 x 8	128 x 16	256 x 8	128 x 16	Comments
READ	1	1 0	$A_7 - A_0$	$A_6 - A_0$			Read Address $A_N - A_0$
ERASE	1	1 1	$A_7 - A_0$	$A_6 - A_0$			ERASE Address $A_N - A_0$
WRITE	1	0 1	$A_7 - A_0$	$A_6 - A_0$	$D_7 - D_0$	$D_{15} - D_0$	WRITE Address $A_N - A_0$
EWEN	1	0 0	11XXXXXX	11XXXXX			Program Enable
EWDS	1	0 0	00XXXXXX	00XXXXX			Program Disable
ERAL	1	0 0	10XXXXXX	10XXXXX			Erase All Addresses
WRAL	1	0 0	01XXXXXX	01XXXXX	$D_7 - D_0$	$D_{15} - D_0$	Program All Addresses

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

8

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25 °C	−0.3 ~ 7	V
Input Voltage	V_i		−0.3 ~ V_{CC} + 0.3	V
Output Voltage	V_o		−0.3 ~ V_{CC} + 0.3	V
Storage Temperature	T_{STG}		−55 ~ + 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Range	Unit
Supply Voltage	V_{CC}	5 ± 10 %	V
Temperature Range	Ta	0 ~ 70	°C
Data Hold Temperature	Ta	0 ~ 70	°C

DC CHARACTERISTICS

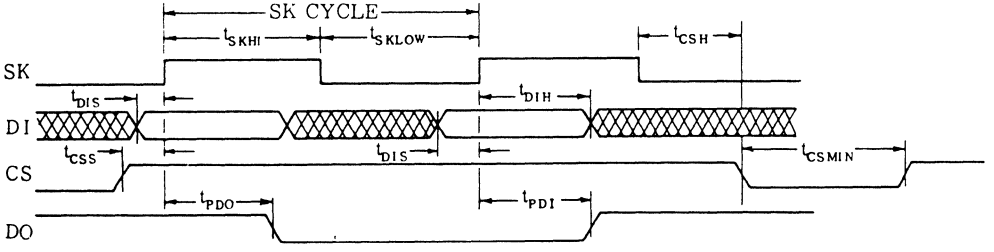
(V_{CC} = 4.5V to 5.5V, Ta = 0 ~ 70°C, unless otherwise specified.)

Parameter	Symbol	Condition	MIN	MAX	Unit
Supply Voltage	V_{CC}		4.5	5.5	V
Power Supply Current	I_{CC1}	V_{CC} = 5.5 V CS = 1		3	mA
	I_{CC2}	V_{CC} = 5.5 V CS = 0 DI = 0 or V_{CC}		100	μA
"L" Input Voltage	V_{IL}		−0.1	0.8	V
"H" Input Voltage	V_{IH}		2.0	V_{CC} + 1	V
"L" Output Voltage	V_{OL}	TTL I_{OL} = 2.1 mA		0.4	V
		CMOS I_{OL} = 100 μA		0.1	V
"H" Output Voltage	V_{OH}	TTL I_{OH} = −400 μA	2.4		V
		CMOS I_{OH} = −100 μA	V_{CC}−0.5		V
Input Leakage Current	I_{LI}	V_{in} = 5.5 V		10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.5 V CS = 0		10	μA

8

AC CHARACTERISTICS

Parameter	Description	Test Condition	Min	Typ	Max	Units
t_{CSS}	CS Setup Time		50			ns
t_{CSH}	CS Hold Time		0			ns
t_{DIS}	DI Setup Time		100			ns
t_{DIH}	DI Hold Time		100			ns
t_{PD1}	Output Delay to 1	CL = 100pF			500	ns
t_{PD0}	Output Delay to 0	V_{OL} = 0.8V, V_{OH} = 2.0			500	ns
t_{HZ}	Output Delay to HiZ	V_{IL} = 0.45V, V_{IH} = 2.4			100	ns
t_{EW}	Erase / Write Pulse Width				10	ms
t_{CSMIN}	Min CS Low Time		250			ns
t_{SKHI}	Min SK High Time		250			ns
t_{SKLOW}	Min SK Low Time		250			ns
t_{SV}	Output Delay to Status Valid	C_L = 100 pF			500	ns
SK_{MAX}	Maximum Frequency		0		1	MHz



Synchronous Timings

8

DEVICE OPERATION

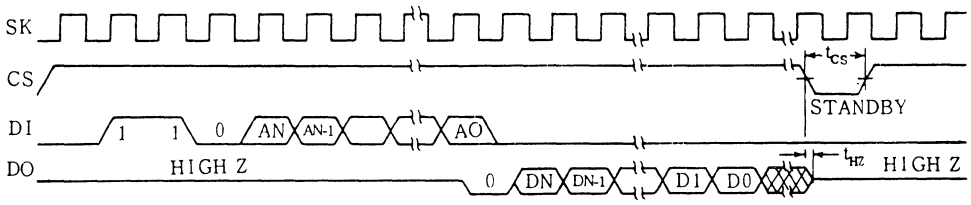
The MSM 16811 RS has 7 instructions that allow it to read, erase, or write. Each instruction consists of a start bit logical '1', an opcode field (2 bits or 4 bits) and an address field (6 or 7 bits).

The DO pin is a multiplexed pin. It is used as Data Out during the Read mode. It can also be used as a Ready Busy status indicator in programming mode. In all the other modes DO is tri-stated.

During power-up, all modes of operation are disabled and the device comes up in a program disabled state. An EWEN instruction has to be issued before starting to program.

At power-down, when V_{CC} falls below a level of approximately 3V, the data protection circuitry inhibits all modes of operation and an EWDS instruction is executed internally.

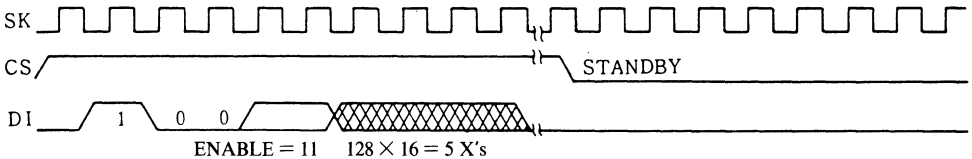
READ MODE



Organization	A_N	D_N
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

The READ instruction reads the contents of the addressed register. It outputs data serially on the DO pin. After the instruction is decoded, a dummy bit (logical "0") precedes the output data string.

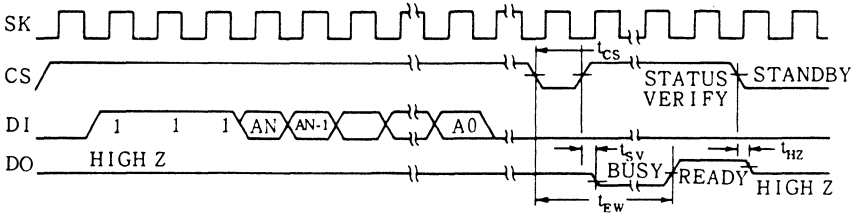
ERASE/WRITE ENABLE AND DISABLE



After power-up and before starting any programming instruction the EWEN instruction has to be issued. Once it has been issued, it will remain active until an EWDS instruction takes place. The EWDS instruction is provided to avoid any accidental programming of the part. The READ instruction is independent from the EWEN and EWDS instructions.

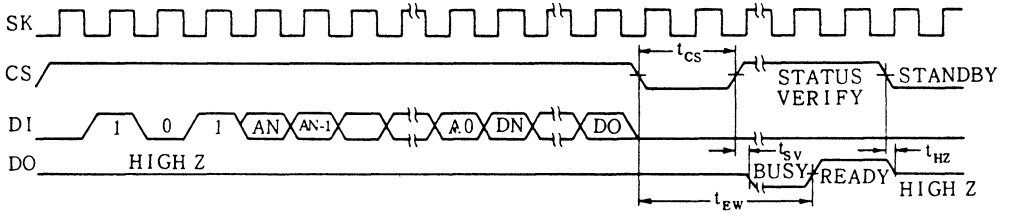
8

ERASE MODE



After an ERASE instruction has been shifted in. CS is dropped low. This will set the beginning of the self timed erase sequence. If CS is then brought high (after observing t_{CS} spec) the DO pin will act as a status indicator. It will remain low as long as the chip is programming. It will go high after all the bits of the addressed register have been set to a logical '1'.

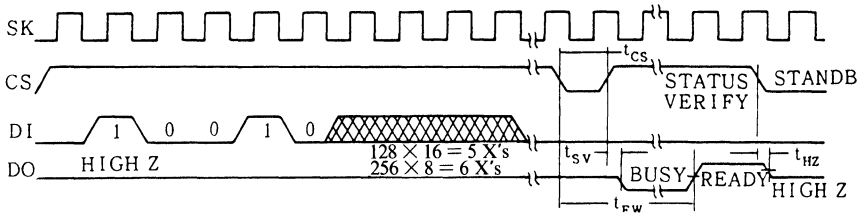
WRITE MODE



After a WRITE instruction has been shifted in with ite corresponding 8 bits or 16 bits of data, CS is dropped low. This will set the beginning of the self timed programming sequence. If CS is brought high during the programming time (after observing the t_{CS} specification), the DO pin will act as a status indicator — it will remain low as long as the chip is programming. It will go high after all the bits of the addressed register have been set to their proper value. With the MSM16812 it is NOT neccessary to erase a memory location before the WRITE instruction.

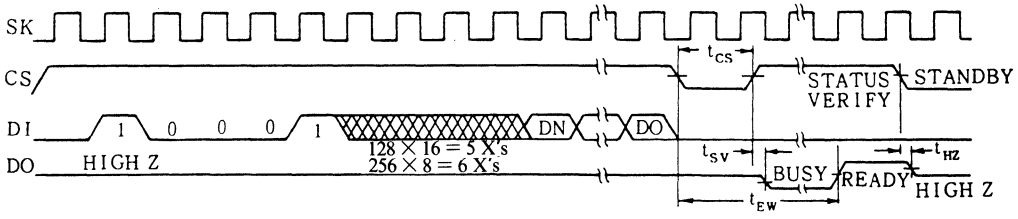
Configuration	A_N	D_N
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

ERASE ALL



This instruction is provided to erase the whole chip. Besides its different opcode, the ERAL instruction is identical to the ERASE instruction.

WRITE ALL



This instruction is provided to write simultaneously all the registers. All the registers must be erased before doing a WRAL operation. Besides its different opcode, the WRAL instruction is identical to the WRITE instruction.

8

Preliminary

OKI semiconductor

MSM16912

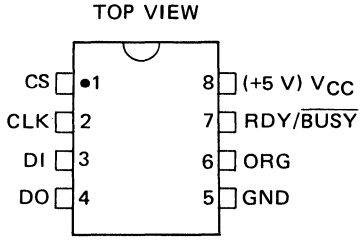
2048 BIT SERIAL EEPROM

FEATURES:

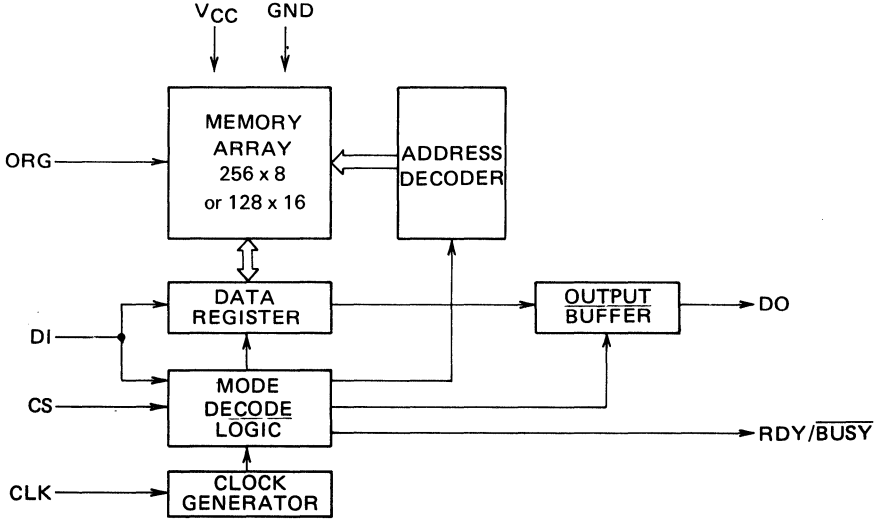
- CMOS Floating Gate Technology
- Single +5-volt supply
- Eight pin plastic package
- 128 x 16 or 256 x 8 user selectable serial memory
- Compatible with GI5912
- Self timed programming cycle with Auto erase
- Word and chip erasable
- Operating Range 0°C to 70°C
- 10,000 erase/write cylces
- 10 year data retention

PIN CONFIGURATION

8 Pin Dual-In-Line



BLOCK DIAGRAM



8

PIN FUNCTIONS			
CS	Chip Select	ORG	Memory Array Organization Selection Input. When the ORG pin is connected to +5 V the 128 x 16 organization is selected. When it is connected to ground the 256 x 8 organization is selected. If the ORG pin is left unconnected, then an internal pull-up device will select the 128 x 16 organization.
CLK	Clock Input		
DI	Serial Data Input		
DO	Serial Data Output		
V_{CC}	+5 V Power Supply		
RDY/$\overline{BUSY}$	Status Output		
GND	Ground		

			INSTRUCTION SET				
Instruction	Start Bit	Opcode	Address		Data		Comments
			256 x 8	128 x 16	256 x 8	128 x 16	
READ	1	1000	$A_7 - A_0$	$A_6 - A_0$			Read Address $A_N - A_0$
PROGRAM	1	x100	$A_7 - A_0$	$A_6 - A_0$	$D_7 - D_0$	$D_{15} - D_0$	Program Address $A_N - A_0$
PEN	1	0011	00000000	0000000			Program Enable
PDS	1	0000	00000000	0000000			Program Disable
ERAL	1	0010	00000000	0000000			Erase All Addresses
WRAL	1	0001	0000000	000000	$D_7 - D_0$	$D_{15} - D_0$	Write All Addresses

DI/DO: It is possible to connect the Data In and Data Out pins together. However, with this configuration it is possible for a "bus conflict" to occur during the "dummy zero" that precedes the read operation, if A_0 is a logic high level. Under such a condition the voltage level seen at Data Out is undefined and will depend upon the relative impedances of Data Out and the signal source driving A_0. The higher the current sourcing capability of A_0, the higher the voltage at the Data Out pin.

Power-On Data Protection Circuitry: During power-up all modes of operation are inhibited until V_{CC} has reached a level of between 2.8 and 3.5 volts. During power-down the source data protection circuitry acts to inhibit all modes when V_{CC} has fallen below the voltage range of 2.8 to 3.5 volts.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Value	Unit
Supply Voltage	V_{CC}	Ta = 25 °C	−0.3 ~ 7	V
Input Voltage	V		−0.3 ~ V_{CC} + 0.3	V
Output Voltage	V_0		−0.3 ~ V_{CC} + 0.3	V
Storage Temperature	T_{STG}		−55 ~ + 150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as recommended. Exposure to ABSOLUTE MAXIMUM RATINGS for extended periods may affect device reliability.

RECOMMENDED OPERATING RANGE

Parameter	Symbol	Range	Unit
Supply Voltage	V_{CC}	5 ± 10%	V
Temperature Range	Ta	0 ~ 70	°C
Data Hold Temperature	Ta	0 ~ 70	°C

DC CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, Ta = 0 ~ 70°C, unless otherwise specified.)

Parameter	Symbol	Condition	MIN	MAX	Unit
Supply Voltage	V_{CC}		4.5	5.5	V
Power Supply Current	I_{CC1}	V_{CC} = 5.5 V CS = 1		3	mA
	I_{CC2}	V_{CC} = 5.5 V CS = 0 DI = 0 or V_{CC}		100	μA
"L" Input Voltage	V_{IL}		−0.1	0.8	V
"H" Input Voltage	V_{IH}		2.0	V_{CC} + 1	V
"L" Output Voltage	V_{OL}	TTL I_{OL} = 2.1 mA		0.4	V
		CMOS I_{OL} = 100 μA		0.1	V
"H" Output Voltage	V_{OH}	TTL I_{OH} = −400 μA	2.4		V
		CMOS I_{OH} = −100 μA	V_{CC}−0.5		V
Input Leakage Current	I_{LI}	V_{in} = 5.5 V		10	μA
Output Leakage Current	I_{LO}	V_{out} = 5.5 V CS = 0		10	μA

8

AC CHARACTERISTICS

(V_{CC} = 4.5 V to 5.5 V, Ta = 0 ~ 70°C, unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Note
f_{CLK}	CLK Frequency	0		1	MHz	
t_{CSS}	CS Setup Time with respect to CLK Falling	50			ns	
t_{CSH}	CS Hold Time with respect to CLK Rising	100			ns	
t_{DIS}	DI Setup Time with respect to CLK Rising	100			ns	
t_{DIH}	DI Hold Time with respect to CLK Rising	100			ns	
t_{CPH}	CLK Pulse High Time	250			ns	
t_{CPL}	CLK Pulse Low Time	250			ns	
t_{PD1}	Delay Time of DO Rising with respect to CLK Rising			500	ns	1
t_{PDO}	Delay Time of DO Falling with respect to CLK Rising			500	ns	1
t_P	"L" Time of Status (Programming Time)			10	ms	

Note 1: Condition: C_L = 100pF and $V_{OL/OH}$ = 0.8/2.0

Figure 1. Synchronous Data Timing

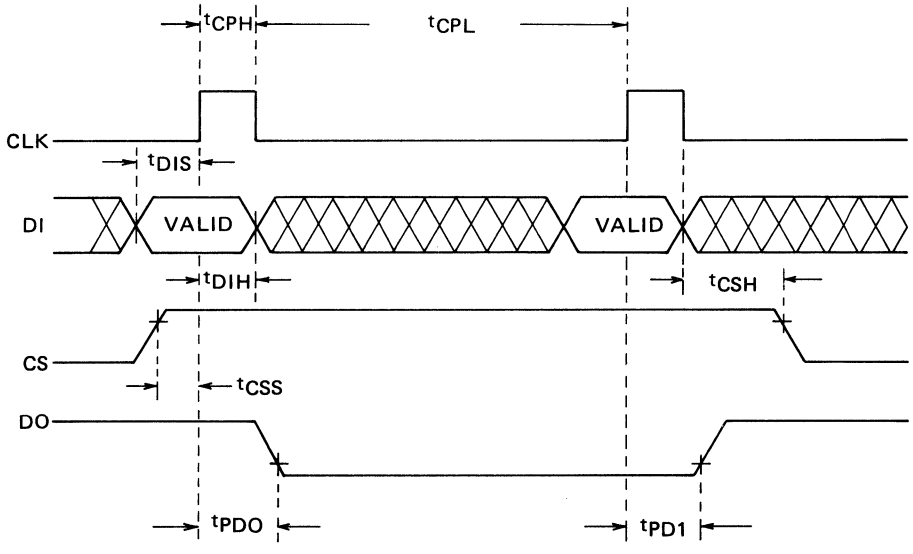


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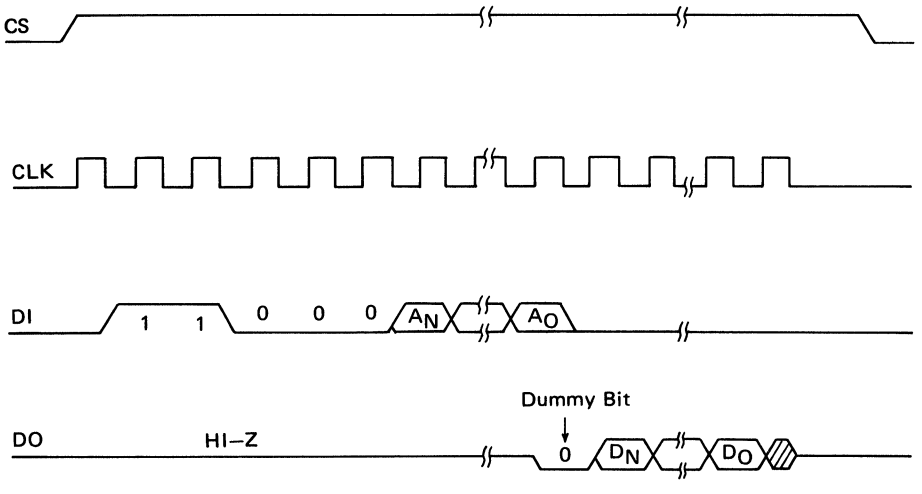
Figure 2. READ Mode



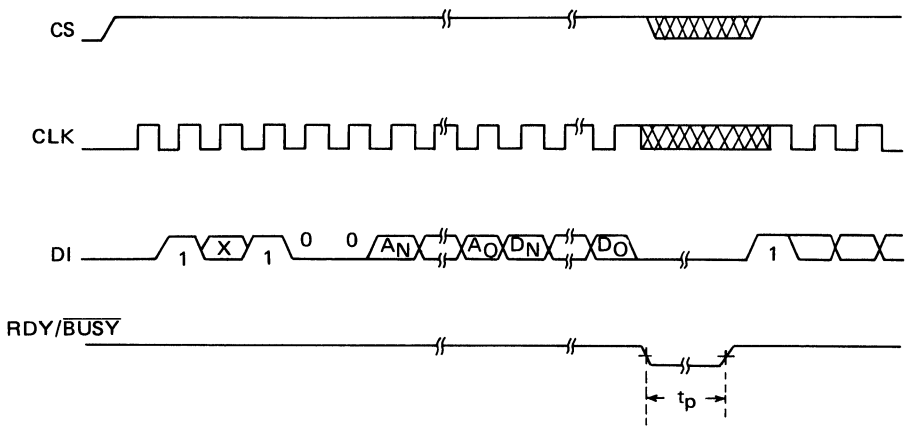
Organization	A_N	D_N
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

8

Read Mode

The READ instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a serial-out shift register. A dummy bit (logical "0") procedes the data output string. The output data changes during the high states of the system clock.

Figure 3. PROGRAM Mode



Organization	A_N	D_N
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

8

Program Mode

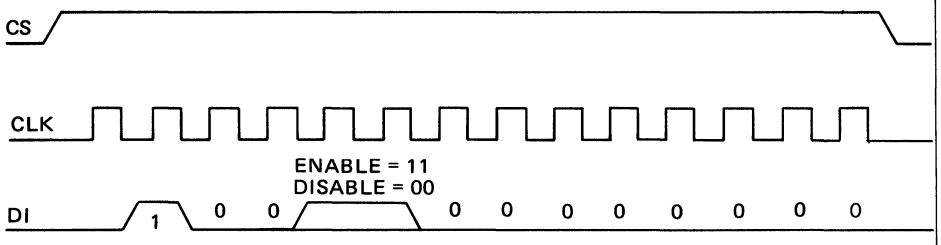
The program instruction is followed by either eight or sixteen bits of data, which are to be written into the specified address.

After the last data bit (DO) has been shifted into the data register the contents of the specified address will be erased and the new data written to the same address.

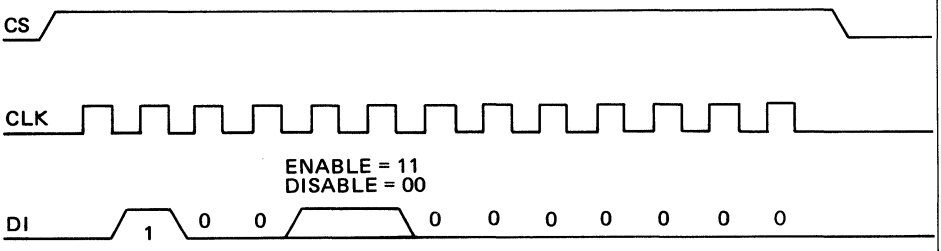
During the automatic erase/write sequence the RDY/$\overline{\text{BUSY}}$ output will go low for the duration of the automatic programming cycle as indicated by tp.

During a program cycle the internal erase and write operations occur automatically and are self-timed on the device. A single memory location may also be erased by programming that address with all "1's".

Figure 4. PEN (Program Enable) and PDS (Program Disable)



PEN AND PDS FOR 256 x 8 ORGANIZATION



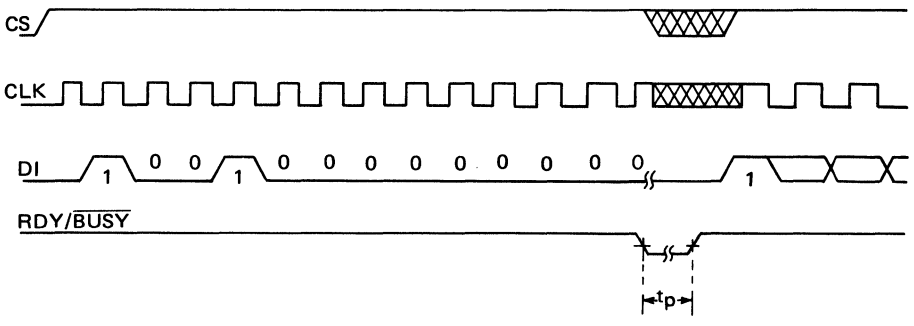
PEN AND PDS FOR 128 x 16 ORGANIZATION

8

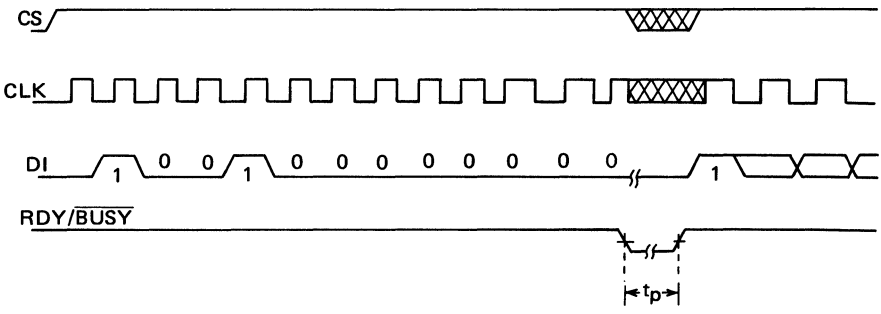
Program Enable and Program Disable

Programming must be preceded once by a programming enable (PEN) instruction. Programming remains enabled until a programming disable (PDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both PEN and PDS instructions.

Figure 5. ERAL (Erase All) Mode (256 x 8)



ERAL (Erase All) Mode (128 x 16)



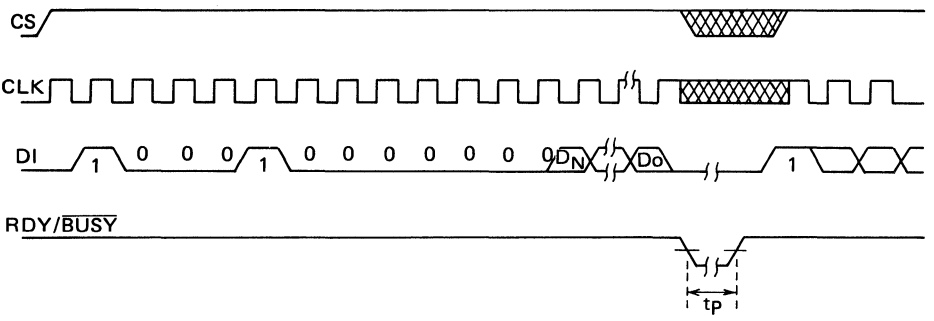
Chip Erase

Entire chip erasing is provided for ease of programming and is implemented with the ERAL (erase all registers) instruction. Erasing the chip means that all registers in the memory array have each bit set to a "1".

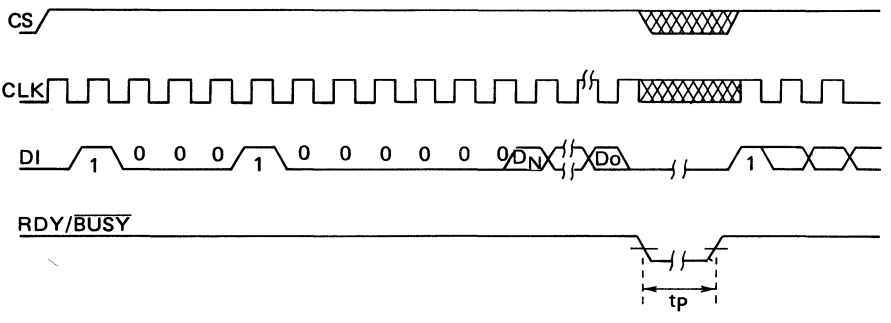
All specifications and details published are subject to change without notice.

Figure 6. WRITE ALL

WRAL (Write All) Mode (256 x 8)



WRAL (Write All) Mode (128 x 16)



	A_N	D_N
256 x 8	A_7	D_7
128 x 16	A_6	D_{15}

Write All

This instruction is provided to write simultaneously all the registers. All the registers must be erased before doing a WRAL operation. After a WRAL instruction has been shifted in, the RDY/BUSY pin goes low and the self timed write sequence starts. The RDY/BUSY pin will act as a status indicator. It will remain low as long as the chip is programming. It will go high after all the bits of the array have been set to their proper value.

8

OKI semiconductor
MSM28C16A

2K x 8 BIT CMOS ELECTRICALLY ERASABLE & PROGRAMABLE ROM

GENERAL DESCRIPTION

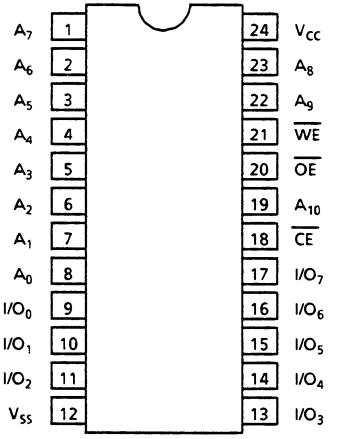
The MSM28C16ARS is a CMOS electrically erasable and programmable read only memory (E^2PROM) with a capacity of 2,048 words x 8 bits using a single 5V power supply. It features easy use because it operates with a single 5V power supply and its operation timing is similar to that of a static RAM. Byte data rewriting in programming mode starts when the $\overline{WE}$ and $\overline{CE}$ signals are set to the TTL low (L) level for 100 ns. The address and data bus information are latched in the IC, and the system is released for other tasks during the write cycle. Writing in the MSM28C16A starts after automatic erasure of the selected byte, and the erase/write cycle completes within 10 ms.

FEATURES

- Single 5V power supply
- High-speed access: 150 ns max.
  200 ns max.
- Byte write cycle: 10 ms max.
- Internal address and data latch in write cycle
- Automatic erasure before writing
- Automatic ending of write operation
- Built-in protective function for false writing
- TTL compatible input/output
- Pin arrangement in compliance with JEDEC Standard
- Compatible with Xicor 2816A

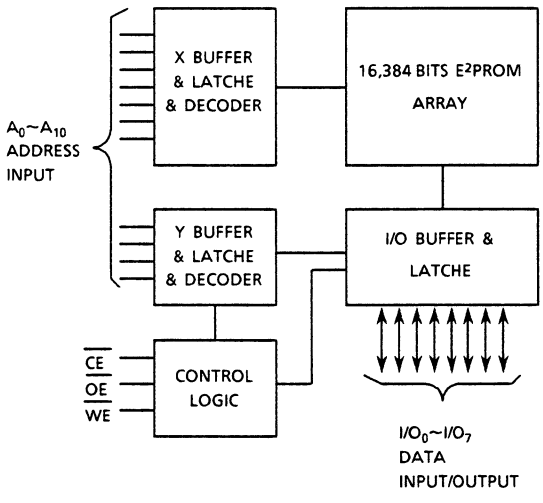
PIN CONFIGURATION

(Top View)



A_0~A_{10} :ADDRESS INPUTS
I/O_0~I/O_7 :DATA I/O
$\overline{CE}$:CHIP ENABLE
$\overline{OE}$:OUTPUT ENABLE
$\overline{WE}$:WRITE ENABLE
V_{CC} : +5V
V_{SS} :GROUND

FUNCTION BLOCK DIAGRAM



8

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
V_{IH}	X	X	Standby	High Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⊓	Byte Write (WE controlled)	D_{IN}	Active
⊓	V_{IH}	V_{IL}	Byte Write (CE controlled)	D_{IN}	Active
X	X	V_{IH}	Write Inhibit	High Z	
X	V_{IL}	X	Write Inhibit	High Z	

Note) X: Don't care (V_{IH} or V_{IL})

DEVICE OPERATION

<READ>

The data in the MSM28C16A can be read by setting $\overline{WE}$ to high (H), $\overline{CE}$ to low (L) and $\overline{OE}$ to L. The data becomes valid upon lapse of t_{AA} after the address change, t_{CE} after $\overline{CE}$ setting to L, or t_{OE} after $\overline{OE}$ setting to L, whichever is the latest. The I/O pin remain in a high impedance state to prevent data bus contention in the system when $\overline{OE}$ or $\overline{CE}$ is set to H.

<WRITE>

The write cycle starts when $\overline{WE}$ and $\overline{CE}$ are set to L and $\overline{OE}$ is set to H. The address input is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ (Whichever is later). The I/O pin data is latched on the first rising edge of $\overline{WE}$ or $\overline{CE}$. The address and data are latched in 100 ns using the TTL level write signal. When the data latch ends, the MSM28C16A automatically erases the selected byte and writes the new data within 10 ms.

8

<DATA POLLING>

DATA polling is provided to indicate the completion of write cycle. While the write operation is in progress, attempt to read the last byte written will output the comlement of that data on I/07. Once the write cycle is completed, all I/Os will produce true data during a read cycle.

<STANDBY>

The power consumption decrease greatly by setting $\overline{CE}$ to TTL H level.

<ENDURANCE>

The MSM28C16A is designed for applications each requiring up to 10,000 write cycles per byte.

<DATA PROTECTION>

Four functions are incorporated to prevent false writing at the time of power up, power down or power noise.

1. V_{CC} Level Detection

   The write cycle to the device is automatically inhibited when V_{CC} drops below 3.0V.

2. TIME DELAY

The MSM28C16A automatically inhibits any write operation for the period between 5 ms and 10 ms after V_{CC} reaches V_{WI} level at the time of power up.
This allows sufficient time for the system to set $\overline{WE}$ or $\overline{CE}$ to the H level before the start of writing.

3. $\overline{OE}$ GATING

The MSM28C16A inhibits any write operation when $\overline{OE}$ is at the L level.

4. $\overline{WE}$ NOISE PROTECTION

The write cycle does not start for a write pulse shorter than 20 ns.

ABSOLUTE MAXIMUM RATINGS (Note 1)

(Ta = 25°C)

Rating	Symbol	Value	Unit	Condition
Power Supply Voltage	V_{CC}	− 0.3 to 7	V	Respect to V_{SS}
Input Voltage (Note 2)	V_I	− 0.3 to V_{CC} + 0.3	V	Respect to V_{SS}
Output Voltaeg (Note 2)	Vo	− 0.3 to V_{CC} + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	Topr	0 to 70	°C	−
Storage Temperature	Tstg	− 55 to 150	°C	−

Note 1) The stress upon exceeding the absolute maximum rating brings about a permanent damage to the device. There are stress ratings only and do not means "- functional operations of the device". They are by no means above the operating characteristics in the data sheet. Leaving the device for a long time in the absolute maximum rating state may adversely affect the device reliability.

Note 2) The device has a special circuit to protect the internal circuit from damage caused by static electricity, but do not use it beyond the maximum rating(s) for safety.

8

ELECTRICAL CHARACTERISTICS

<DC OPERATING CHARACTERISTICS>

(VCC = 5V ± 10%, Ta = 0°C~70°C)

PARAMETER	SYMBOL	TEST CONDITION	Limits		UNIT
			MIN.	MAX.	
Input Low Voltage	V_{IL}		−0.3	0.8	V
Input High voltage	V_{IH}		2.0	V_{CC} + 0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	−	0.4	V
Output High Voltage	V_{OH}	I_{OH} = −400μA	2.4	−	V
V_{CC} Voltage for Write Inhibit	V_{WI}		3.0	4.0	V
Input Leakage Current	I_{LI}	V_{IN} = 0 ~ V_{CC}	−10	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 ~ V_{CC}	−10	10	μA
V_{CC} Power Current	I_{CCA}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, Io = 0mA t_{RC} = 150ns V_{CC} = MAX	−	30	mA
Standby Current	I_{CCS}	$\overline{CE}$ = V_{CC} − 0.2V V_{CC} = MAX	−	0.1	mA
	I_{CCS1}	$\overline{CE}$ = V_{IH}, V_{CC} = MAX	−	1	mA

<CAPACITANCE>

(Ta = + 25°C, f = 1.0MHz, V_{CC} = 5V)

PARAMETER	SYMBOL	TEST CONDITION	MAX.	UNIT
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF

8

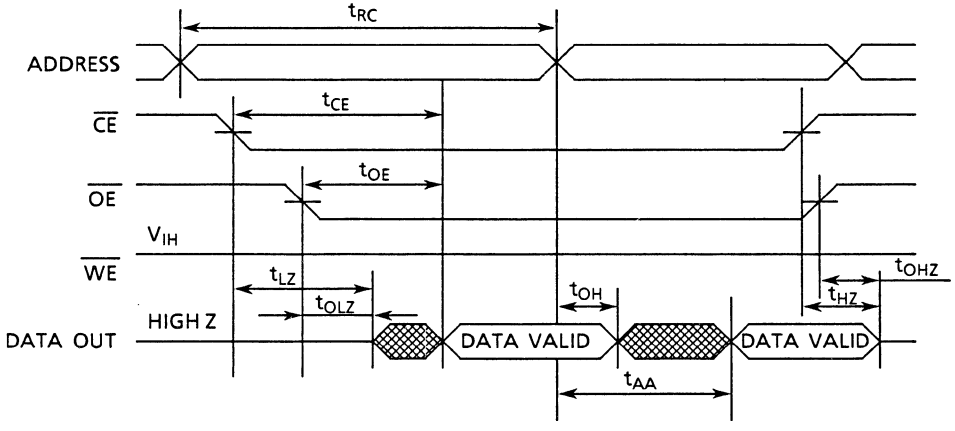
AC CHARACTERISTICS

<READ OPERATION>

(V_{CC} = 5V ± 10%, Ta = 0°C~70°C)

PARAMETER	SYMBOL	MSM28C16A-15		MSM28C16A-20		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	150	-	200	-	ns
Address Access Time	t_{AA}	-	150	-	200	ns
CE Access Time	t_{CE}	-	150	-	200	ns
OE Access Time	t_{OE}	-	70	-	80	ns
CE to Output in Low Z	t_{LZ}	10	-	10	-	ns
CE to Output in High Z	t_{HZ}	10	50	10	50	ns
OE to Output in Low Z	t_{OLZ}	10	-	10	-	ns
OE to Output in High Z	t_{OHZ}	10	50	10	50	ns
Output Hold Time	t_{OH}	15	-	20	-	ns

READ CYCLE



AC test conditions

Input Pulse Levels 0.6 to 2.4 volts
Input Rise/Fall times 5 ns

Timing Reference Levels INPUT : 1.5V,
OUTPUT: 0.8V & 2.0V

Output Load 1 TTL gate and C_L = 100 pF

8

<WRITE OPERATION>

(V_{CC} = 5V ± 10%, Ta = 0°C ~ 70°C)

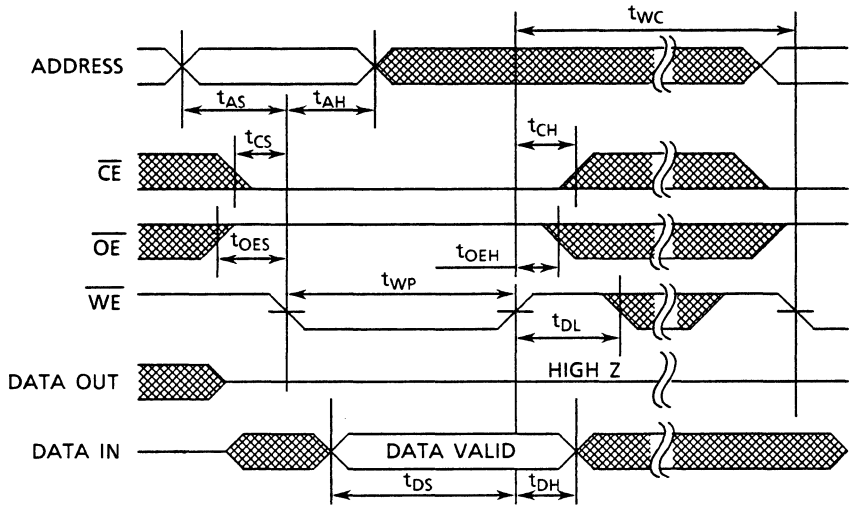
PARAMETER	SYMBOL	LIMITS		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	–	10	ms
Address Setup Time	t_{AS}	10	–	ns
Address Hold Time	t_{AH}	70	–	ns
Chip Enable or Write Setup Time	t_{CS}	0	–	ns
Chip Enable or Write Hold Time	t_{CH}	0	–	ns
Chip Enable Pulse Width	t_{CW}	100	–	ns
Output Enable Setup Time	t_{OES}	10	–	ns
Output Enable Hold Time	t_{OEH}	10	–	ns
Write Enable Pulse Width (Note 1)	t_{WP}	100	–	ns
Data Latch Time	t_{DL}	50	–	ns
Data Setup Time	t_{DS}	50	–	ns
Data Hold Time	t_{DH}	10	–	ns
Write Inhibit Time On Power Up	t_{INIT}	5	10	ms

Note 1) $\overline{WE}$ is protected from noise. The write cycle does not start when the write pulse is less than 20 ns.

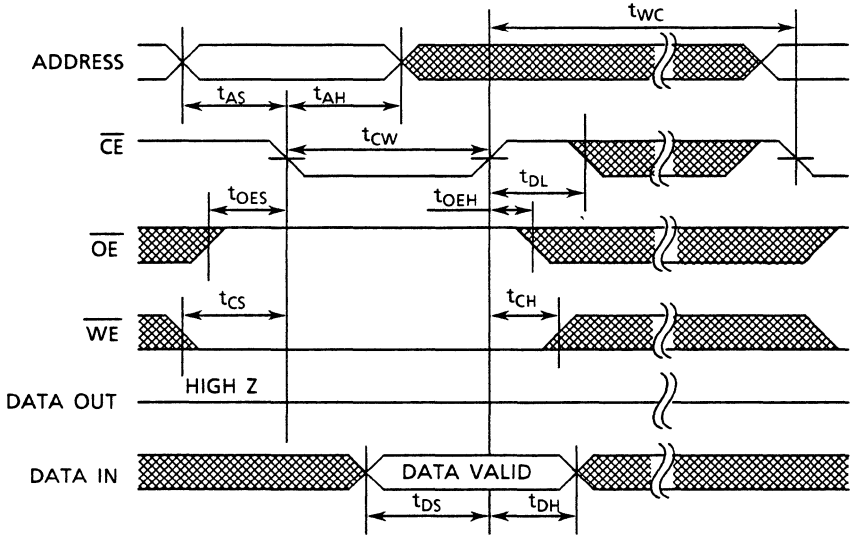
8

WRITE CYCLE

- CONTROLLED BY $\overline{WE}$



- CONTROLLED BY $\overline{CE}$



8

OKI semiconductor
MSM28C64A

8K x 8 BIT CMOS ELECTRICALLY ERASABLE & PROGRAMABLE ROM

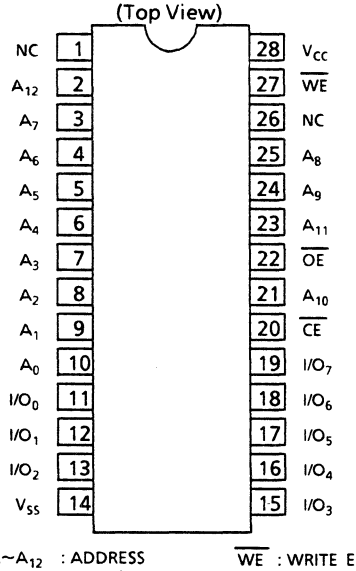
GENERAL DESCRIPTION

The MSM28C64ARS is a CMOS electrically erasable and programmable read only memory (E^2PROM) with a capacity of 8192 words x 8 bits using a single 5V power supply. It features easy use because it operates with a single 5V power supply and its operation timing is similar to that of a static RAM. The automatic page write allows the system to write up to 32 bytes during a single write cycle, providing an effective byte cycle of 312μs/byte. MSM28C64A also supports $\overline{\text{DATA}}$ polling to indicate the early completion of a write cycle.

FEATURES

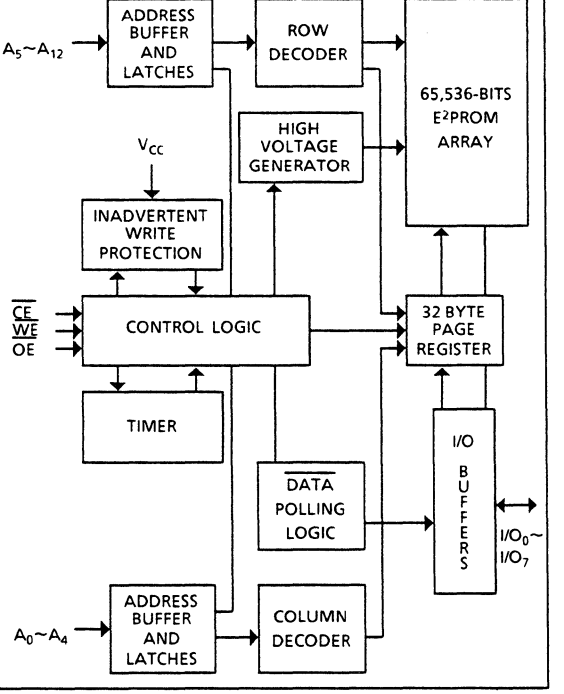
- Fast read access time 120 ns
- CMOS low power operation
- 5 volt-only operation including write mode
- Automatic page write 1 to 32 bytes in 10 ms max.
- Data polling status indicator
- TTL compatible inputs and outputs
- 10,000 rewrites per byte
- 10 years data retention
- JEDEC standard approved byte wide pinout

PIN CONFIGURATION



A_0~A_{12} : ADDRESS INPUTS
I/O_0~I/O_7 : DATA I/O
$\overline{CE}$: CHIP ENABLE
$\overline{OE}$: OUTPUT ENABLE
$\overline{WE}$: WRITE ENABLE
V_{CC} : V_{CC} POWER SUPPLY
V_{SS} : GROUND
NC : NO CONNECT

FUNCTION BLOCK DIAGRAM



MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
V_{IH}	X	X	Standby	High Z	Standby
V_{IL}	V_{IL}	V_{IH}	Read	D_{OUT}	Active
V_{IL}	V_{IH}	⎍	Byte write (WE controlled)	D_{IN}	Active
⎍	V_{IH}	V_{IL}	Byte write (CE controlled)	D_{IN}	Active
X	X	V_{IH}	Write inhibit	High Z	
X	V_{IL}	X	Write inhibit	High Z	

Note) X: Don't care (V_{IH} or V_{IL})

DEVICE OPERATION

<READ>

The data in the MSM28C64A can be read by setting $\overline{WE}$ to high (H), $\overline{CE}$ to low (L) and $\overline{OE}$ to L. The data becomes valid upon lapse of t_{AA} after the address change, t_{CE} after $\overline{CE}$ setting to L, or t_{OE} after $\overline{OE}$ setting to L, whichever is the latest. The I/O pin remain in a high impedance state to prevent data bus contention in the system when $\overline{OE}$ or $\overline{CE}$ is set to H.

<BYTE WRITE>

The write cycle starts when $\overline{WE}$ and $\overline{CE}$ are set to L and $\overline{OE}$ is set to H. The address input is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ (Whichever is later). The I/O pin data is latched on the first rising edge of $\overline{WE}$ or $\overline{CE}$. The address and data are latched in 150 ns using the TTL level write signal. When the data latch ends, the MSM28C64A automatically erases the selected byte and writes the new data within 10 ms.

<PAGE WRITE>

The MSM28C64A contains a 32 byte temporary buffer which allows programming of 1 to 32 bytes on a single 10 ms nonvolatile write cycle, which can effectively reduce programming time by a factor of 32. The 32 byte page into which the data will be written is specified by the addresses A5-A12 during the first system write operation following the completion of a previous nonvolatile write cycle. The byte within the specified page is identified by the adresses A0-A4 during the first and subsequent system write cycles. Bytes can be written into the page in any order. Each successive data load cycle, started by $\overline{WE}$ HIGH to LOW transition, must begin within 10 µs of the rising edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 µs, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide so long as the host continues to access the device within the data load cycle time of 10µs.

<DATA POLLING>

DATA polling is provided to indicate the completion of write cycle. While the write operation is in progress, any attempt to read the last byte written will output the comlement of that data on I/07. Once the write cycle is completed, all I/Os will produce true data during a read cycle.

<STANDBY>

The power consumption decrease greatly by setting CE to TTL H level.

<ENDURANCE>

The MSM28C64A is designed for applications each requiring up to 10,000 rewrites per byte.

<DATA PROTECTION>

Four functions are incorporated to prevent false writing at the time of power up, power down or power noise.

1. V_{CC} LEVEL DETECTION

The write cycle to the device is automatically inhibited when V_{CC} drops below 3.0V.

2. TIME DELAY

The MSM28C64A automatically inhibits any write operation for the period between 4 ms and 20 ms after V_{CC} reaches V_{WI} level at the time of power up.
This allows sufficient time for the system to set $\overline{WE}$ or $\overline{CE}$ to the H level before the start of writing.

3. $\overline{OE}$ GATING

The MSM28C64A inhibits any write operation when $\overline{OE}$ is at the L level.

4. $\overline{WE}$ NOISE PROTECTION

The write cycle does not start for a write pulse shorter than 20 ns.

8 ABSOLUTE MAXIMUM RATINGS (Note 1)

(Ta = 25°C)

Rating	Symbol	Value	Unit	Condition
Power Supply Voltage	V_{CC}	− 0.3 to 7	V	Respect to V_{SS}
Input Voltage (Note 2)	V_I	− 0.3 to V_{CC} + 0.3	V	Respect to V_{SS}
Output Voltaeg (Note 2)	Vo	− 0.3 to V_{CC} + 0.3	V	Respect to V_{SS}
Power Dissipation	P_D	1	W	Per package
Operating Temperature	Topr	0 to 70	°C	−
Storage Temperature	Tstg	− 55 to 150	°C	−

Note 1) The stress upon exceeding the absolute maximum rating brings about a permanent damage to the device. There are stress ratings only and do not means "- functional operations of the device". They are by no means above the operating characteristics in the data sheet. Leaving the device for a long time in the absolute maximum rating state may adversely affect the device reliability.

Note 2) The device has a special circuit to protect the internal circuit from damage caused by static electricity, but do not use it beyond the maximum rating(s) for safety.

ELECTRICAL CHARACTERISTICS

<DC OPERATING CHARACTERISTICS>

(V_{CC} = 5V ± 10%, Ta = 0°C ~ 70°C)

PARAMETER	SYMBOL	TEST CONDITION	LIMITS		UNIT
			MIN.	MAX.	
Input Low Voltage	V_{IL}		− 0.3	0.8	V
Input High voltage	V_{IH}		2.2	V_{CC} + 0.3	V
Output Low Voltage	V_{OL}	I_{OL} = 2.1mA	−	0.4	V
Output High Voltage	V_{OH}	I_{OH} = − 400μA	2.4	−	V
V_{CC} Voltage for Write Inhibit	V_{WI}		3.0	4.0	V
Input Leakage Current	I_{LI}	V_{IN} = 0 ~ V_{CC}	− 10	10	μA
Output Leakage Current	I_{LO}	V_{OUT} = 0 ~ V_{CC}	− 10	10	μA
V_{CC} Power Current	I_{CCA}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, I_O = 0mA t_{RC} = 120ns V_{CC} = MAX	−	30	mA
Standby Current	I_{CCS}	$\overline{CE}$ = V_{CC} − 0.2V, V_{CC} = MAX	−	0.1	mA
	I_{CCS1}	$\overline{CE}$ = V_{IH}, V_{CC} = MAX	−	1	mA

8

<CAPACITANCE>

Ta = + 25°C, f = 1.0MHz, V_{CC} = 5V

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT
Input/Output Capacitance	$C_{I/O}$	V_{IN} = 0V	-	10	pF
Input Capacitance	C_{IN}	V_{IN} = 0V	-	10	pF

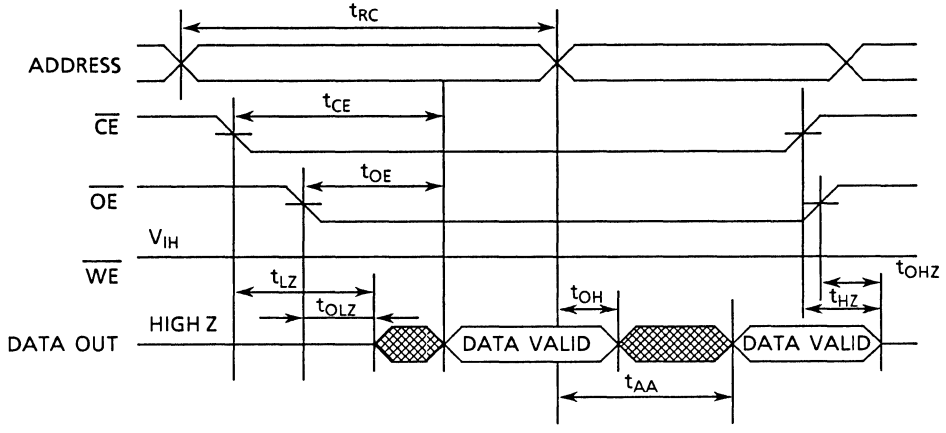
AC CHARACTERISTICS

<READ OPERATION>

Ta = 0°C to 70°C, V_{CC} = 5V ± 10%

PARAMETER	SYMBOL	28C64A-12		28C64A-15		28C64A-20		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	120	-	150	-	200	-	ns
Address Access Time	t_{AA}	-	120	-	150	-	200	ns
CE Access Time	t_{CE}	-	120	-	150	-	200	ns
OE Access Time	t_{OE}	-	60	-	70	-	90	ns
CE to Output in Low Z	t_{LZ}	10	-	10	-	10	-	ns
CE to Output in High Z	t_{HZ}	10	60	10	70	10	90	ns
OE to Output in Low Z	t_{OLZ}	10	-	10	-	10	-	ns
OE to Output in High Z	t_{OHZ}	10	60	10	70	10	90	ns
Output Hold Time	t_{OH}	20	-	20	-	20	-	ns

READ CYCLE



AC test conditions

Input Pulse Levels	0.6 to 2.4 volts
Input Rise/Fall times	5 ns

Timing Reference Levels INPUT : 1.5V, OUTPUT: 0.8V & 2.0V

Output Load 1 TTL gate and C_L = 100 pF

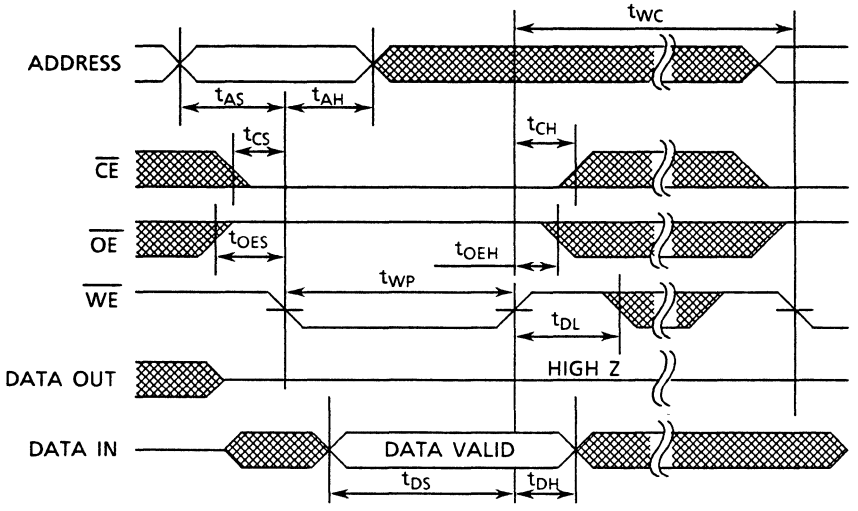
<WRITE OPERATION>

PARAMETER	SYMBOL	LIMITS		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	–	10	ms
Address Setup Time	t_{AS}	0	–	ns
Address Hold Time	t_{AH}	100	–	ns
Chip Enable or Write Setup Time	t_{CS}	0	–	ns
Chip Enable or Write Hold Time	t_{CH}	0	–	ns
Chip Enable Pulse Width	t_{CW}	150	–	ns
Output Enable Setup Time	t_{OES}	10	–	ns
Output Enable Hold Time	t_{OEH}	10	–	ns
Write Enable Pulse Width	t_{WP}	150	–	ns
Data Latch Time	t_{DL}	100	–	µs
Data Setup Time	t_{DS}	70	–	ns
Data Hold Time	t_{DH}	10	–	ns
Data Load Time (Page Write)	t_{PL}	0.05	10	µs
Write Inhibit Time On Power Up	t_{INIT}	4	20	ms

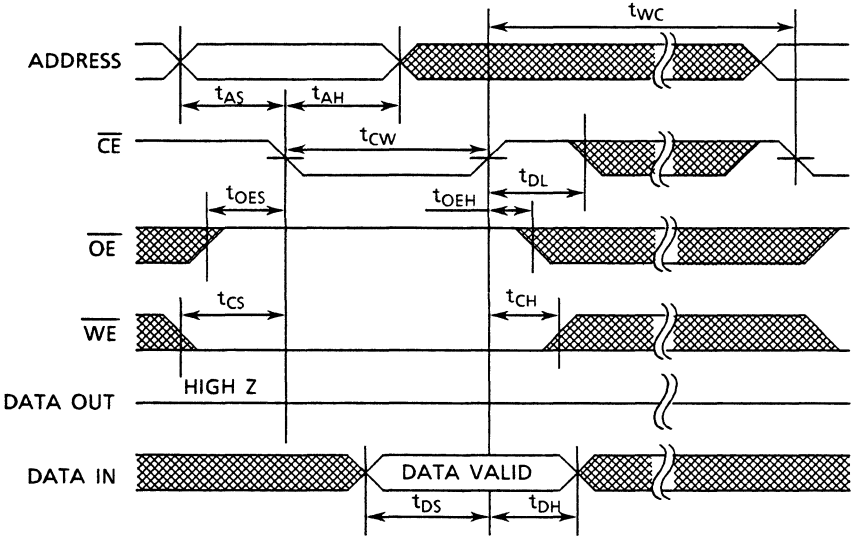
8

BYTE WRITE CYCLE

- CONTROLLED BY $\overline{WE}$

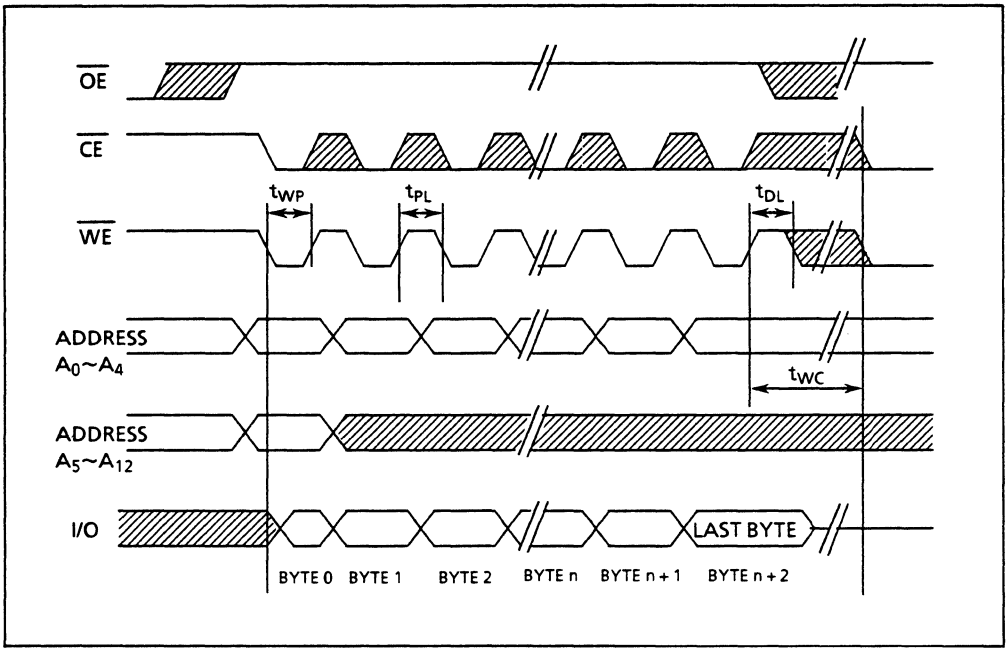


- CONTROLLED BY $\overline{CE}$



8

PAGE WRITE CYCLE



PRELIMINARY

OKI semiconductor
MSM28C256

32Kx8 BIT CMOS ELECTRICALLY ERASABLE & PROGRAMABLE ROM

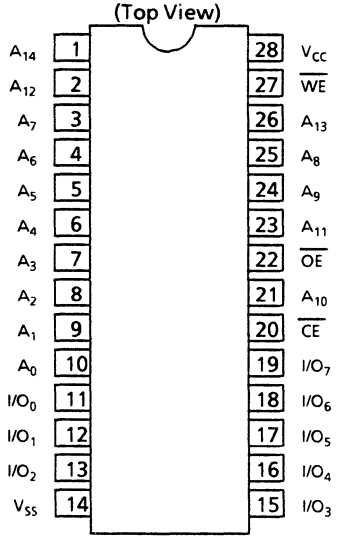
GENERAL DESCRIPTION

The MSM28C256RS is a CMOS electrically erasable and programmable read only memory (E^2PROM) with a capacity of 32,768 words x 8 bits using a single 5V power supply. It features easy use because it operates with a single 5V power supply and its operation timing is similar to that of a static RAM. The automatic page write allows the system to write up to 64 bytes during a single write cycle, providing an effective byte cycle of 156µs/byte. MSM28C256 also supports DATA polling and toggle bit to indicate the early completion of a write cycle.

FEATURES

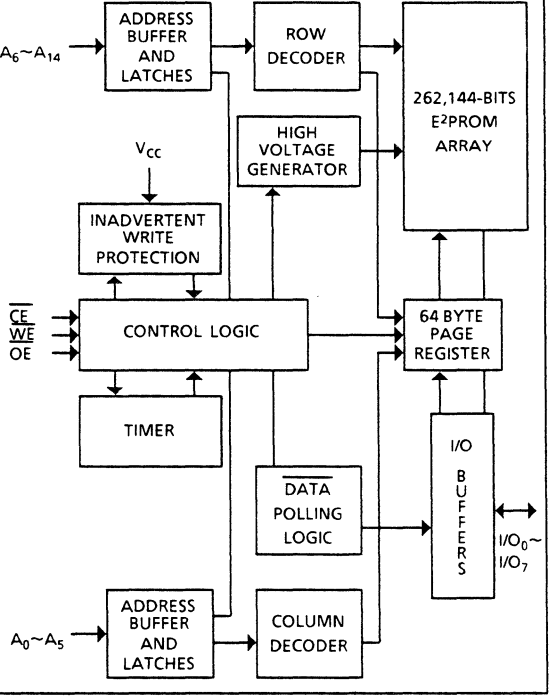
- Access time 200 ns
- Power Dissipation: I_{CCA} 60mA MAX, I_{CCS} 100µA MAX
- 5 volt-only operation including write mode
- Automatic page write 1 to 64 bytes in 10 ms max.
- Detection of Write Completion — Data Polling, Toggle Bit
- Software Write Protection
- TTL compatible inputs and outputs
- 10,000 rewrites per byte
- 10 years data retention
- JEDEC standard approved byte wide pinout

PIN CONFIGURATION



A_0~A_{14} : ADDRESS INPUTS
I/O_0~I/O_7 : DATA I/O
CE : CHIP ENABLE
OE : OUTPUT ENABLE
WE : WRITE ENABLE
V_{CC} : V_{CC} POWER SUPPLY
V_{SS} : GROUND

FUNCTION BLOCK DIAGRAM



8

ASMP

9 ASMP

MSM514212	5k x 8 Line Memory	681
MSM514221	262,263-Word x 4-Bits Field Memory	692
MSM514252	262,144-Word x 4-Bits Multi-port DRAM	700
MSM51C262	65,536-Word x 4-Bits Multi-port DRAM	727
MSM514201	1,048,576-Word x 1-Bits Serial Register	757

PRELIMINARY

OKI semiconductor
MSM514212

5KX8 LINE MEMORY

GENERAL DESCRIPTION

The MSM514212 is a high speed FIFO line memory organized as 5048 words by 8 bits. OKI's 1 micron CMOS technology and advanced circuit design architecture provide higher speed access time and lower power consumption.

The MSM514212 design incorporates well experienced 1M DRAM cell fro main memories. This allows the MSM514212 high performance and high reliability.

The MSM514212's first read/write bit just after read/write reset operation requires no extra waiting time for synchronized access. This enables the MSM514212 continuous uniform synchronized access.

The MSM514212's read and write operations are independent and asynchronous. So, the MSM514212 allows system design wide flexibility.

The MSM514212 has the applications as one line delay device for fast facsimiles and digital copy machines, buffer memory for machines having different system clock cycles, and synchronize clock standarizer memory for memories controled by multi-inputs.

Having 28ns fact cycle time, the MSM514212 can also be applied as digital line memory for NTSC, PAL and SEC AM video systems having 8 fsc cycle time.

The MSM514212 provides variable delay bits, from 40 bits to 5048 bits. The wide range variable delay bits is convenient when more than one line bits delay is required for noise reduction or digital filter of VTR, IDTV, ED TV and HDTV systems.

FEATURES

- Capacity : 5048 x 8 bits
- Access : I/O asynchronous
- Access time : 28 nsec (MIN.)
- Cycle time : 28 nsec (MIN.)
- Delay bits : Variable (40-5048)
- Package : 400 mil 28 pin ZIP
- Current consumption : 120 mA (MAX.)
- Operating voltage range : 4.5V~5.5V
- Operating temperature range : 0°C~70°C

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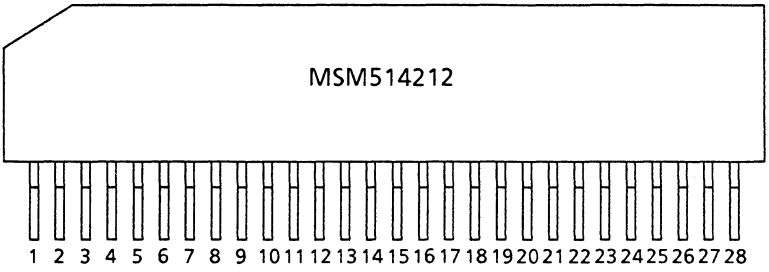
PIN CONFDIGURATION



1.	GND	: Ground	15.	RCK	: Read clock
2.	GND	: Ground	16.	GND	: Ground
3.	DIN3	: Data input	17.	DOUT4	: Data output
4.	DIN2	: Data input	18.	DOUT5	: Data output
5.	DIN1	: Data input	19.	DOUT6	: Data output
6.	DIN0	: Data input	20.	DOUT7	: Data output
7.	VCC	: Power supply	21.	VCC	: Power supply
8.	DOUT0	: Data output	22.	$\overline{WE}$	: Write enable
9.	DOUT1	: Data output	23.	$\overline{WR}$	: Write address reset
10.	DOUT2	: Data output	24.	DIN7	: Data input
11.	DOUT3	: Data output	25.	DIN6	: Data input
12.	GND	: Ground	26.	DIN5	: Data input
13.	$\overline{RR}$	: Read address reset	27.	DIN4	: Data input
14.	$\overline{RE}$	: Read enable	28.	WCK	: Write clock

MSM514212 PIN DESCRIPTION

Symbol	Function
DO0~DO7	Data output. Access time is measured from RCk rising edge.
DI0~DI7	Data in. Input setup-time and hold-time is measured from WCK rising edge.
RCK	Read clock. Read operation occurs synchronized with RCK clocks when $\overline{RE}$ level is low when read operation, read address pointer incremention also occurs.
$\overline{RE}$	Read enable. Output operation is prohibited synchronized with RCK when $\overline{RE}$ level is high. Then, read address pointer is stopped. When $\overline{RE}$ level is low, output operation is enabled.
$\overline{RR}$	Read address pointer reset. Read address pointer is reset synchronized with RCK when $\overline{RR}$ is low. $\overline{RR}$ setup time and hold time are measured form RCK rising edge. When delay bit number comes to 5048, read address pointer is automatically reset.
WCK	Write clock. Write operation is prohibitted synchronized with WCK when $\overline{WE}$ level is high. Then, write address pointer is stopped. When $\overline{WE}$ level is low, input operation is enabled.
$\overline{WE}$	Write enable. Input operation is prohibited synchronized with WCK when WE level is high. Then, write address pointer is stopped. When $\overline{WE}$ level is low, input operation is enabled.
$\overline{WR}$	Write address pointer reset. Write address pointer reset operation starts at the WCK rising edge when $\overline{WR}$ level is low. $\overline{WR}$ setup time and hold time are measured from WCK riisng edge. When delay bit number comes to 5048, write address pointer is automatically reset.
VCC	Power supply. (+ 5V)
GND	Ground.

ELECTRICAL CHARACTERISTICS

• Absolute Maximum Ratings

Rating	Symbol	Conditions	Value	Unit
Pin voltage relative to Vss	V_T		− 1.5~ + 7.0	V
Supply voltage	V_{CC}		− 1.5~ + 7.0	V
Circuit output current	I_O		20	mA
Operating temperature	Topt		0~70	°C
Storage temperature	Tstg		− 55~ + 125	°C

• Recommended Operating Condition

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply voltage	V_{CC}		4.5	5.0	5.5	V
Input high voltage	V_{IH}		2.4		5.5	V
Input low voltage	V_{IL}		− 1.5		0.8	V
Temperature around	Ta		0		+ 70	°C

• DC Characteristics (on the recommended operating conditions)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Power supply current	I_{CC}				120	mA
Input leakage current	I_I	V_I = 0~V_{CC}, Other pins are 0V	− 10		10	µA
Output leakage current	Io	Vo = 0~5.5V, DOUT high inpedance	− 10		10	µA
Output high level voltage	V_{OH}	I_{OH} − 1mA	2.4			V
Output low level voltage	V_{OL}	I_{OL} = 2mA			0.4	V

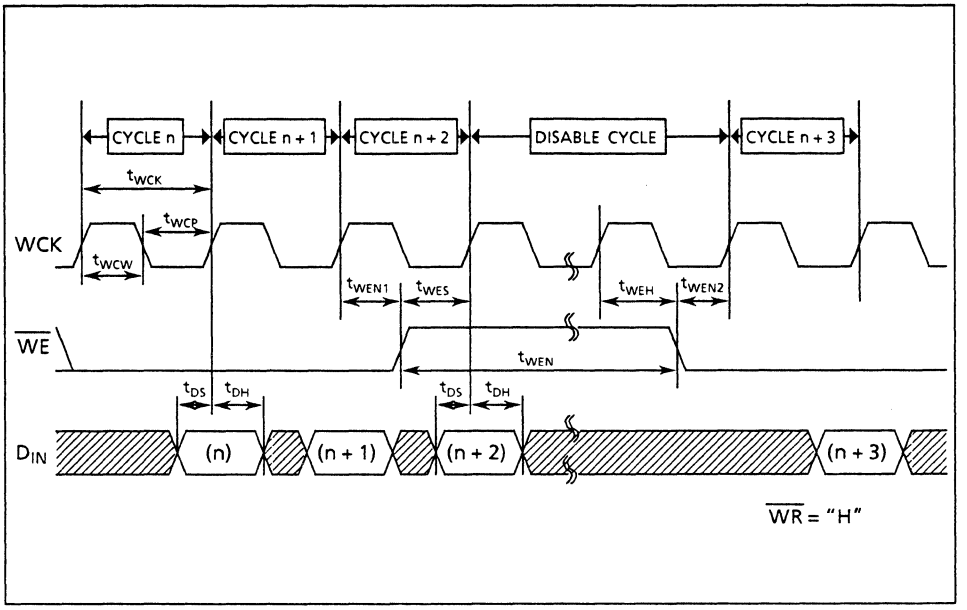
• Capacitance (Ta = 25 'C, f = 1 MHz)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Input capacitance	C_I				5	pF
Output capacitance	C_O				7	pF

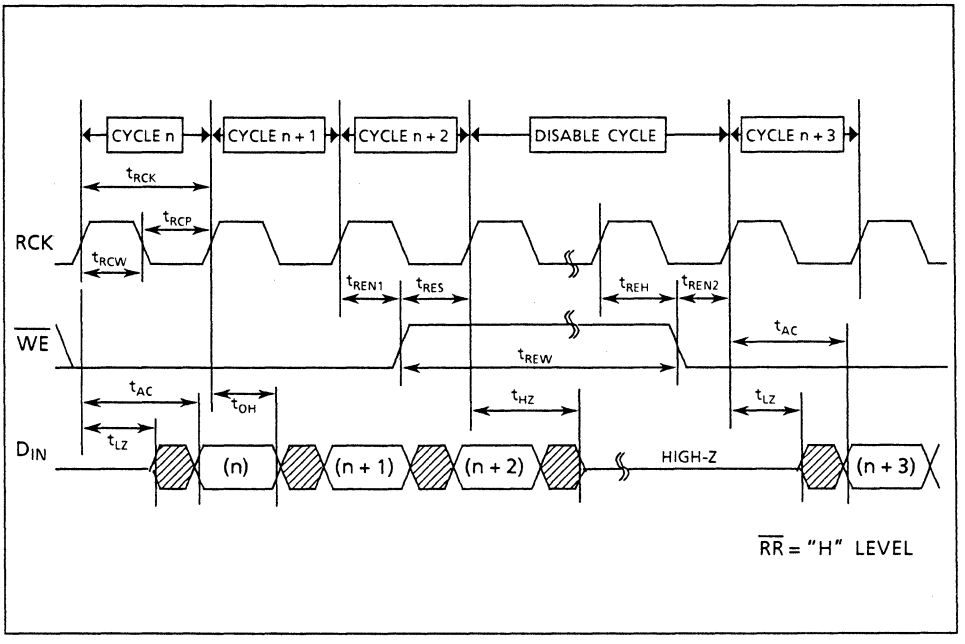
•AC Characteristics - On the recommended operating conditions

Parameter	Symbol	514212-28		514212-34		514212-50		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Write clock cycle time	t_{WCK}	28	1090	34	1090	50	1090	ns
Write clock pulse width	t_{WCW}	11		14		20		ns
Write clock precharge time	t_{WCP}	11		14		20		ns
Read clock cycle time	t_{RCK}	28		34		50		ns
Read clock pulse width	t_{RCW}	11		14		20		ns
Read clock precharge time	t_{RCP}	11		14		20		ns
Access time	t_{AC}		28		34		40	ns
Cycle access time right after reset	t_{ACR}		28		34		40	ns
Output hold time	t_{OH}	5		5		5		ns
Output hold time right after reset	t_{OHR}	5		5		5		ns
Output low impedance period	t_{LZ}	5	28	5	34	5	40	ns
Output high impedance period	t_{HZ}	5	28	5	34	5	40	ns
Input data setup time	t_{DS}	11		14		15		ns
Input data hold time	t_{DH}	5		5		5		ns
$\overline{WR}/\overline{RR}$ setup time from WCK/RCK	t_{RS}	11		14		15		ns
$\overline{WR}/\overline{RR}$ hold time from WCK/RCK	t_{RH}	5		5		5		ns
$\overline{WR}/\overline{RR}$ nonselective time 1 from WCK/RCK	t_{RN1}	5		5		5		ns
$\overline{WR}/\overline{RR}$ nonselective time 2 from WCK/RCK	t_{RN2}	11		14		15		ns
$\overline{WE}$ setup time from WCK	t_{WES}	11		14		15		ns
$\overline{WE}$ hold time from WCK	t_{WEH}	5		5		5		ns
$\overline{WE}$ nonselective time 1 from WCK	t_{WEN1}	5		5		5		ns
$\overline{WE}$ nonselective time 2 form WCK	t_{WEN2}	11		14		15		ns
$\overline{RE}$ setup time from RCK	t_{RES}	11		14		15		ns
$\overline{RE}$ hold time from RCK	t_{REH}	5		5		5		ns
$\overline{RE}$ nonselective time 1 from RCK	t_{REN1}	5		5		5		ns
$\overline{RE}$ nonselective time 2 from RCK	t_{REN2}	11		14		15		ns
$\overline{WE}$ high level period	t_{WEW}	0		0		0		ns
$\overline{RE}$ high level period	t_{REW}	0		0		0		ns
$\overline{WR}$ low level period (Write reset period)	t_{RSTW}	0		0		0		ns
$\overline{WR}$ low level period ;(Read reset period)	t_{RSTR}	0		0		0		ns
Transition time	t_T	3		3		3		ns

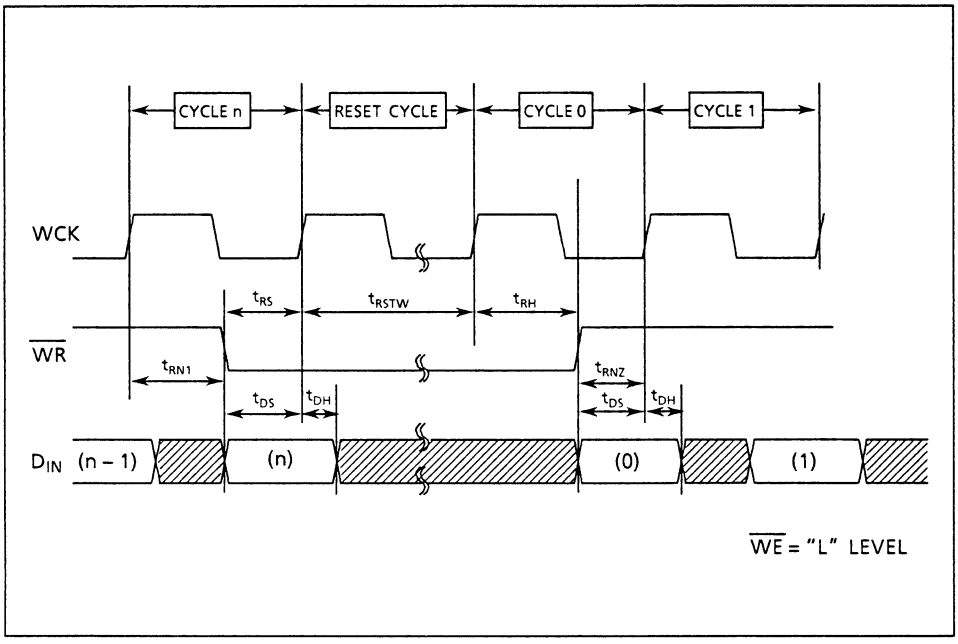
WRITE CYCLE



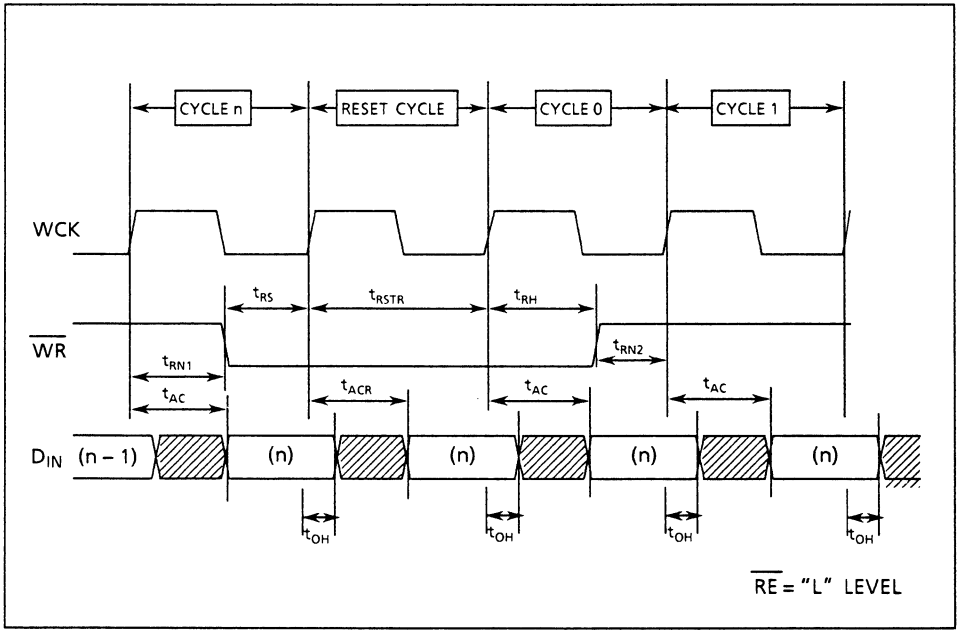
READ CYCLE



WRITE RESET CYCLE



READ RESET CYCLE



NOTE: Read/Write reset cycle is not necessarily required

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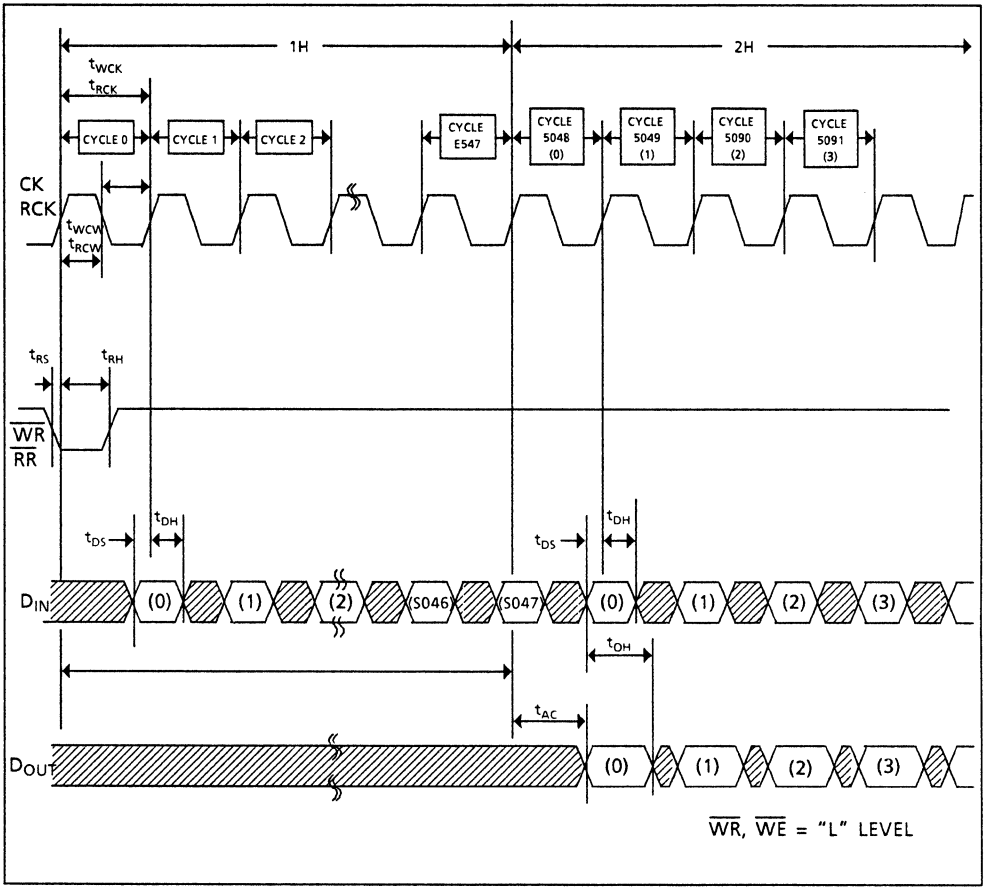
1H DELAY TIMING



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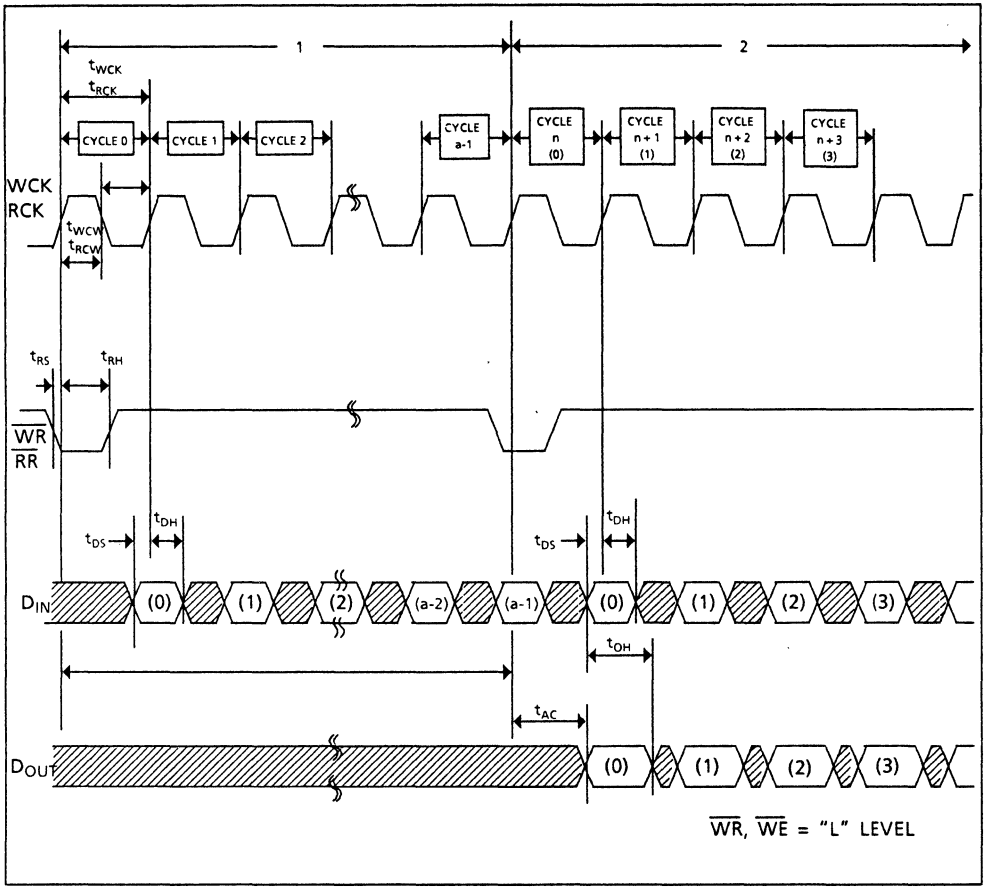
n bit DELAY TIMING (1)



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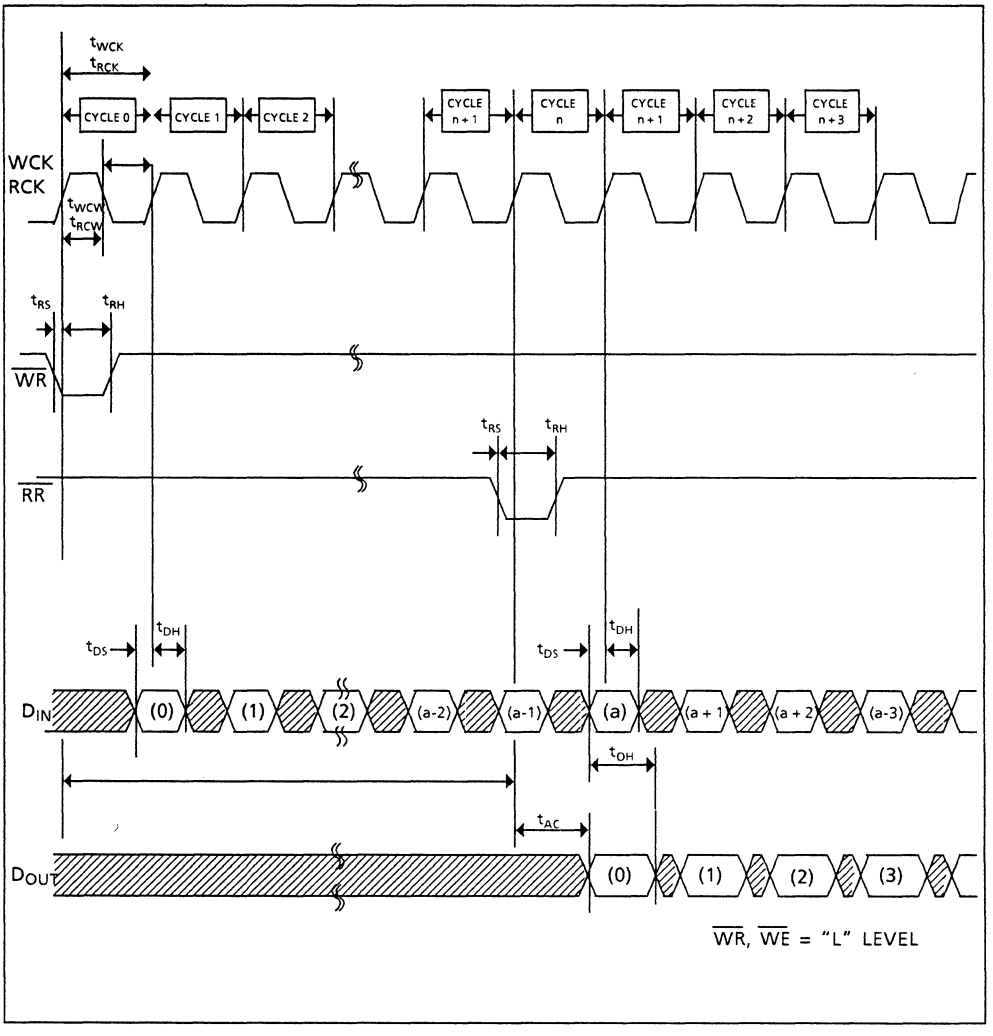
n bit DELAY TIMING (2)



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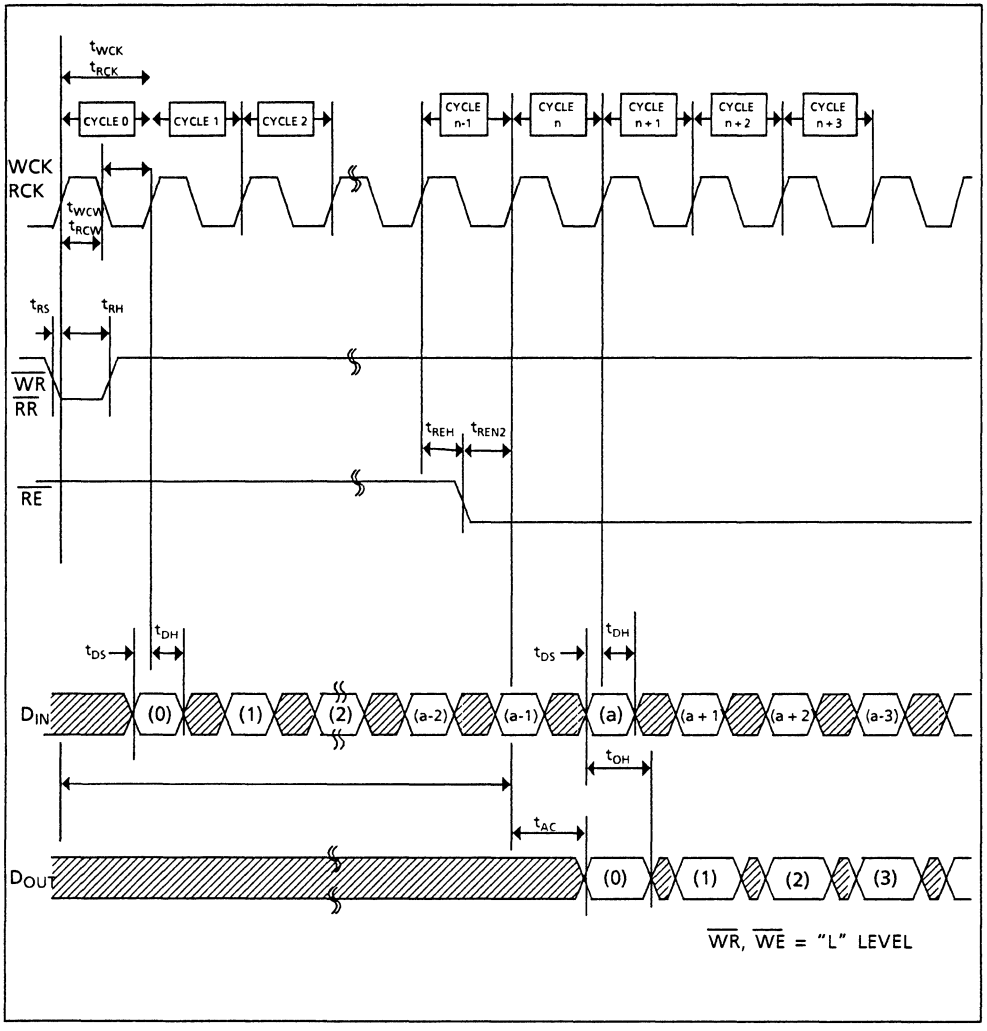
n bit DELAY TIMING (3)



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OKI semiconductor
MSM514221

262, 263 words X 4 bits field memory

GENERAL

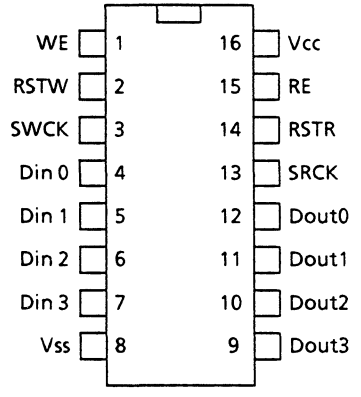
MSM514221 is a CMOS dynamic memory device organized as 256K + 120 words by 4 bits; it is a serial access memory that performs high speed, asynchronous read/write operation. It is used mainly for fields of digital TV/VTR that requires higher speed operation, lower power consumption, and larger capacity. Minimizing its external control pins allows itself to be packaged in a standard, plastic 300mil 16PIN-DIP.

Serial read/write operation of MSM514221 can be separately controlled asynchronously and in a different clock rate with dedicated clock. Also, access time and read/write cycle time synchronizes with the clock, and its execution can be standard immediately with any address without wait time. MSM514221 has a built-in, self refresh control circuit, which requires no external refersh.

FEATURES

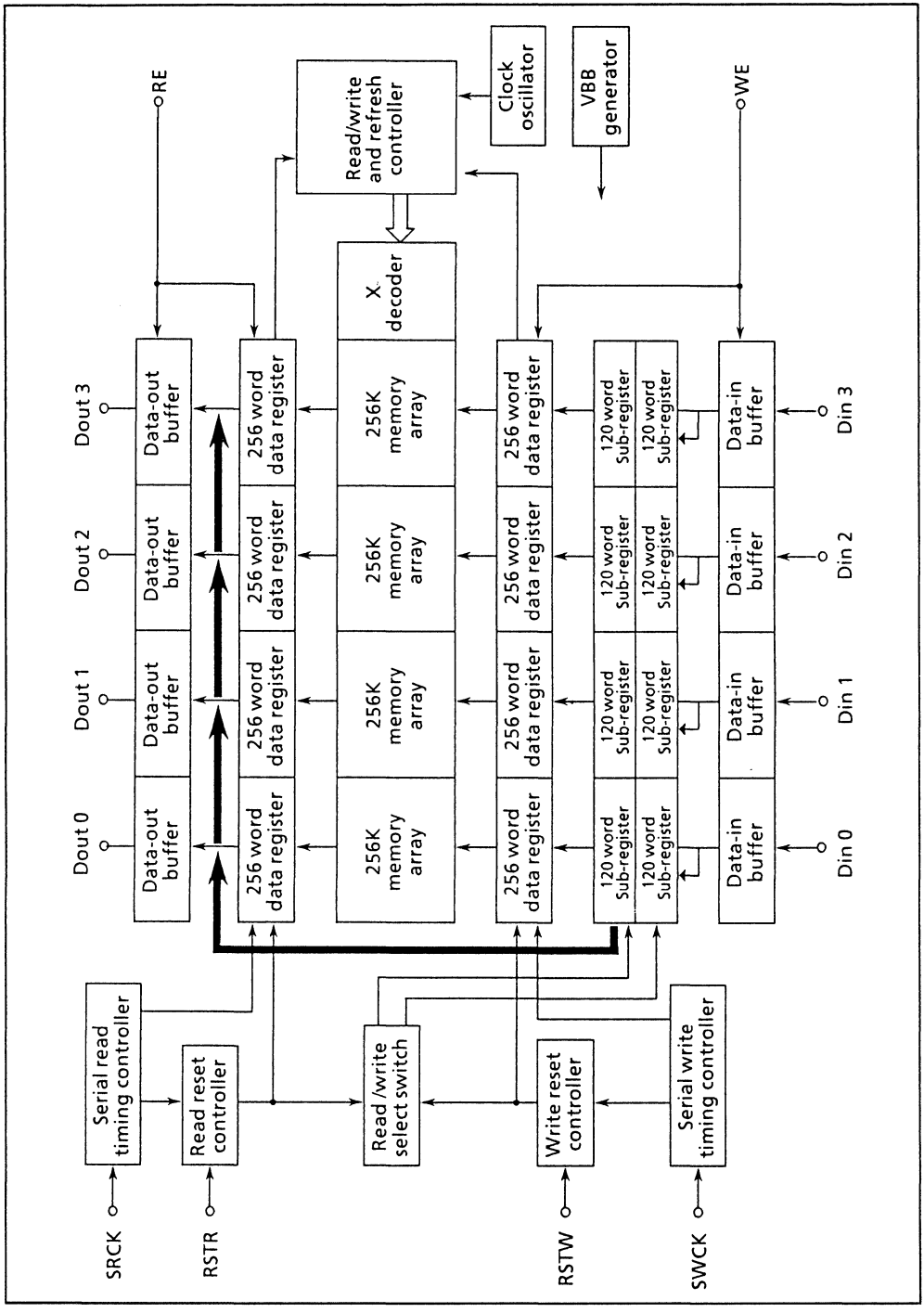
- 512 x 512 x 4 bit organization
- High speed FIFO operation
  - Serial access time 25nS/30nS
  - Serial read/write cycle time 30nS/60nS
- Low power consumption 275 mW max. at the highest speed
- Power voltage single 5V ± 10%
- 16PIN 300mil width, plastic DIP
- 1.2μm standard CMOS DRAM process
- TI's TMS4C1050 compatible

PIN CONFIGURATION



SWCK		:	serial write clock
SRCK		:	serial read clock
WE		:	write enable
RE		:	read enable
RSTW		:	reset write
RSTR		:	reset read
Din	0-3	:	data input
Dout	0-3	:	data output
Vcc		:	power supply (+ 5V)
Vss		:	ground

BLOCK DIAGRAM



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PIN FUNCTION

- **Data input (Din 0-3)**

  Used for serial data input.

- **Data output (Dout 0-3)**

  Used for serial data output.

- **Reset write (RSTW)**

  Used as a reset input pin for initializing (return to address 1) write address pointer.

- **Reset read (RSTR)**

  Used as a reset input pin for initializing (return to address 1) read address pointer.

- **Write enable (WE)**

  When this pin is at "L" level, write operation is disabled, and the internal write address pointer remains unchanged regardless of the SWCK input.

- **Read enable (RE)**

  When this pin is at "L" level, read operation is disabled, and the internal read address pointer remains unchanged regardless of the SRCK input. The output becomes high impedance stage.

- **Serial write clolck (SWCK)**

  Clock input to this pin executes write operation.
  The write operation synchronizes with serial write clock while the WE is at "H" level; internal write address pointer is also incremented simultaneously.

- **Serial read clolck (SRCK)**

  Clock input to this pin executes read operation.
  The read operation synchronizes with serial read clock while the RE is at "H" level; internal read address pointer is also incremented simultaneously.

OPERATION MODE

- **Write cycle**

  Write operation is executed synchronizing with SWCK clock when WE is enabled (at "H" level). At this time make sure to perform RSTW operation first to initialize internal circuit. When finishing write operation, make sure to RSTW operation first to transfer the last data to memory cell. At this time, disable WE ("L") and perform RSTW operation to properly transfer data to the last address. If the RSTW operation is performed with WE enabled ("H") the data is not written on the last address but on the first address.

- **Read cycle**

  Read operation is executed synchronizing with SRCK clock when RE is enabled (at "H" level).
  At this time make sure to perform RSTR operation first to initialize internal circuit.

- **Power up**

  To perform normal memory operation, start operation with more than 100 μsec of a pause after Vcc has reached the specified voltage after the power up. AT this time, execute RSTW and RSTR operation, and perform initialization of each pointer since the locations of internal read address pointer and write address pointer have not been fixed. After reset operation, data read/write operation can be started with the first address (address 1).

- **Read access of new data**

  In reading new data (when the written data is read immediately after the write operation), the difference between read address and write address must not be less than 600, and not be more than 262, 263.

- **Read access of old data**

  In reading old data (where the data written before the writing operation is read), the difference between read address and write address must be within zero and 119.

ELECTRICAL CHARACTERISTICS

- **Absolute maximum rating**

Description	Symbol	Conditions	Ratings
Pin voltage	VT	at TA = 25°C, Vss	-1.0~7.0V
Output short circuited current	I_{OS}	TA = 25°C	50 mA
Allowable power loss	PD	TA = 25°C	1W
Operation temperature	Top	-	0~70°C
Storage temperature	Tstg	-	- 55~150°C

- **Recommended operation condition**

Description	Symbol	MIN.	TYP.	MAX.	Unit
Power voltage	Vcc	4.5	5.0	5.5	V
Power voltage	Vss	0	0	0	V
Input "H" voltage	V_{IH}	2.4	Vcc	Vcc + 1	V
Input "L" voltage	V_{IL}	- 1.0	0	0.8	V

- **Direct current characteristics**

Description	Symbol	Measuring condition	MIN.	MAX.	Unit
Output "H" voltage	V_{OH}	IOH = - 5mA	2.4		V
Output "L" voltage	V_{OL}	IOL = 4.2mA		0.4	V
Input leak current	I_{LI}	0<VI<Vcc + 1, other input 0V	- 10	10	µA
Output leak current	I_{LO}	0<VO<5.5V	- 10	10	µA
Power current (operating)	Icc1	t_{RC} = min		50	mA
Power current (waiting)	Icc2	Input pin = V_{IL}/V_{IH}		5	mA

- **Pin capacity**

(Ta = 25°C, f = 1MHz)

Description	Symbol	MAX.	Unit
Input capacitance (Din, SWCK, SRCK, RSTW, RSTR, WE, RE)	Ci	7	pF
Output capacitance (Dout)	Co	7	pF

- **Alernate current characteristics**

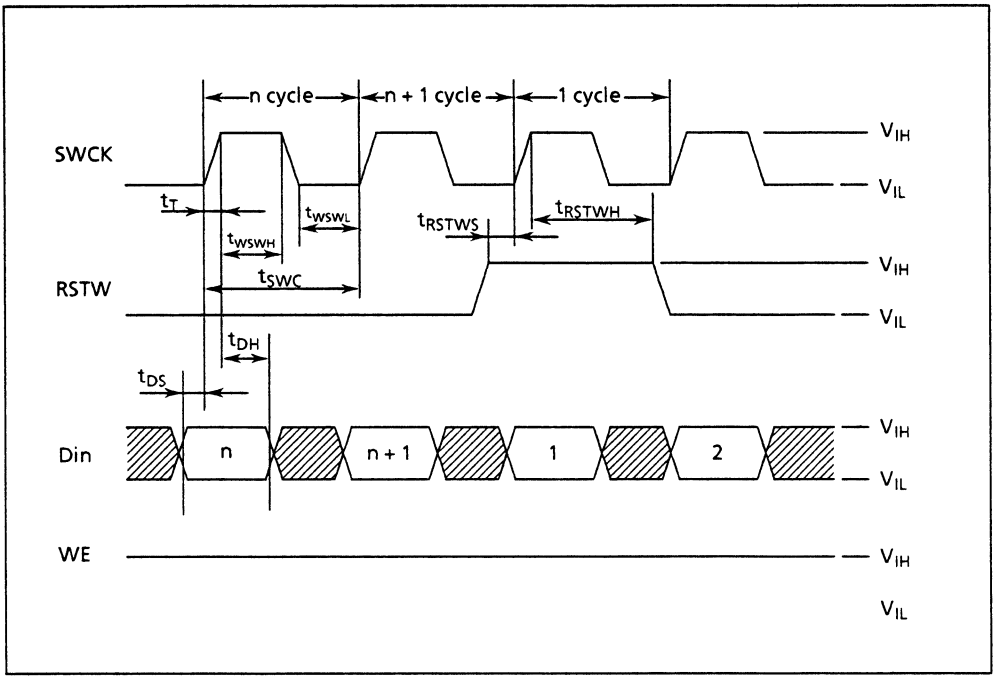
(Vcc = 5V ± 10%, Ta = 0~70°C)

Description	Symbol	MSM514221-3		MSM514221-6		Unit
		MAX.	MAX.	MIN.	MAX.	
Dout access time from SRCK	t_{AC}		25		30	ns
Dout hold time from SRCK	t_{DDCK}	10		15		ns
Dout hold time from RE	t_{DDRE}	13		18		ns
SWCK "H" pulse width	t_{WSWH}	12		17		ns
SWCK "L" pulse width	t_{WSWL}	12		17		ns
Input data setup time	t_{DS}	0		0		ns
Input data hold time	t_{DH}	10		15		ns
Write instruction setup time	t_{WCS}	0		0		ns
Write instruction hold time	t_{WCH}	0		0		ns
WE "L" pulse width	t_{WWE}	5n		10n		s
RSTW setup time	t_{RSTWS}	0		0		ns
RSTW hold time	t_{RSTWH}	10		15		ns
SRCK "H" pulse width	t_{WSRH}	12		17		ns
SRCK "L" pulse width	t_{WSRL}	12		17		ns
Read instruction setup time	t_{RCS}	0		0		ns
Read instruction hold time	t_{RCH}	0		0		ns
RE "L" pulse width	t_{WRE}	5n		10n		s
RSTR setup time	t_{RSTRS}	0		0		ns
RSTR hold time	t_{RSTRH}	10		15		ns
SWCK cycle time	t_{SWC}	30n		60n		s
SRCK cycle time	t_{SRC}	30n		60n		s
Rise time and fall time	t_T	3	30	3	30	ns

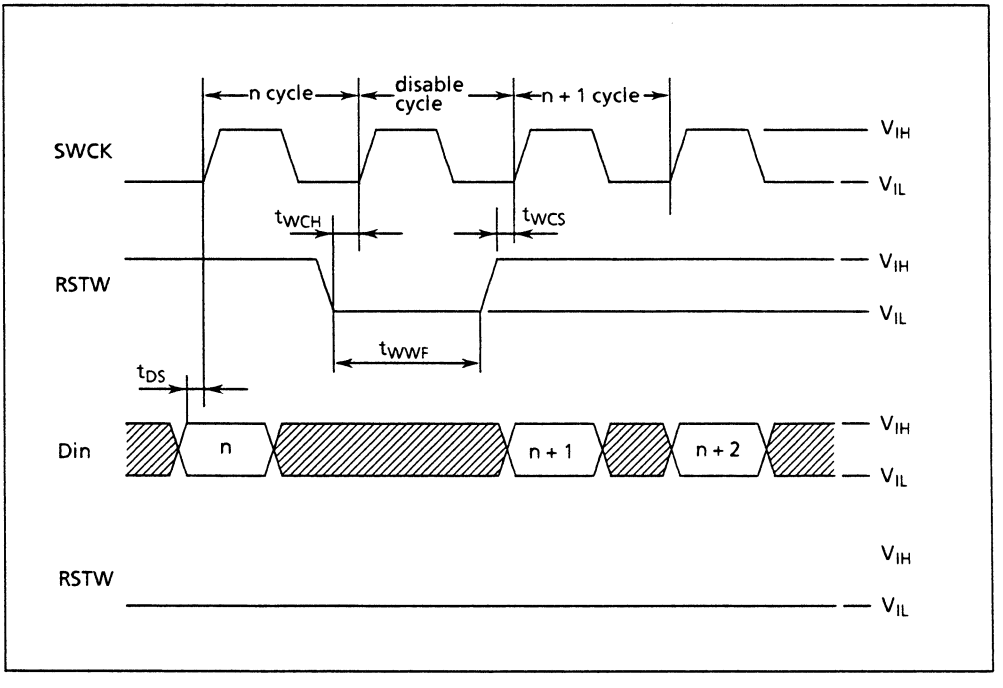
(Note)

1. The input voltage reference levels stipulated in the timing specification are V_{IH} = 2.4V and V_{IL} = 0.8V. The tT is a transition time betwen V_{IH} = 2.4V and V_{IL} = 0.8V.
2. Rise and fall times Tt of all the cycles is specified as 3ns.
3. During asynchronous execution of write and read, the difference between write address and read address should not be less than 600.
4. To read data that was written during a cartain cycle, read cycle should be executed with an address difference more than 600. However, if the read address is less than 119, compared with the write address, the old write address is output.
5. Where the read address is, compared with the write address, between 120 and 599 and if it is not less than 262, 263, there is not guarantee in the output data.

Write Cycle Timing (Reset Write)

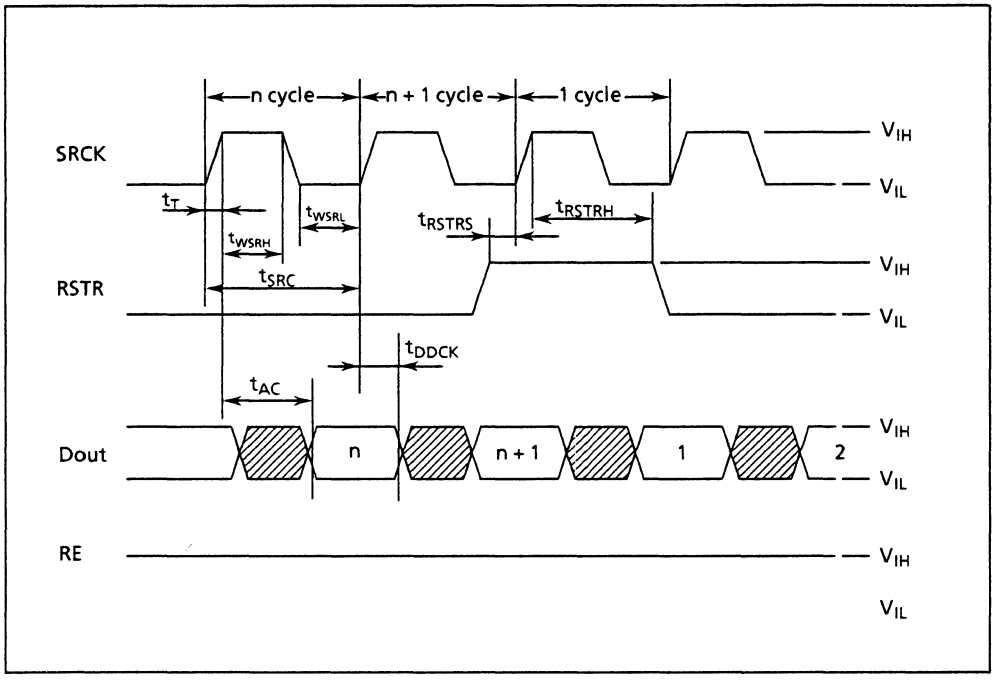


Write Cycle Timing (Write Enable)

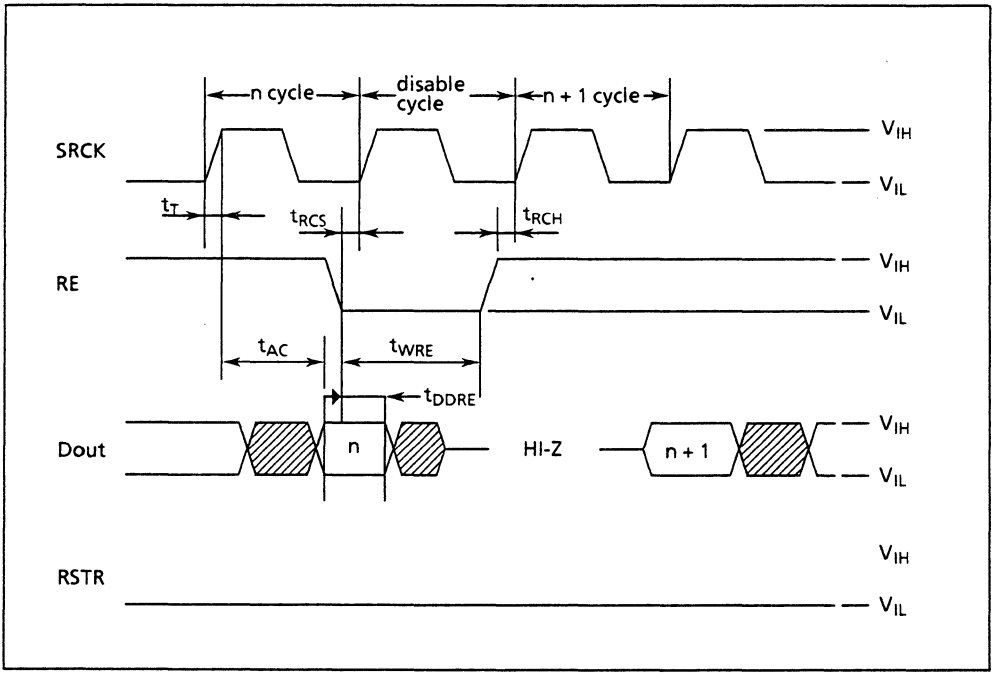


9

Read Cycle Timing (Reset Read)



Read Cycle Timing (Read Enable)



9

OKI semiconductor
MSM514252

262, 144 words X 4 bits Multi-port DRAM

< Fast Page Mode >

DESCRIPTION

The OKI MSM514252 is a high speed 1M bits Multi-port Dynamic Randam Access Memory designed especially for high performance graphics applications. The multiport DRAM consists of a 256K x 4 bits DRAM port with multiplexed addresses and a 512 x 4 bits serial Read/Write port.

The multi-port DRAM uses OKI's N-well CMOS process combined with silicide technology and a single transister dynamic storage cell. The technology provides wide operating margins as well as high density and low power dissipation.

In addition to the conventional 1 megabit random access port which has fast page operation mode, the multi-port DRAM has a second fast serial access read/write port with a clock rate of 33MHz for driving a video-type display.

The multiport DRAM has an internal 512 X 4 bits shift register which can be parallel loaded with an entire row of data from sense amps in a special cycle which is referred to as the Read Data Transfer Cycle. Data is shifted out via the serial port for screen refresh, independent of the random access port. The shift register is also used to write 512 X 4 bits of data to connected sense amps in a special cycle which is referred to as the Write Transfer Cycle. Serial read and random read/write operation can occur simultaneously except when the serial shift register load operation must be synchronized with any random access port operations. Serial write and random read/write operations can occur except in a Write Data Transfer cycle.

The 512 X 4 bits shift register can supply a constant 33 MHz, four-bit wide data stream. The shift register requires no refresh operation because it uses static CMOS flip-flops.

FEATURES

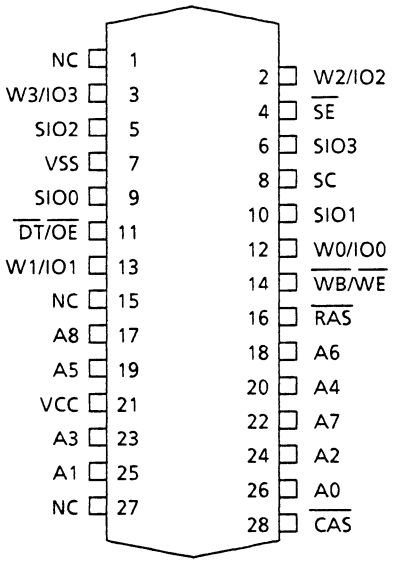
9

- Dual Port
  - RAM port : 256K words X 4 bits
  - SAM port : 512 words X 4 bits
- Fast Access
  - RAM port :Cycle time 190 ns (MIN)
    :Access time 100 ns (MAX)
  - SAM port :Cycle time 30 ns (MIN)
    :Access time 30 ns (MAX)
- Asynchronous Operation (Except during data transfer period)
- Bidirectional Data Transfer
  - Read Data Transfer:
    From RAM array to data register
  - Write Data Transfer:
    From data register to RAM array
  - Pseudo Write Data Transfer:
    No data transfer from data register to RAM array
- Pointer Control
  - Addressable serial read/write start bit

FEATURES (Continued)

- Write Per Bit
  - Write mask to any combination of the 4 bits on the random access pins
- Continuous Serial Read
  - Real time data transfer from the RAM array to the data register
- Fast Page Mode
  - Fast Page Cycle : 55 ns (MIN)
  - $\overline{CAS}$ Access Time: 35 ns (MAX)
- Refresh Capabilities
  - $\overline{RAS}$ Only Refresh Mode: 512 cycle/8 ms
  - Hidden Refresh Mode
  - $\overline{CAS}$ before $\overline{RAS}$ Refresh Mode
- Full TTL Compatibility
- Single Power supply
  - 5V ± 10%
- JEDEC Pinout
  400 mil 28 pin ZIP

PIN OUT

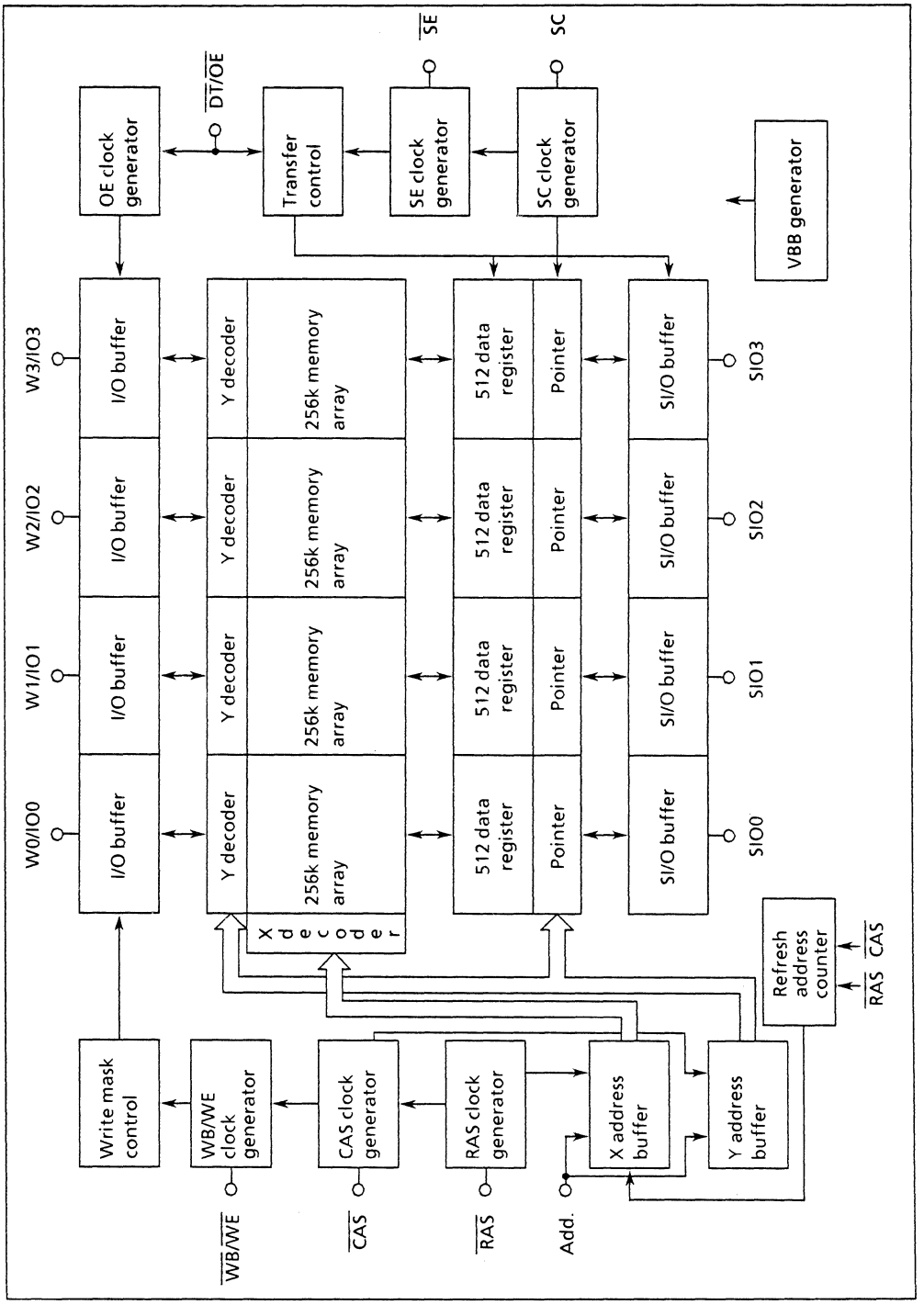


28 PIN ZIP

SC	=	SERIAL CLOCK
SIO0-3	=	SERIAL DATA IN, DATA OUT
DT/OE	=	DATA TRANSFER ENABLE, DRAM OUTPUT ENABLE
IO0-3	=	DRAM DATA IN, DATA OUT
WB/WE	=	WRITE PER BIT/WRITE ENABLE
NC	=	NO CONNECTION
RAS	=	ROW ADDRESS STROBE
A0-8	=	ADDRESS INPUT
VCC	=	POWER (+ 5V)
VSS	=	GROUND
SE	=	SERIAL ENABLE
CAS	=	COLUMN ADDRESS STROBE

9

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply Voltage		-1~7	V
Vi	Input Voltage	With respect to Vss, Ta = 25°C	-1~7	V
Vo	Output Voltage		-1~7	V
Io	Output Current	Ta = 25°C	50	mA
Pd	Power Dissipation	Ta = 25°C	1000	mW
Topr	Operating Temperature		0~70	°C
Tstg	Storage Temperature		-55~150	°C

CAPACITANCE (Ta = 25°C, f = 1MHz, Vi = 25mVrms)

Symbol	Parameter	Min	Max	Unit
C_{IN1}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, SC, $\overline{SE}$, $\overline{DT/OE}$		8	pF
C_{IN2}	A0-A7		5	pF
C_{IO1}	I/O0-3, SIO0-3		7	pF

RECOMMENDED OPERATING CONDITIONS

(Ta = 0~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
Vcc	Supply Voltage	4.5	5	5.5	V
Vss	Supply Voltage	0	0	0	V
V_{IH}	High-level Input voltage, all inputs	2.4		Vcc + 1	V
V_{IL}	Low-level Input voltage, all inputs	-1		0.8	V

*All input voltages are with respect to Vss

DC CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage	I_{OH} = -2mA	2.4		Vcc	V
V_{OL}	Low-level output voltage	I_{OL} = 4.2mA	0		0.4	V
I_{LO}	Off-state output current	Output nonactive, 0V ≦ Vout ≦ 5.5V	-10		10	uA
I_{LI}	Input current	0V ≦ Vin ≦ Vcc, Other input pins = 0V	-10		10	uA

* Current flowing into an IC is positive, out is negative

DC CHARACTERISTICS (Cont.)

Symbol	Parameter		MSM514252		Unit
			-10	-12	
	RAM port	Serial I/O port	Max	Max	
Icc1(AV)	Random R/W cycle ($\overline{RAS}$, $\overline{CAS}$ Address cycling, tRC = tRC (min))	Standby (SC = V_{IL})	70	60	mA
Icc2**	Standby ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, Dout = HZ)	Standby (SC = V_{IL})	5	5	mA
Icc3(AV)	$\overline{RAS}$ only refresh cycling ($\overline{CAS}$ = V_{IH}, tRC = tRC (min))	Standby (SC = V_{IL})	70	60	mA
Icc4(AV)	Page mode cycle, ($\overline{RAS}$ = V_{IL}, tPC = tPC(min) $\overline{CAS}$ cycling)	Standby (SC = V_{IL})	45	35	mA
Icc5(AV)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$/$\overline{CAS}$ Cycling, (tRC = tRC(min))	Standby (SC = V_{IL})	70	60	mA
Icc6(AV)	Data transfer cycle, ($\overline{DT/OE}$, $\overline{CAS}$ $\overline{RAS}$ cycling, (tRC = tRC(min))	Standby (SC = V_{IL})	75	65	mA
Icc7(AV)	Random R/W cycle ($\overline{RAS}$, $\overline{CAS}$ cycling, tRC = tRC(min))	Active (tSCC = tSCC(min))	120	100	mA
Icc8(AV)	Standby ($\overline{RAS}$ = V_{IH}, Dout = HZ)	Active (tSCC = tSCC(min))	50	40	mA
Icc9(AV)	$\overline{RAS}$ only refresh cycle, ($\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH}, tRC = tRC(min))	Active (tSCC = tSCC(min))	110	90	mA
Icc10(AV)	Page mode cycle ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, tRC = tRC(min))	Active (tSCC = tSCC(min))	100	80	mA
Icc11(AV)	$\overline{CAS}$ before $\overline{RAS}$ refresh ($\overline{RAS}$, $\overline{CAS}$ cycling, tRC = tRC(min))	Active (tSCC = tSCC(min))	110	90	mA
Icc12(AV)	Data transfer cycle $\overline{DT/OE}$, $\overline{RAS}$ $\overline{CAS}$ cycling, tRC = tRC(min))	Active (tSCC = tSCC(min))	125	105	mA

* Icc (AV) is obtained with the output open. (AV) specifies average value.
** If $V_{IH} \geqq$ VccX0.9 and $V_{IL} \leqq$ 0.6V, then Icc2 $\leqq$ 1.5mA.

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TIMING REQUIREMENTS-Dynamic Access (Vcc = 5V ± 10%, Ta = 0-70°C)

Symbol		MSM514252				Unit	Note
		-10		-12			
		MIN.	MAX.	MIN.	MAX.		
tRC	Random read or write cycle time	190	-	220	-	ns	
tRMW	Read modify write cycle time	255	-	295	-	ns	
tPC	Fast page mode cycle time	55	-	70	-	ns	
tPRMW	Fast page mode read/write cycle time	120	-	145	-	ns	
tRAC	Access time from $\overline{RAS}$	-	100	-	120	ns	2.7
tCAC	Access time from $\overline{CAS}$	-	35	-	45	ns	2.7
tAA	Access time from column address	-	50	-	60	ns	2.8
tCPA	Access time from $\overline{CAS}$ precharge	-	50	-	65	ns	2
tCLZ	Output low impedance time from $\overline{CAS}$	5	-	5	-	ns	2
tOFF	Output buffer turn-off delay	0	30	0	35	ns	3
tT	Transition time	3	50	3	50	ns	1
tRP	$\overline{RAS}$ precharge time	80	-	90	-	ns	
tRAS	$\overline{RAS}$ pulse width	100	10,000	120	10,000	ns	
tRSH	$\overline{RAS}$ hold time from $\overline{CAS}$	35	-	45	-	ns	
tCSH	$\overline{CAS}$ hold time from $\overline{RAS}$	100	-	120	-	ns	
tCAS	$\overline{CAS}$ pulse width	35	10,000	45	10,000	ns	
tRCD	$\overline{RAS}$ to $\overline{CAS}$ delay	25	65	25	75	ns	7
tRAD	$\overline{RAS}$ to column address delay	20	50	20	60	ns	
tCRP	$\overline{CAS}$ to $\overline{RAS}$ precharge time	10	-	10	-	ns	
tCPN	$\overline{CAS}$ precharge time	15	-	20	-	ns	
tCP	$\overline{CAS}$ precharge time (Fast page mode)	10	-	15	-	ns	
tASR	Row address set-up time	0	-	0	-	ns	
tRAH	Row address hold time	15	-	15	-	ns	
tASC	Column address set-up time	0	-	0	-	ns	
tCAH	Column address hold time	20	-	25	-	ns	
tRRH	Read command hold time reference to $\overline{RAS}$	0	-	0	-	ns	4
tWP	Write command pulse width	20	-	25	-	ns	
tRWL	Write command to $\overline{RAS}$ load time	25	-	30	-	ns	
tCWL	Write command to $\overline{CAS}$ lead time	25	-	30	-	ns	
tDS	Data-in set-up time	0	-	0	-	ns	5
tDH	Data-in hold time	20	-	25	-	ns	5
tREF	Refresh period (512 cycles: A0~A8)	-	8	-	8	ns	
tWCS	Write command set-up ;time	0	-	0	-	ns	6
tCWD	$\overline{CAS}$ to $\overline{WE}$ delay	75	-	85	-	ns	6

TIMING REQUIREMENTS-Dynamic Access (Vcc = 5V ± 10%, Ta = 0-70°C)

Symbol		MSM514252				Unit	Note
		-10		-12			
		MIN.	MAX.	MIN.	MAX.		
tAWD	Column adress to $\overline{WE}$ delay time	85	-	100	-	ns	6
tCSR	$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	10	-	10	-	ns	
tCHR	$\overline{RAS}$ to $\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	30	-	30	-	ns	
tRPC	$\overline{CAS}$ active delay from $\overline{RAS}$ precharge	10	-	10	-	ns	
tOEA	Access time from $\overline{OE}$	-	35	-	45	ns	
tOED	$\overline{OE}$ delay time	25	-	30	-	ns	
tOEZ	$\overline{OE}$ to data output buffer turn-off delay	0	25	0	30	ns	3
tWCH	Write command hold time	20	-	25	-	ns	
tOEH	$\overline{OE}$ command hold time	25	-	30	-	ns	
tRCS	Read command set-up time	0	-	0	-	ns	
tRCH	Read command hold time	0	-	0	-	ns	4
tAR	Column address hold time from $\overline{RAS}$	75	-	90	-	ns	
tRAL	$\overline{RAS}$ read time from column address	50	-	60	-	ns	
tWCR	Write command hold time from $\overline{RAS}$	75	-	90	-	ns	
tDHR	Data-in hold time from $\overline{RAS}$	75	-	90	-	ns	
tRWD	$\overline{RAS}$ to $\overline{WE}$ delay	135	-	160	-	ns	
tROH	$\overline{RAS}$ hold time reference to $\overline{OE}$	20	-	20	-	ns	

TIMING REQUIREMENTS-Serial Access (Vcc = 5V ± 10%, Ta = 0-70°C)

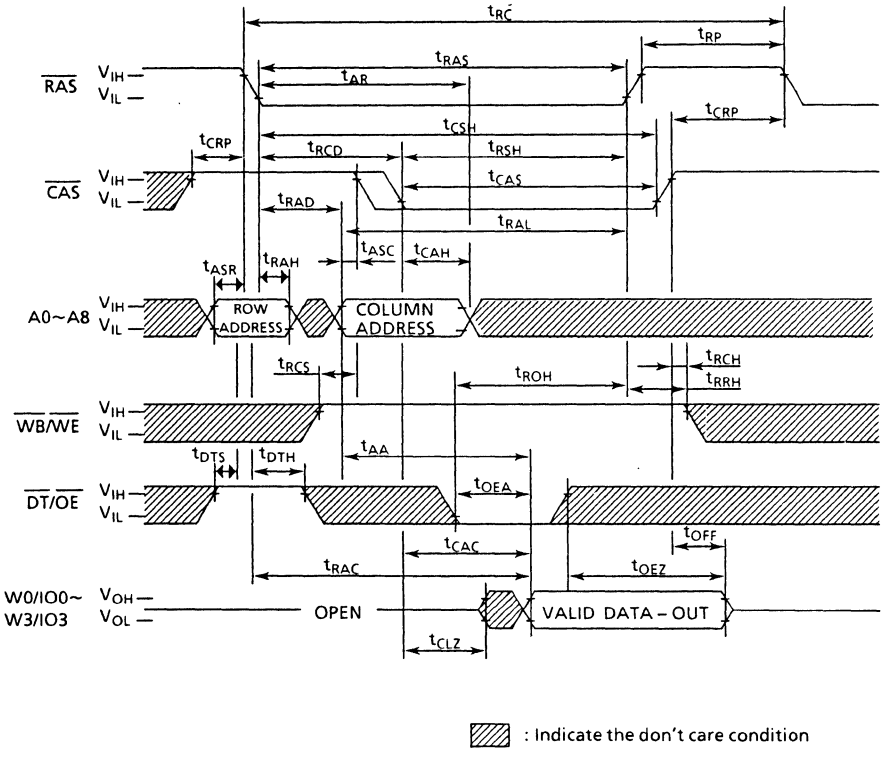
Symbol		MSM514251				Unit	Note
		-10		-12			
		MIN.	MAX.	MIN.	MAX.		
tSCC	Serial clock cycle time	30	-	40	-	ns	
tSCA	Access time from SC	-	30	-	40	ns	9
tSEA	Access time from $\overline{SE}$	-	30	-	40	ns	9
tSP	SC pulse width	10	-	10	-	ns	
tSCP	SC precharge time	10	-	10	-	ns	
tSOH	Serial data-out data hold time	10	-	10	-	ns	
tSEZ	$\overline{SE}$ to serial output buffer turn-off delay	0	25	0	25	ns	
tSIS	Serial data-in set-up time	0	-	0	-	ns	
tSIH	Serial data-in hold time	15	-	20	-	ns	
tDTS	$\overline{RAS}$ to $\overline{DT}$ set-up time	0	-	0	-	ns	
tRDH	$\overline{RAS}$ to $\overline{DT}$ hold time (Read transfer cycle)	80	-	100	-	ns	
tDTH	$\overline{RAS}$ to $\overline{DT}$ hold time	15	-	15	-	ns	
tCDH	$\overline{CAS}$ to $\overline{DT}$ hold time	30	-	40	-	ns	11
tSDD	Last SC to $\overline{DT}$ delay time	10	-	10	-	ns	
tSDH	$\overline{DT}$ to 1st SC hold time	10	-	10	-	ns	
tDTR	$\overline{DT}$ to $\overline{RAS}$ hold time	10	-	10	-	ns	
tRSD	$\overline{RAS}$ to 1st SC delay	85	-	105	-	ns	
tCSD	$\overline{CAS}$ to 1st SC delay	35	-	45	-	ns	
tMWS	$\overline{RAS}$ to $\overline{WE}$ set-up time	0	-	0	-	ns	
tMWH	$\overline{RAS}$ to $\overline{WE}$ hold time	15	-	15	-	ns	
tMS	$\overline{RAS}$ to mask data set-up time	0	-	0	-	ns	
tMH	$\overline{RAS}$ to mask data hold time	15	-	15	-	ns	
tSRZ	$\overline{RAS}$ to serial output buffer turn-off delay	10	50	10	60	ns	
tSRS	$\overline{RAS}$ to SC set-up time	30	-	40	-	ns	
tSRD	$\overline{RAS}$ to SC delay	25	-	30	-	ns	
tSID	$\overline{RAS}$ to serial data-in delay	50	-	60	-	ns	
tSZD	Serial data-in to $\overline{DT}$ delay	0	-	0	-	ns	
tES	$\overline{RAS}$ to $\overline{SE}$ set-up time	0	-	0	-	ns	
tEH	$\overline{RAS}$ to $\overline{SE}$ hold time	15	-	15	-	ns	
tSWS	Serial write enable set-up time	0	-	0	-	ns	
tSWH	Serial write enable hold time	30	-	40	-	ns	
tSWIS	Serial write disable set-up time	0	-	0	-	ns	
tSWIH	Serial write disable hold time	30	-	40	-	ns	
tDLZ	$\overline{DT}$ to serial data-out delay	5	-	10	-	ns	

NOTE

1. It is measured between V_{IH}(min) and V_{IL}(max).
2. Measured with a load circuit equivalent to 100pF and 2TTL.
3. tOFF(max) and tOEZ(max) define the time at which the output achieves the high impedance state (Iout ± 10uA) and are not referenced to V_{OH}(min) or V_{OL}(max)
4. Either tRRH or tRCH must be satisfied for a read cycle.
5. Measured from the $\overline{CAS}$ falling edge when the cycle is early write and measured from the WE falling edge when read-modify-write.
6. tWCS, tWH, tCWD, tRWD and tAWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If tWCS ≧ tWCS(min) and tWH ≧ tWH(min), the data out pin will remain open circuit(high inpedance) through the entire cycles ; If tCWD ≧ tCWD(min), tRWD ≧ tRWD(min) and tAWD ≧ tAWD(min), the cycle is a read-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out is indeterminate.
7. tRCD(max) is specified as a reference point only. When tRCD is less than tRCD(max), access time is tRAC. When tRCD is greater than tRCD(max), access time is tRCD + tCAC.
8. tRAD(max) is specified as a reference point only. When tRAD is less than tRAD(max), access time is tRAC(max). When tRAD is greater than tRAD(max), access time is tRAD + tAA.
9. Measured with a load equivalent to 50pF and 2 TTL.

TIMING DIAGRAM

Read cycle



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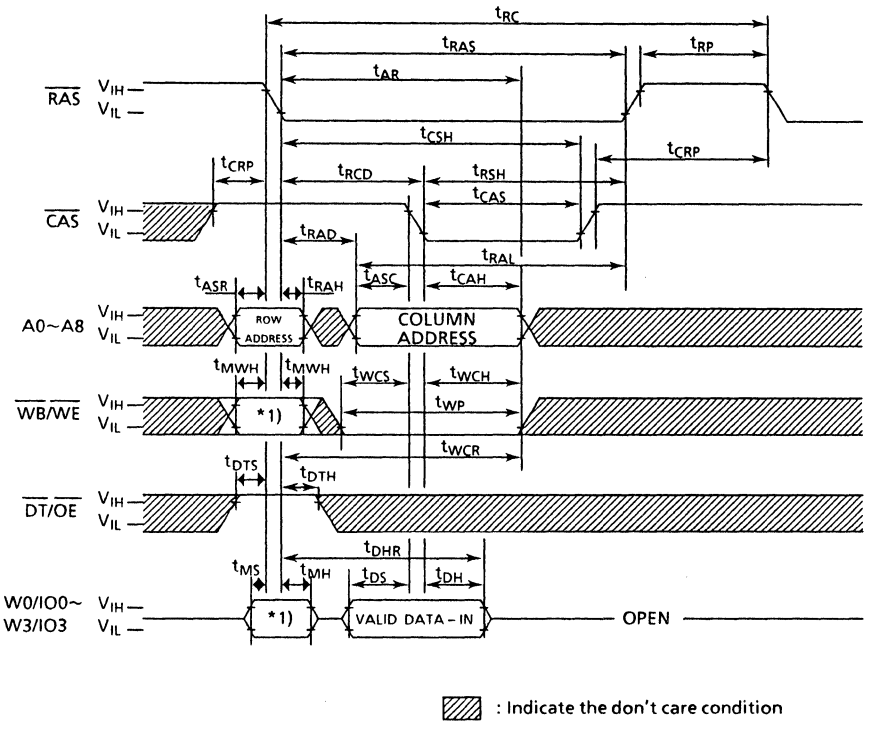
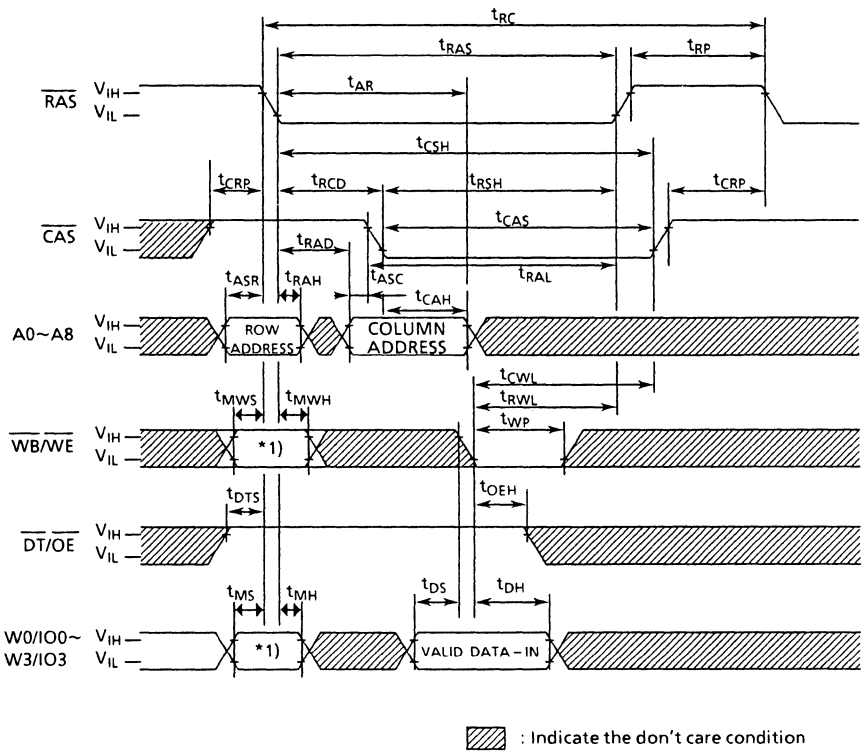
Write cycle (Early Write)



*1) I/O0 – 3 = "H": Non masked
I/O0 – 3 = "L" : Masked

9

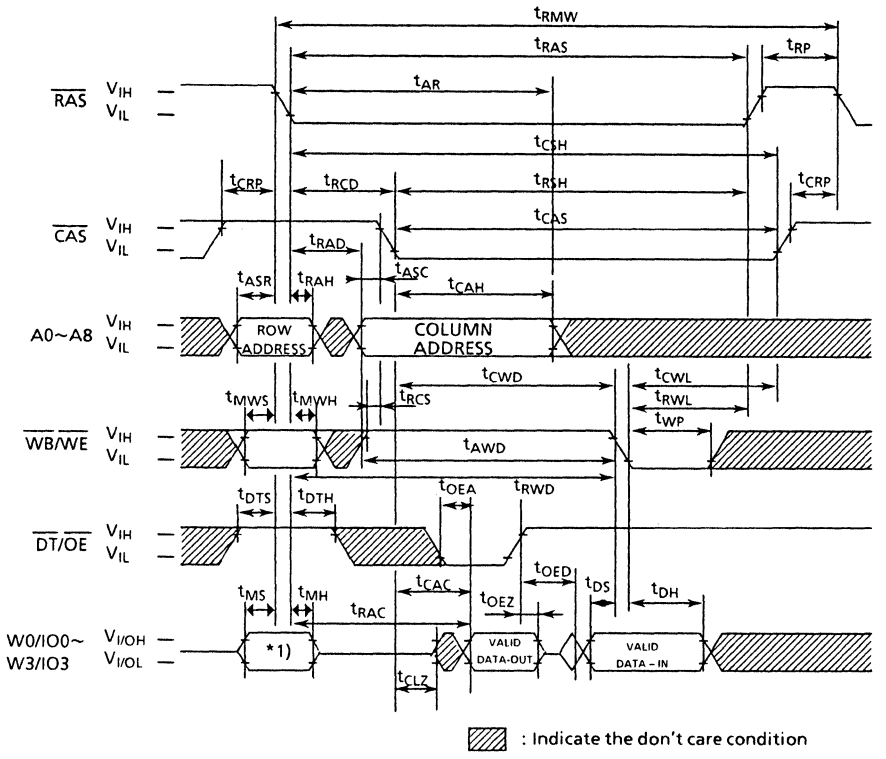
Write cycle ($\overline{DT}/\overline{OE}$ Control Write)



*1) I/O0 – 3 = "H" : Non masked
I/O0 – 3 = "L" : Masked

9

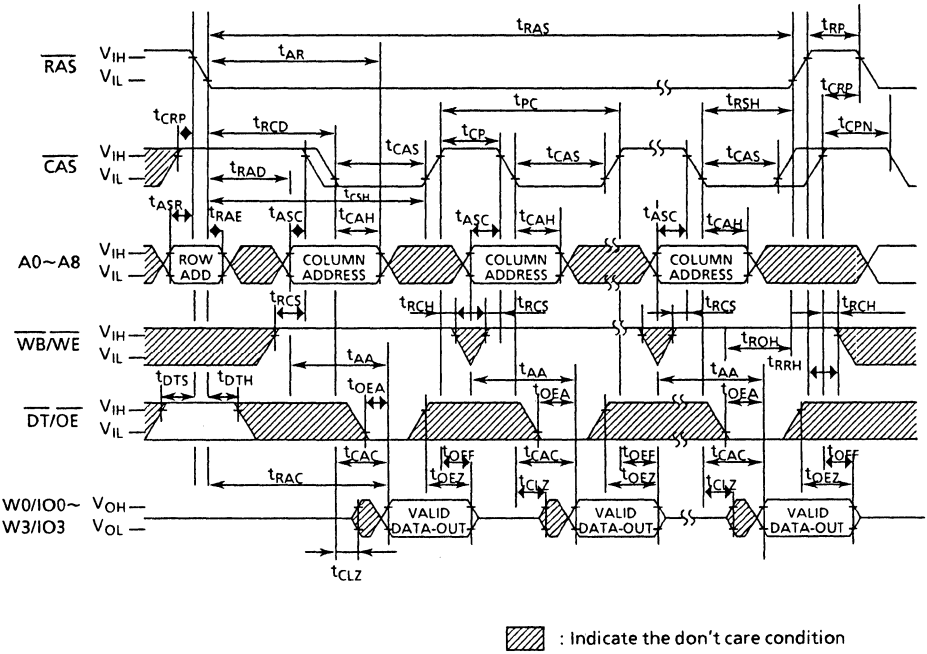
Read Modify Write cycle



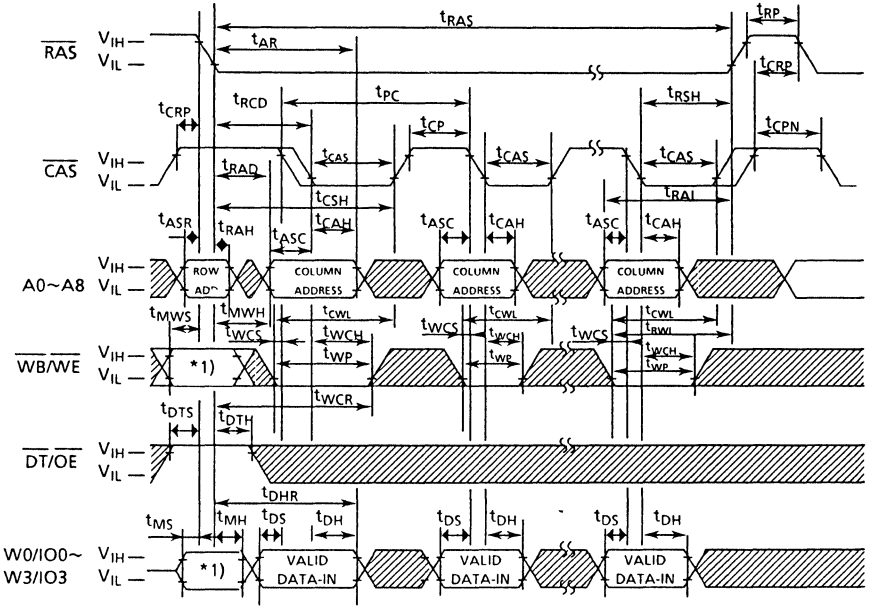
*1) I/O0 – 3 = "H": Non masked
I/O0 – 3 = "L" : Masked

9

Fast Page Read cycle



Fast Page Write cycle (Early Write)

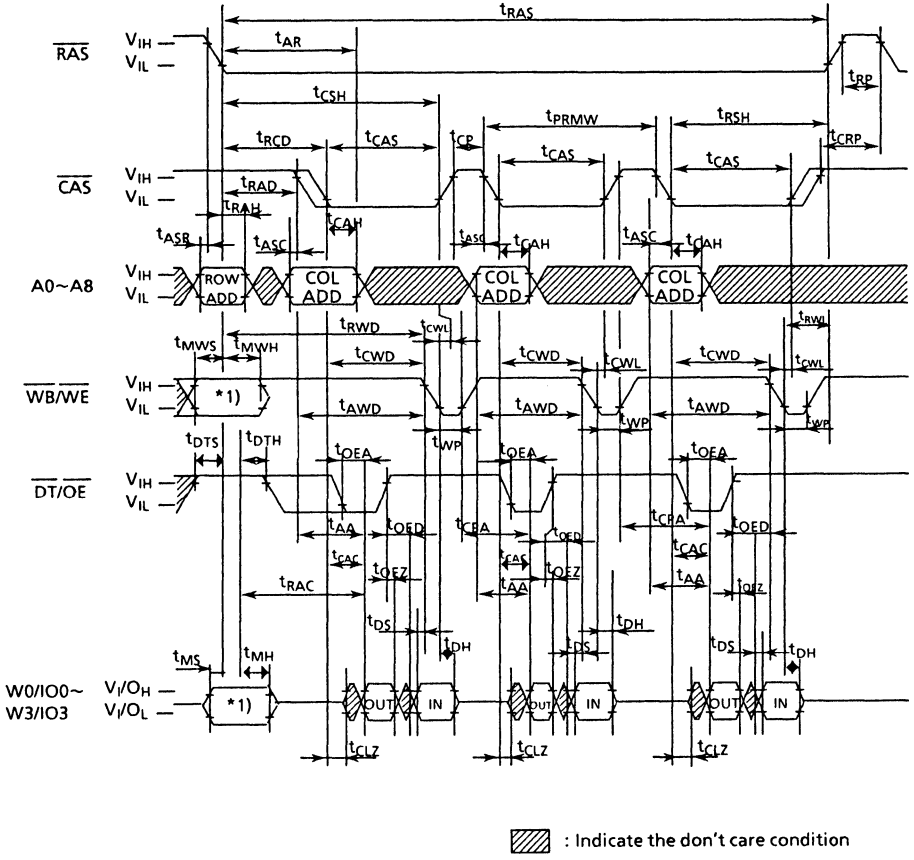


▨ : Indicate the don't care condition

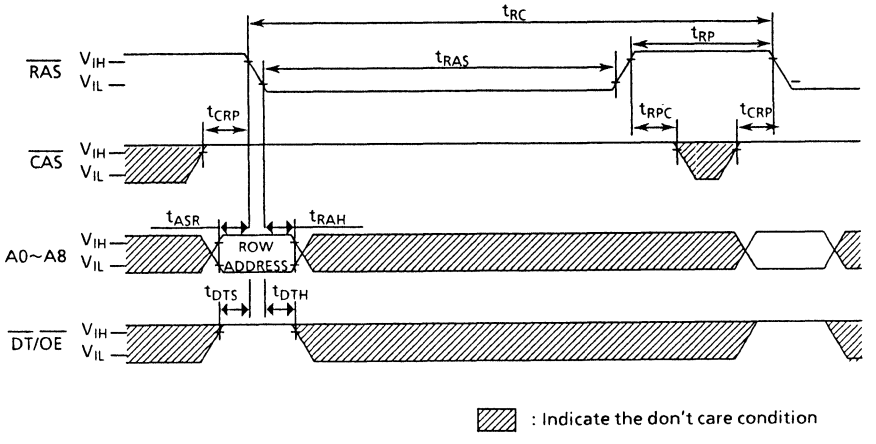
*1) I/O0 – 3 = "H": Non masked
I/O0 – 3 = "L" : Masked

9

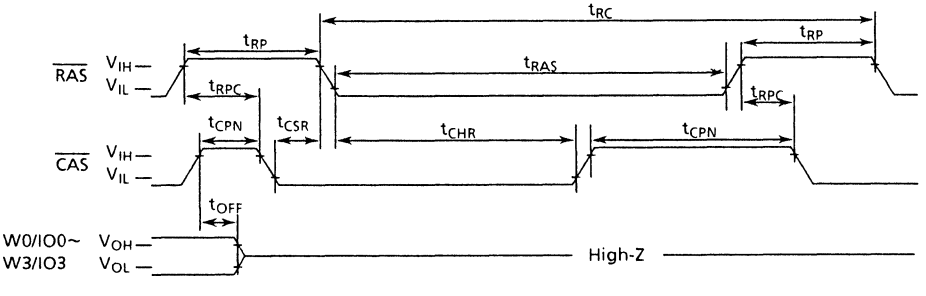
Fast Page Read Modify Write cycle



$\overline{RAS}$ Only Refresh



$\overline{CAS}$ Before $\overline{RAS}$ Refresh



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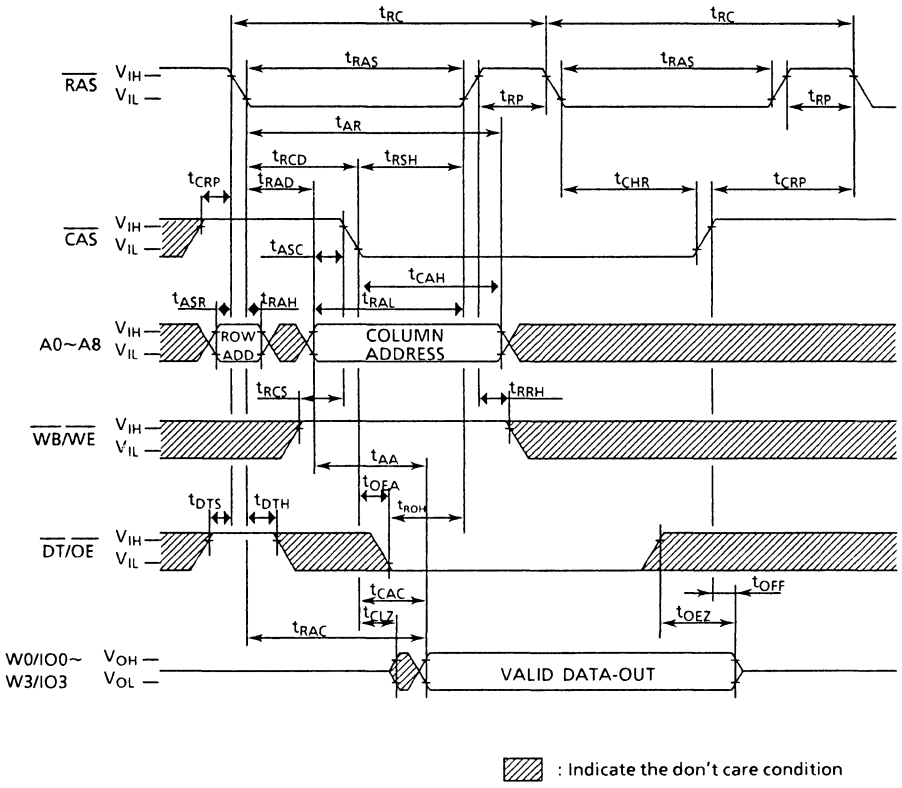
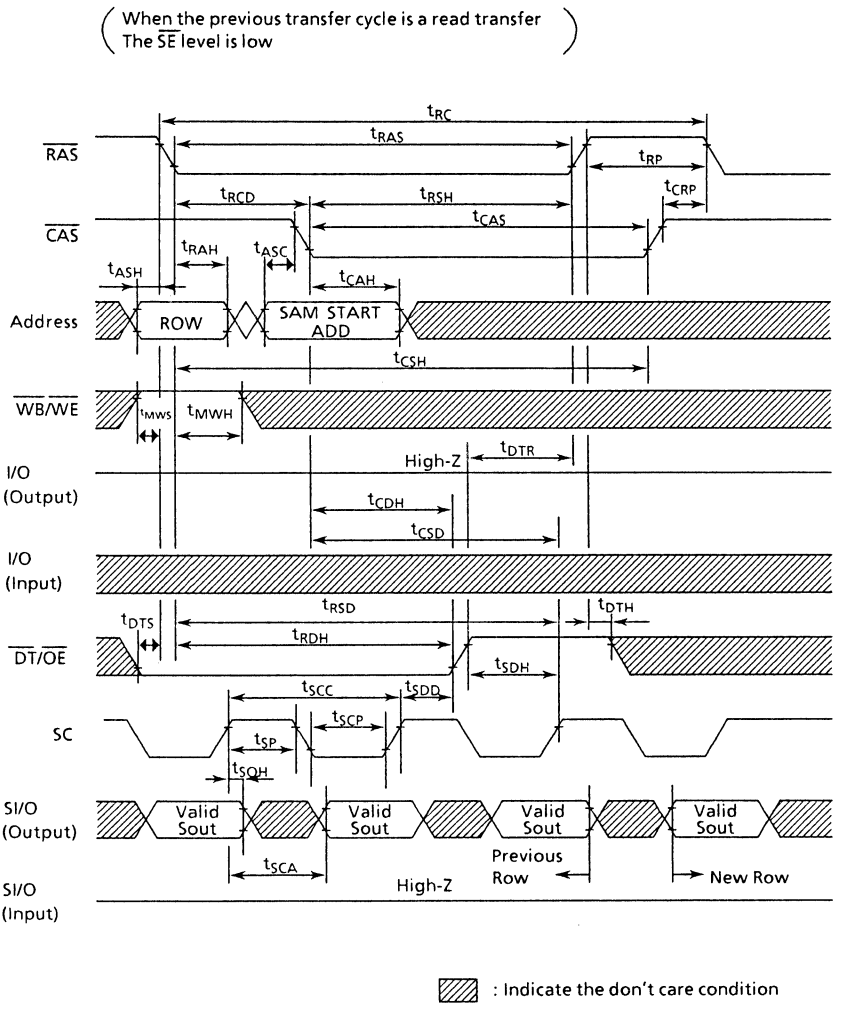
Hidden Refresh cycle



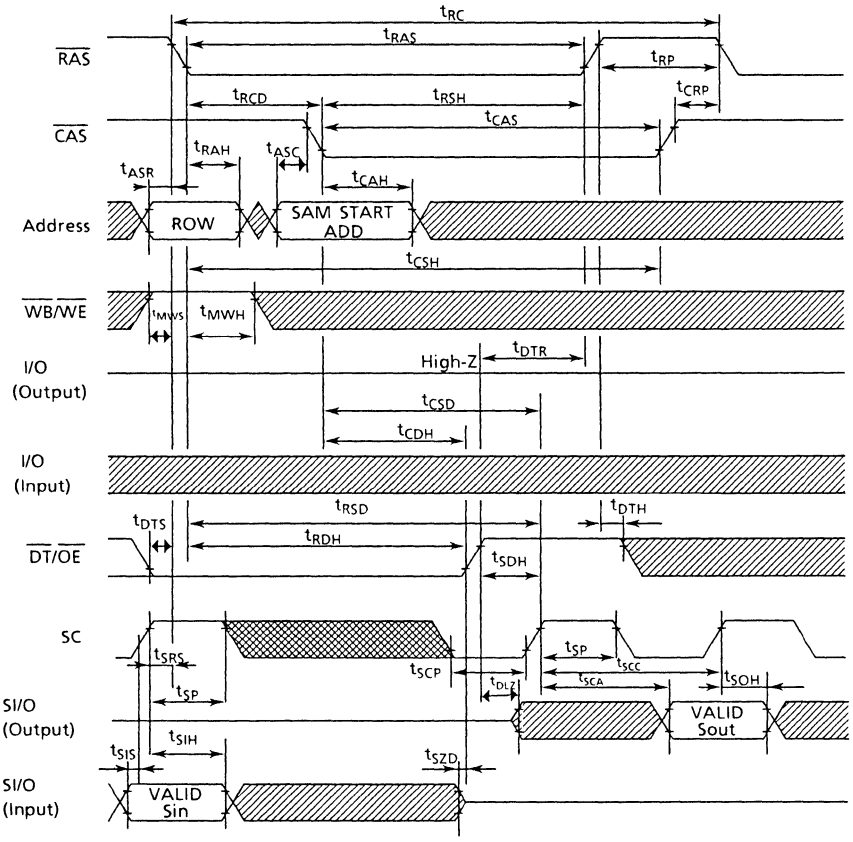
9

Read Transfer cycle (cycle-1)



Read Transfer cycle (cycle-2)

When the previous transfer cycle is a write transfer or a pseudo write transfer
The $\overline{SE}$ level is low

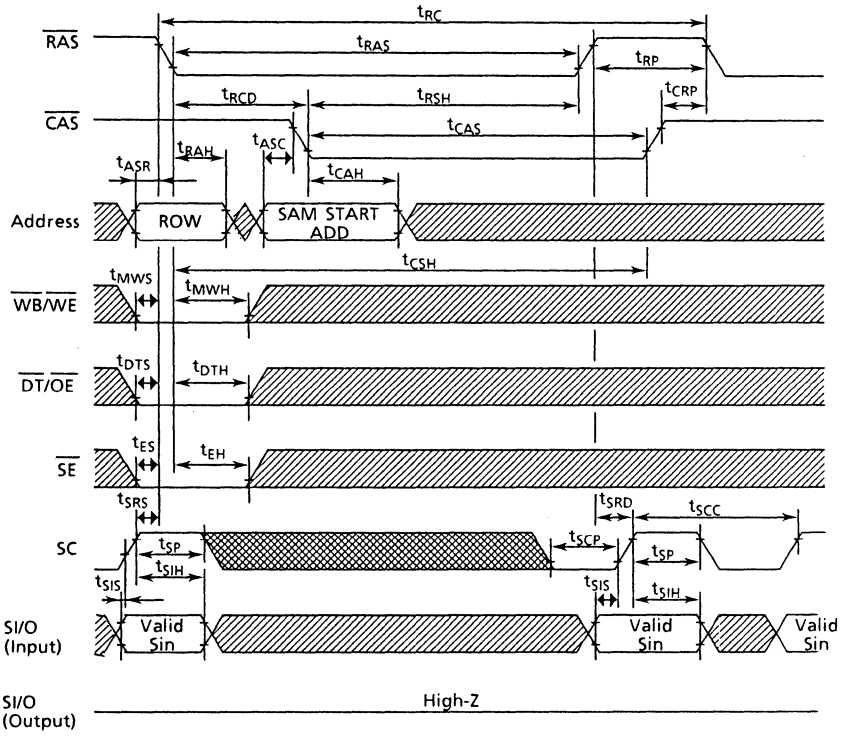


: Indicate the don't care condition

: Indicate that the rising edge is prohibited

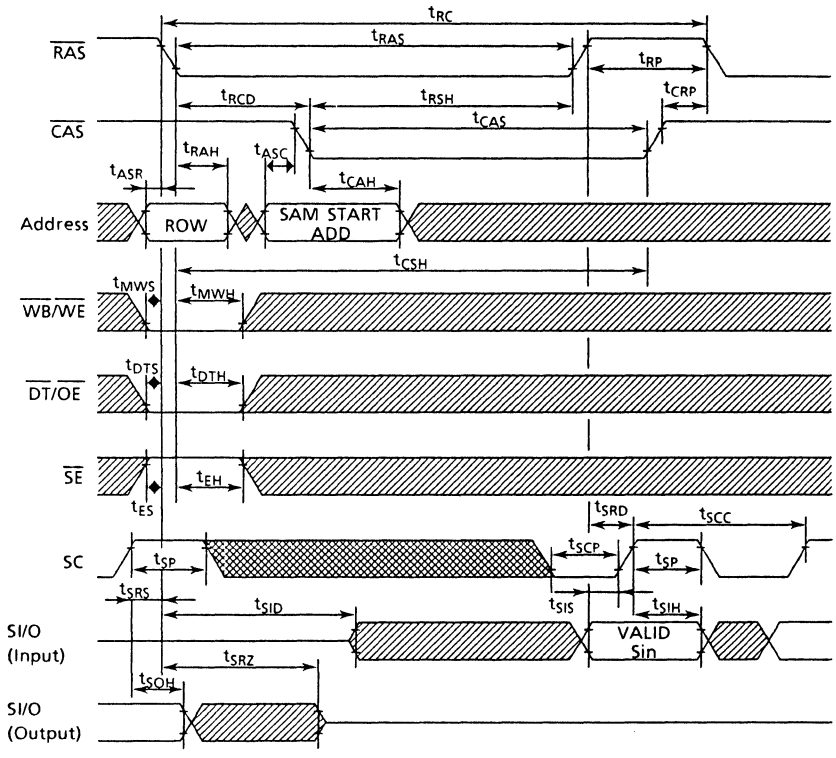
9

Write Transfer cycle



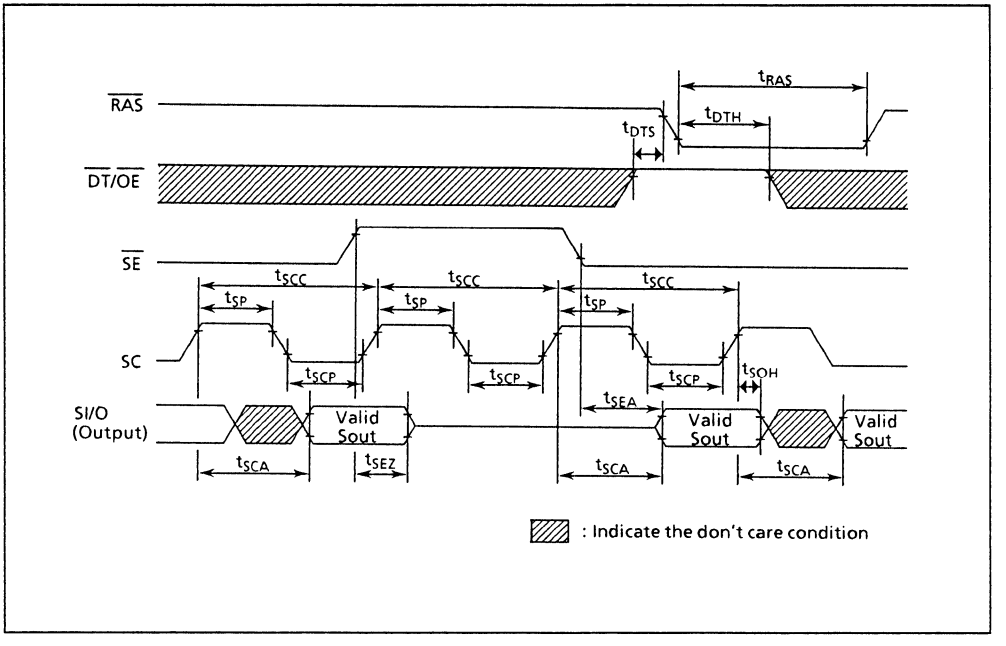
9

Pseudo Write Transfer cycle

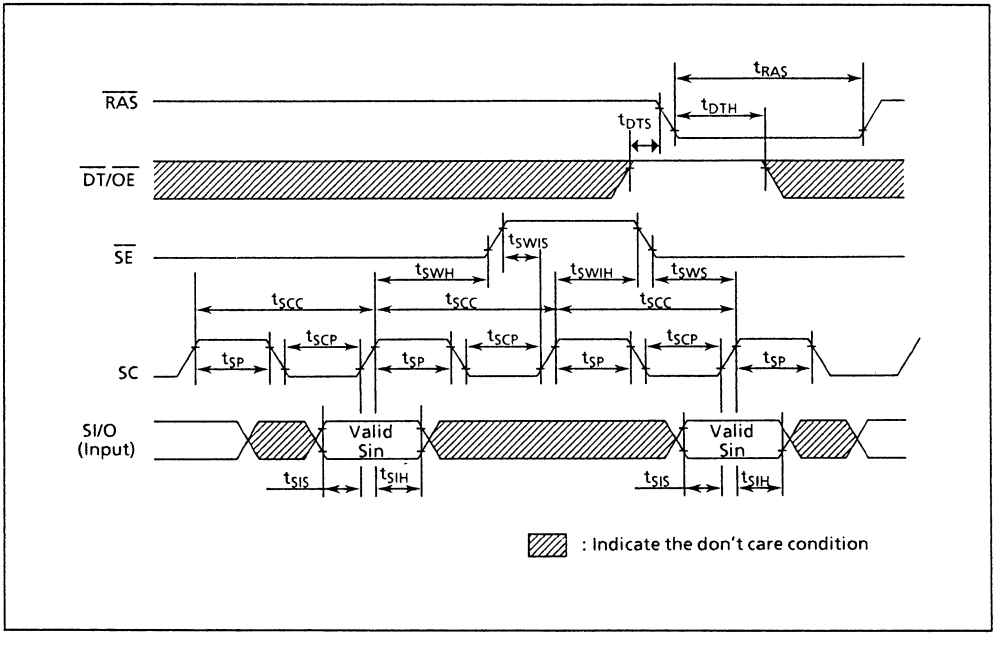


9

Serial Read cycle



Serial Write cycle



PIN DESCRIPTION

$\overline{RAS}$ (Row Address Strobe-input, active low)
Depending on the states of $\overline{CAS}$ and DT/OE, $\overline{RAS}$ will clock an internal row address (when $\overline{CAS}$ before $\overline{RAS}$ mode) or external row address into the row decoder. $\overline{RAS}$ also selects the write-per bit and the data transfer mode.

$\overline{CAS}$ (Column Address Strobe-input, active low)
In the data transfer cycle, $\overline{CAS}$ will clock an external column address into the column decoder. The selected column address becomes the SAM start address. $\overline{CAS}$ is also used as a clock which controls RAM port output impedance.
$\overline{CAS}$ will clock external column address into the column address decoder.

$\overline{WB/WE}$ (Write Enable-input, active low)
$\overline{WB/WE}$ is sampled when $\overline{RAS}$ falls and decoded in conjunction with $\overline{DT/OE}$ and $\overline{CAS}$ according to the Truth Table. When the $\overline{WB/WE}$ level is low at the $\overline{RAS}$ falling edge, the write-per-bit or write transfer cycle is selected. And when $\overline{WB/WE}$ level is high at the $\overline{RAS}$ falling edge, a 4-bit write to the RAM port or a read transfer cycle is selected. That is, if write-per-bit cycle is not selected then $\overline{WB/WE}$ functions as a normal write enable.

$\overline{DT/OE}$ (Data Transfer/Output Enable-input, active low)
The state of $\overline{DT/OE}$ is sampled along with $\overline{WB/WE}$ and $\overline{CAS}$ when $\overline{RAS}$ falls. The functions performed are shown in the Truth Table. When the $\overline{DT/OE}$ level at the $\overline{RAS}$ falling edge is low, the data transfer cycle is selected. And when $\overline{DT/OE}$ level is high, the read/write cycle is selected. During random access reads, $\overline{DT/OE}$ functions as the output enable pin.

A0-A8 (Address inputs, active high)
The MSM514252 employs an address-multiplexed-method which inputs the row addresses and the column addresses separately in order to select one word from the 256k words memory cells by using 9 address input pins. In the fast page mode, when the $\overline{RAS}$ level is low, column address specified by $\overline{CAS}$ enable 512 X 4 bits fast column access at a specified row address. In the data transfer cycle, the selected address input is also combined with the serial start address.

IO0-IO3 (random access data Input and Output-bidirectional, three state)
If the $\overline{WB/WE}$ level is low at the $\overline{RAS}$ falling edge then high level on IO0-IO3 enables data to be written to the enabled locations ; write-per-bit cycle. IO0-IO3 also serve as the data I/O pins for the random access port.

SC (Serial Control-input, active high)
Each SC rising edge starts the serial access. In the serial read cycle, the rising edge clocks four bits data from the serial data register to the output pins if $\overline{DT/OE}$ is active. In the serial write cycle, the rising edge clocks four bits data from serial data input pins to the serial data register.
If the $\overline{DT/OE}$ level is high, the SC signal is ignored.

$\overline{SE}$ (Serial Enable-input, active low)
$\overline{SE}$ enables serial input/output. When the $\overline{SE}$ level is high at the $\overline{RAS}$ falling edge, the cycle is pseudo-write data transfer cycle. When the $\overline{SE}$ level is low at the $\overline{RAS}$ falling edge, the cycle is write data transfer cycle.

SIO0-SIO3 (Serial access data Input and Output-bidirectional, three state)
Serial data appears if $\overline{SE}$ is active, otherwise they are high impedance.

FUNCTION

RAM Port Operation

The row address is specified by the $\overline{RAS}$ clock. The MSM514252 has a fast page mode capability so that when the $\overline{CAS}$ clock is activated, column data can be read/written continually.

The MSM514252 read/write cycle is set up by maintaining the $\overline{DT/OE}$ level high, while the $\overline{RAS}$ clock is falling. Data is read out when the $\overline{DT/OE}$ level is low and is written when the $\overline{WB/WE}$ level is low.

In the fast page mode cycle, when the $\overline{RAS}$ level is low, the column data in one specified row can be read/write continually according to the column address specified by $\overline{CAS}$.

When the $\overline{WB/WE}$ clock falls before the $\overline{CAS}$ falling edge, it becomes an early write cycle. When the $\overline{WE}$ clock falls after the $\overline{CAS}$ falling edge, it becomes a late write cycle.

In the random write cycle, the write-per-bit function is available.

SAM Port Operation

The data transfer cycle is set up when the $\overline{DT/OE}$ level is low at the $\overline{RAS}$ falling edge. A read data transfer cycle is performed when $\overline{WB/WE}$ is high. A write data transfer cycle is performed when $\overline{WB/WE}$ is low.

In the data transfer cycle, the row/column addresses are specified by the $\overline{RAS}/\overline{CAS}$ clocks, then the row address selects one row of RAM memory array and the column address selects the serial access start address.

- In the cycle which begins when the $\overline{DT/OE}$ level is high at the $\overline{RAS}$ falling edge, RAM and SAM are accessed independently. At the time, if the $\overline{DT/OE}$ level is low, the data transfer between RAM and SAM occurs.
  In one data transfer cycle, 512 X 4 bits data are transferred between the serial data register and any rows in the RAM array.

- The data transfer direction is selected by the $\overline{WB/WE}$ level at the $\overline{RAS}$ falling edge.
  From RAM to SAM (Read Data Transfer) : $\overline{WB/WE}$ = "H"
  From SAM to RAM (Write Date Transfer) : $\overline{WB/WE}$ = "L"

- Transfer cycle decides the following serial access cycles.
  Read data transfer - - - - → Serial read cycle
  Write data transfer - - - - → Serial write cycle
  (Pseudo write data transfer - - - - → Serial write cycle)

- No data transfer occurs from serial data register to RAM array when the $\overline{SE}$ level is high at the $\overline{RAS}$ falling edge in the write data transfer cycle. The data transfer is referred to as a pseudo write data transfer.

- During a read data transfer, a high speed data transfer execution is started at the $\overline{DT/OE}$ rising edge.

REFRESH OPERATION

Three operation methods for refreshing the MSM514252 dynamic RAM cells are available to users. The refresh operations on all 512 row addresses are required in every 8 ms.

• $\overline{RAS}$ Only Refresh

$\overline{RAS}$ only refresh is similar to a read cycle using any row address, except that $\overline{CAS}$ is high throughout the cycle and no column address is required. All the column data in the designated row address are refreshed simultaneously.

• $\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh uses an internal 9 bits refresh counters as the row address specifying the row to be refreshed. One $\overline{CAS}$ before $\overline{RAS}$ cycle increments an internal refresh counter one address. The refresh counter will be incremented each subsequent $\overline{CAS}$ before $\overline{RAS}$ cycle.

• Hidden Refresh

Hidden refresh is similar to $\overline{CAS}$ before $\overline{RAS}$ refresh, except that the $\overline{CAS}$ level and the $\overline{DT}/\overline{OE}$ level remain low. The data which was read in the previous cycle is held throughout the refresh period.

DATA TRANSFER OPERATION

• Read Data Transfer

Depending on the states of the $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ level at the $\overline{RAS}$ falling edge, (see the Truth Table) the Read Data Transfer Cycle is selected. The column data of one row designated by the row address are transferred to the serial shift data register.

At the same time, the decoded column address is set to the secondary serial register or serial address selector, which determines the serial read start address. This function is referred to as the pointer control. After the data transfer, every SC rising edge enables a serial data output and the serial address selector moves into the next bit.

As the serial address selector is cyclical in nature, the same data from the start address is output again when the SC clock is input more than 513 times.

$\overline{SE}$ controls the serial output buffers. When the $\overline{SE}$ level is low, the serial register data are output. When the $\overline{SE}$ level is high, the SIO0-SIO3 are at high impedance. The serial address selector has no relation with the $\overline{SE}$ level and shifts one bit at every SC rising edge.

Serial read data transfer can be done when SAM is in operation. That is the data from different rows can be continuously output. This operation is referred to as the Real Time Data Transfer.

• Write Data Transfer

Depending on the states of the $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ level at the $\overline{RAS}$ falling edge, (see the Truth Table) the Write Data Transfer Cycle is selected. The data on the serial data registers are transferred to the one row of RAM array which is designated by the row address.

At the same time, the decoded column address is set to the secondary serial register or serial address selector, which determines the serial write start address. After the data transfer, every SC rising edge enables a serial data input and the serial address selector moves into the next bit. The data input to the SIO0-SIO3 pins are written into the serial data register of SAM.

$\overline{SE}$ controls the serial input buffers. When the $\overline{SE}$ level is low, the input data are written into SAM. The serial address selector is not related to the $\overline{SE}$ level and shifts one bit at every SC rising edge. So when the $\overline{SE}$ level is high, the SC clock only shifts the serial address selector without writing the data in SAM.

• Pseudo Write Transfer

Depending on the states of the $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ level at the $\overline{RAS}$ falling edge, (see the Truth Table) the Pseudo Write Data Transfer Cycle is selected. The operation is the same as the write data transfer operation except for the fact that the data on the serial data register are not transferred to the RAM array. The row address which is input is ignored.

When the mode changes from serial read to serial write, a pseudo write transfer is used so that the one row data of RAM designated by the row address are not destroyed and are also used to change the mode of the serial port.

The difference between the read transfer and the write/pseudo-write transfer is that the write transfer and pseudo transfer cannot be done while SAM is operating.

POWER ON

An initial pause of 500 μsec is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause. And $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 8msec) of $\overline{RAS}$ inactivity before proper device operation is achieved.

After the above operation, prior to the SAM operation, the serial access mode must be selected by performing a data transfer cycle.

TRUTH TABLE (Mode Selection)

Input pin state at $\overline{RAS}$ falling				RAM	RAM	SAM
$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	I/O0-3		Bit Mask	SIO1-3
H	X	X	X	READ	-	-
H	X	X	X	WRITE	-	-
H	L	X	H	Write-Per-Bit	Non Masked	-
H	L	X	L	Write-Per-Bit	Masked	-
L	H	X	X	Read Transfer	-	Output Mode
L	L	L	X	Write Transfer	-	Input Mode
L	L	H	X	Pseudo Write Transfer	-	Input Mode

OKI semiconductor
MSM51C262

High Performance Low Power 64K x 4 Multi-port Memory with Fast Page Mode

DESCRIPTION

The OKI MSM51C262 is a high speed 65,536 x 4 bit multiport CMOS dynamic memory. The two ports, random access and serial access, are configured to offer optimum flexibility in graphics and other systems that require an interface between a processor and a high speed serial data channel such as a CRT or graphics display device.

The organization of the random access port of the MSM51C262 is exactly like, a 64K x 4 CMOS DRAM. Additional functions such as transfer between RAM and SAM utilize otherwise unused states of the $\overline{CAS}$, $\overline{DT}/\overline{OE}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ signals sampled at the falling edge of $\overline{RAS}$ at the beginning of a cycle.

The Serial Access Memory (SAM) is organized as 256 x 4 bits that can be read or written at high speed. The contents of the SAM can be loaded into RAM, and the contents of a selected RAM row (256 x 4) can be loaded into SAM. Except when transferring data between one another, the SAM and RAM operate in an asynchronous manner. The transfer from RAM to SAM or SAM to RAM also refreshes the transferred row in the RAM.

In a RAM to SAM load cycle, 8 bits are needed to specify which of the 256 rows is to be transferred. The state of the address lines at the falling edge of $\overline{CAS}$ is used to specify the starting point in the SAM where data is to be written or read. The static mechanization of the SAM (allowed by CMOS) does not require refreshing. The first access to SAM, either read or write, will be to the location specified at $\overline{CAS}$ time in the previous cycle, and subsequent accesses will continue in an increasing address direction, module 256.

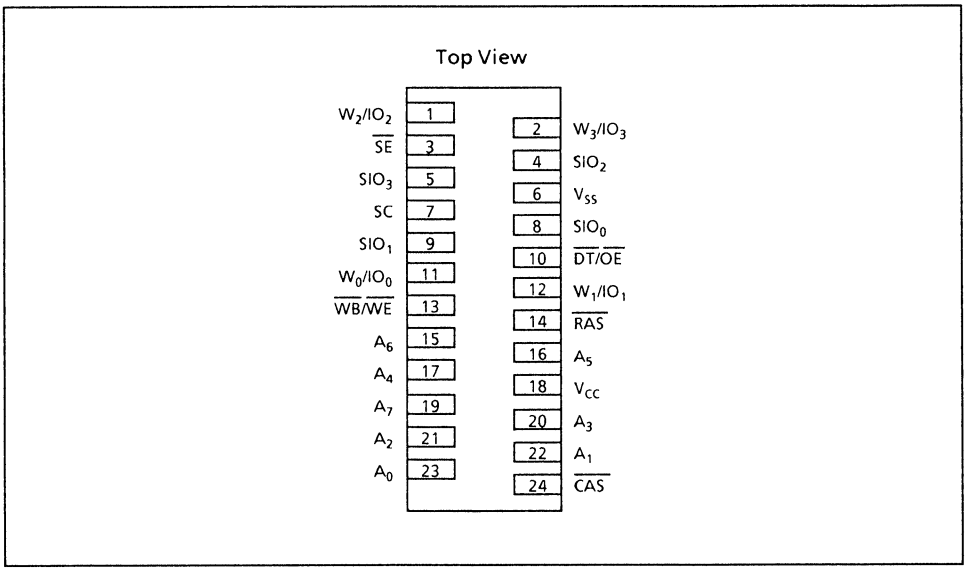
The MSM51C262 is processed utilizing OKI's CMOS silicon gate process technology. This advanced CMOS processing allows memory devices to be fabricated with lower operating current and higher performance than comparable NMOS designs. All I/O signals are TTL compatible. Input and I/O capacitances are significantly lowered to enhance system performance.

FEATURES

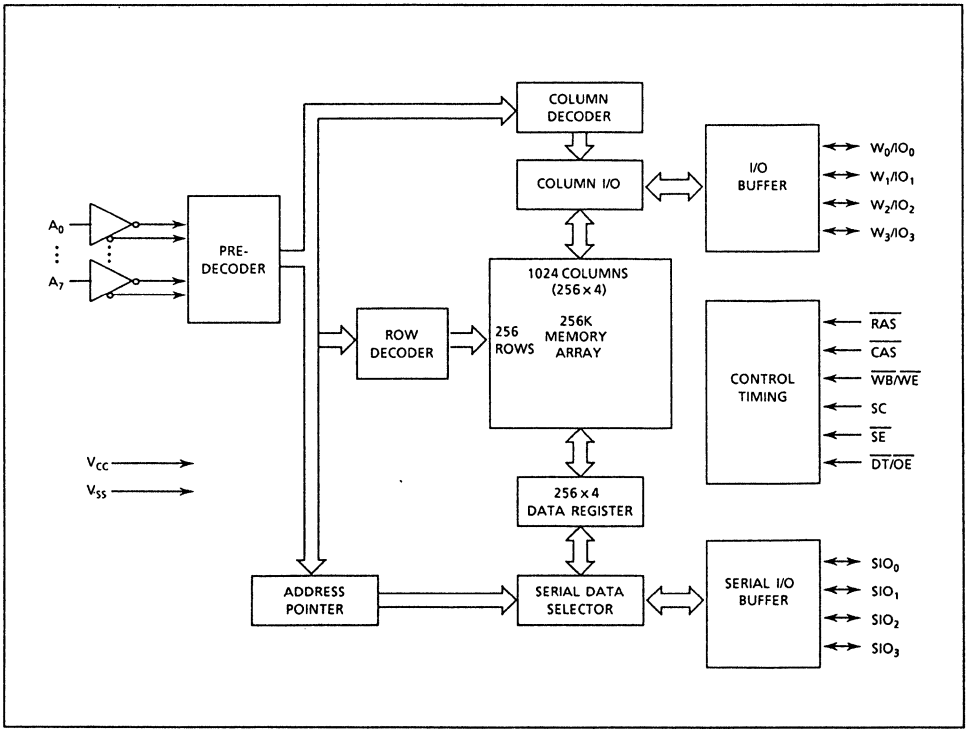
- Low power dissipation for MSM51C262-12
  - RAM Port operating alone – 50 mA
  - SAM Port operating alone – 35 mA
  - RAM/SAM operating 5 together – 85 mA
- Low CMOS standby current – 6 mA
- Fast Page Mode access, $\overline{RAS}$-only refresh, and $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Bi-directional data transfer between RAM and SAM with real-time operation.
- Bit-masked Write function on RAM port for additional flexibility.
- 256 Refresh cycle/4 ms.
- Standard package is 24 pin 400 mil Plastic ZIP.

High performance MSM51C262	– 80	– 10	– 12
Max. $\overline{RAS}$ Access Time (t_{RAC})	80 ns	100 ns	120 ns
Max. Column Address Time (t_{CAA})	40 ns	45 ns	55 ns
Min. Fast Column Mode Cycle Time (t_{PC})	55 ns	60 ns	70 ns
Min. Read/Write Cycle Time (t_{RC})	145 ns	175 ns	205 ns
Min. Serial Port Cycle Time (t_{SCC})	30 ns	35 ns	40 ns

24 LEAD PLASTIC ZIP PIN CONFIGURATION



BLOCK DIAGRAM



9

Absolute Maximum Ratings*

Rating	Value	Unit
Ambient Temperature Under Bias	0 to 70	°C
Storage Temperature (plastic)	− 55 to + 125	°C
Voltage on any Pin Except V_{CC} Relative to V_{SS}	− 1.0 to + 7.0	V
Voltage on V_{CC} Relative to V_{SS}	− 1.0 to + 7.0	V
Data Output Current	50	mA
Power Dissipation	1.0	W

* Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

AC Test Conditions

Conditions	Value	Unit
Input Rise Levels	0 to 3.0	V
Input Rise and Fall Times	5 between 0.8 V and 2.4 V	ns
Input Timing Reference Levels	0.8 and 2.4	V
Output Timing Reference Levels	0.8 and 2.4	V
Output Load (RAM Port)	2 TTL (and 100)	pF
Output Load (SAM Port)	2 TTL (and 50)	pF

CAPACITANCE*

$T_A = 25°C$, $V_{CC} = 5\ V \pm 10\%$, $V_{SS} = 0\ V$

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance		5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$, $\overline{SE}$, $\overline{SC}$, $\overline{DT/OE}$ Capacitance		8	pF
C_{OUT}	I/O Capacitance		7	pf

* Note: Capacitance is sampled and not 100% tested.

DC Characteristics (1)

(T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.)

Symbol	Parameter	Access Time	V53C261			Test Conditions	Notes
			min.	max.	Unit		
I_{LI}	Input Leakage Current, (any input pin)		-10	10	µA	$V_{SS} < V_{IN} < V_{CC}$	
I_{LO}	Output Leakage Current, (for Hige-Z State)		-10	10	µA	$V_{SS} < V_{OUT} < V_{CC}$ $\overline{RAS}$, $\overline{CAS}$ and $\overline{SE}$ at V_{IH}	
I_{CC1}	V_{CC} Supply Current	80		70	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port TTL Standby t_{RC} (min.), SC = V_{IL}	2, 3
		100		60			
		120		50			
I_{CC2}	V_{CC} Supply Current, TTL Stanbdy			8	mA	RAM/SAM ports TTL Standby $\overline{RAS}$, $\overline{CAS}$ at V_{IH}, I/O > V_{SS} SC = V_{IL}	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-Only Refresh	80		70	mA	$\overline{RAS}$ Cycling, $\overline{CAS}$ at V_{IH} SAM port TTL Standby t_{RC} (min.), SC = V_{IL}	2, 3
		100		60			
		120		50			
I_{CC4}	V_{CC} Supply Current, Page Mode Operation	80		60	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling SAM port TTL Standby t_{PC} (min.), SC = V_{IL}	2, 3
		100		50			
		120		40			
I_{CC5}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ Refresh	80		70	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port TTL Standby t_{RC} (min.), SC = V_{IL}	2, 3
		100		60			
		120		50			
I_{CC6}	V_{CC} Supply Current, RAM/SAMTransfer Mode	80		75	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port TTL Standby t_{RC} (min.), SC = V_{IL}	2, 3
		100		65			
		120		55			
I_{CC7}	V_{CC} Supply Current, Both Ports Active	80		120	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port Active t_{RC} (min.), t_{SCC} (min.)	2, 3
		100		100			
		120		85			
I_{CC8}	V_{CC} Supply Current, SAM Only Operation	80		50	mA	$\overline{RAS}/\overline{CAS}$ at V_{IH}, I/O > V_{SS} SAM port Active t_{SCC} (min.)	2
		100		40			
		120		35			
I_{CC9}	V_{CC} Supply Current, $\overline{RAS}$-Only Refresh and SAM Active	80		120	mA	$\overline{RAS}$ Cycling, $\overline{CAS}$ at V_{IH}, SAM port Active t_{RC} (min.), t_{SCC} (min.)	2, 3
		100		100			
		120		85			
I_{CC10}	V_{CC} Supply Current, Page Mode Operation and SAM Active	80		100	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling SAM port Active t_{PC} (min.), t_{SCC} (min.)	2, 3
		100		90			
		120		75			

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DC Characteristics (Cont'd)

Symbol	Parameter	Access Time	V53C261			Test Conditions	Notes
			min.	max.	Unit		
I_{CC11}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ Refresh and SAM Active	80		120	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port Active t_{RC} (min.), t_{SCC} (min.)	2, 3
		100		100			
		120		85			
I_{CC12}	V_{CC} Supply Current, RAM/SAM Transfer Mode and SAM Active	80		125	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port Active t_{RC} (min.), t_{SCC} (min.)	2, 3
		100		105			
		120		90			
I_{CC13}	V_{CC} Supply Current, Both Ports CMOS Standby	80		6	mA	$\overline{RAS}$, $\overline{CAS}$, $\overline{SE}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE} > V_{CC} - 0.5$ V SC < 0.6 V	
		100		6			
		120		6			
V_{IL}	Input Low Voltage		−1	0.8	V		
V_{IH}	Input High Voltage		2.4	V_{CC} +1	V		
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		V	I_{OH} = −2 mA	

AC Characteristics (4, 5, 6)

Read, Write, Read-Modify-Write and Refresh Cycles

(T_A = 0°C to 70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.)

#	Symbol	Parameter	-80		-10		-12		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
	t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	ns	
	t_{RI}	Refresh Interval (256 Cycles)		4		4		4	ms	
1	t_{RC}	Read or Write Cycle Time	145		175		205		ns	
2	t_{RAS}	$\overline{RAS}$ Pulse Width	80	37K	100	37K	120	37K	ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	55		65		75		ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	80		100		120		ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	25		30		35		ns	
6	t_{ASR}	Row Address Setup Time	0		0		0		ns	
7	t_{RAH}	Row Address Hold Time	15		15		15		ns	
8	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		10		ns	
9	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	55	25	70	25	85	ns	7
10	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CAH}	Column Address Hold Time	15		20		20		ns	
12	t_{RSH}	$\overline{RAS}$ Hold Time	25		30		35		ns	
13	t_{DHS}	$\overline{DT}$ High Setup Time	0		0		0		ns	
14	t_{DHH}	$\overline{DT}$ High Hold Time	20		20		20		ns	
15	t_{AR}	Column Address Hold Time from $\overline{RAS}$	60		70		80		ns	

AC Characteristics (Cont'd)

Read Cycle

#	Symbol	Parameter	-80		-10		-12		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
16	t_{RAC}	$\overline{RAS}$ Access Time		80		100		120	ns	8, 9
17	t_{CAC}	$\overline{CAS}$ Access Time		25		30		35	ns	9,10,11
18	t_{CAA}	Column Address Access Time		40		45		55	ns	9
19	t_{RCS}	Read Command Setup Time	0		0		0		ns	
20	t_{RRH}	Read Command Hold Time $\overline{RAS}$-Referenced	5		5		10		ns	12
21	t_{RCH}	Read Command Hold Time $\overline{CAS}$-Referenced	0		0		0		ns	12
22	t_{OAC}	$\overline{OE}$ Access Time		20		25		30	ns	9
23	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to Output High-Z		20		25		30	ns	13
24	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Output Low-Z	0		0		0		ns	
25	t_{OH}	Output Hold Time from OE or CAS	0		0		0		ns	

AC Characteristics (Cont'd)

Write Cycle

#	Symbol	Parameter	-80		-10		-12		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
26	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	25		30		35		ns	
27	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	25		30		35		ns	
28	t_{WP}	Write Command Pulse Width	15		20		25		ns	
29	t_{WCS}	Write Command Setup Time	0		0		0		ns	14
30	t_{WCH}	Write Command Hold Time	15		20		25		ns	
31	t_{DS}	Data In Setup Time	0		0		0		ns	
32	t_{DH}	Data In Hold Time	15		20		25		ns	
33	t_{WBS}	Write Mask Setup Time	0		0		0		ns	
34	t_{WBH}	Write Mask Hold Time	20		20		20		ns	
35	t_{WS}	Write Mask Select Setup Time	0		0		0		ns	
36	t_{WH}	Write Mask Select Hold Time	20		20		20		ns	
37	t_{OEH}	$\overline{OE}$ Hold Time Referenced to WE	10		10		15		ns	
38	t_{WCR}	Write Hold Time from $\overline{RAS}$	65		80		95		ns	
39	t_{DHR}	Data Hold Time from $\overline{RAS}$	65		80		95		ns	

Read-Modify-Write Cycle

#	Symbol	Parameter	-80		-10		-12		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
40	t_{RWC}	Read-Modify-Write Cycle Time	205		245		285		ns	
41	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	140	37K	170	37K	200	37K	ns	
42	t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	85		100		115		ns	
43	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	110		135		160		ns	14
44	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	55		65		75		ns	14
45	t_{AWD}	Column Address to $\overline{WE}$ Delay	70		80		95		ns	
46	t_{OED}	$\overline{OE}$ to Data In Delay Time	20		25		30		ns	

AC Characteristics (Cont'd)

Fast Page Mode Operation

#	Symbol	Parameter	-80		-10		-12		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
47	t_{PC}	Page Mode Cycle Time	55		60		70		ns	
48	t_{CP}	$\overline{CAS}$ Precharge Time	15		20		25		ns	
49	t_{CAP}	Access Time from Column Precharge		50		55		65	ns	15

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

#	Symbol	Parameter	-80		-10		-12		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
50	t_{CSR}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Setup Time	10		10		10		ns	
51	t_{CHR}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Hold Time	25		25		25		ns	
52	t_{RPC}	$\overline{RAS}$ Precharge to CAS Active Time	0		0		0		ns	

AC Characteristics (Cont'd)

Read/Write, Pseudo Write Transfer and Serial Read/Write Cycle

#	Symbol	Parameter	-80		-10		-12		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
53	t_{SCC}	Serial Clock Cycle Time	30		35		40		ns	
54	t_{SCL}	SC Precharge Time	10		10		10		ns	
55	t_{SOO}	$\overline{SE}$ to Serial Out Setup Time	0		0		5		ns	
56	t_{SOH}	Serial Out Hold after SC High	0		0		5		ns	
57	t_{SCA}	Serial Output Access Time from SC		25		30		35	ns	16
58	t_{SOA}	Serial Output Access Time from $\overline{SE}$		20		25		30	ns	16
59	t_{SOZ}	Serial Output Disable Time from $\overline{SE}$ High		15		20		25	ns	13
60	t_{SCH}	SC Pulse Width	10		15		15		ns	
61	t_{SOE}	$\overline{SE}$ Pulse Width	10		10		10		ns	
62	t_{SOP}	$\overline{SE}$ Precharge Time	10		10		10		ns	
63	t_{DLS}	Transfer Command to $\overline{RAS}$ Setup Time	0		0		0		ns	
64	t_{RDH}	Transfer Command to $\overline{RAS}$ Hold Time	60		75		90		ns	
65	t_{CDH}	Transfer Command to $\overline{CAS}$ Hold Time	20		25		30		ns	
66	t_{SDD}	SC to Transfer Command Lead Time	10		15		20		ns	
67	t_{SDH}	SC Hold Time after $\overline{DT}$ High	10		10		10		ns	
68	t_{SZS}	Serial Data Input to $\overline{DT}$ High Delay Time		0		0		0	ns	
69	t_{DTP}	$\overline{DT}$ Precharge Time	20		25		30		ns	
70	t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	65		75		85		ns	
71	t_{SWS}	Serial Write Enable Setup Time	10		10		10		ns	
72	t_{SWH}	Serial Write Enable Hold Time	10		15		20		ns	
73	t_{SWIS}	Serial Write Disable Setup Time	10		10		10		ns	
74	t_{SWIH}	Serial Write Disable Hold Time	10		15		20		ns	
75	t_{SRS}	SC to $\overline{RAS}$ Setup Time	15		20		20		ns	

AC Characteristics (Cont'd)

Read/Write, Pseudo Write Transfer and Serial Read/Write Cycle

#	Symbol	Parameter	-80		-10		-12		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
76	t_{ES}	Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Setup Time	0		0		0		ns	
77	t_{EH}	Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Hold Time	20		20		20		ns	
78	t_{SIS}	Serial Data In Setup Time	0		0		0		ns	
79	t_{SIH}	Serial Data In Hold Time	10		10		10		ns	
80	t_{SDS}	SC to $\overline{DT}$ High Setup Time	0		0		0		ns	
81	t_{SCR}	SC to $\overline{RAS}$ Precharge Setup Time	0		0		0		ns	

Notes:

1. All voltages are referenced to V_{SS}. An initial pause of 200 μs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock e.g. $\overline{RAS}$-only refresh). Eight initialization cycles are required after extended periods of bias without clocks (greater than 4 ms).
2. I_{CC} is dependent on output loading when the device output is enabled. I_{CC} (max.) is measured with all outputs open.
3. I_{CC} is dependent on the number of address transitions while $\overline{CAS}$ is at V_{IH}. Specified I_{CC} (max.) is measured with a maximum of two transitions per address input per random cycle and one transition per address cycle in Fast Page Mode.
4. All voltages are referenced to V_{SS}. V_{IH} (min.) and V_{IL} (max.) are the reference levels for measuring input signal timing. Transition times are measured between V_{IH} (min.) and V_{IL} (max.).
5. An initial pause of 200 μs and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks or upon Power Up. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
6. AC characteristics assume $t_T = 5$ ns. All AC measurements are made with a load equivalent to two TTL inputs and either 50 or 100 pF in parallel. V_{IL} (min.) > V_{SS} and V_{IH} (max.) < V_{CC}.
7. t_{RCD} (max.) is for reference only. t_{RCD} (min.) = t_{RAH} (min.) + $2t_T$ + t_{ASC} (min.).
8. Assumes that t_{RCD} < t_{RCD} (max.). If t_{RCD} > t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
9. Measured with a load equivalent to 2 TTL loads and 100 pF in parallel.
10. Assumes t_{RCD} > t_{RCD} (max.).

11. If $t_{ASC} < (t_{CAA}$ (max.) $- t_{CAC}$ (max.) $- t_T)$, access time is defined by t_{CAA} rather than t_{CAC}.

12. Either t_{RCH} or t_{RRH} must be satisfied.

13. An output disable time defines the time when the output reaches the open-circuit condition and is not referenced to output voltage levels.

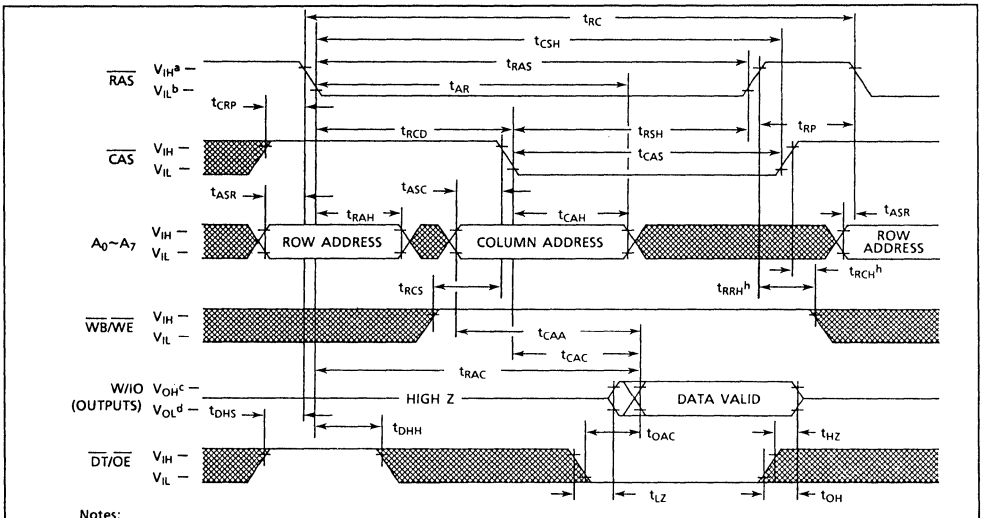
14. t_{WCS}, t_{RWD} and t_{CWD} are specified for reference only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is a $\overline{CAS}$-controlled write cycle (Early Write), and the DQ pins will be at High-Z during the entire cycle. If $t_{CWD} > t_{CWD}$ (min.), and $t_{RWD} > t_{RWD}$ (min.), the cycle is a Read-Modify-Write cycle, and the DQ pins will reflect the data read from the addressed location. If any of the above conditions is not satisfied, the condition of the Data Out pins will be indeterminate.

15. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.

16. Measured with a load equivalent to 2 TTL loads and 50 pF in parallel.

TIMING CHART

Read Cycle



Notes:

a, b: V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals.

c, d: V_{OH} (min.) and V_{OL} (max.) are reference levels for measuring timing of D_{OUT}.

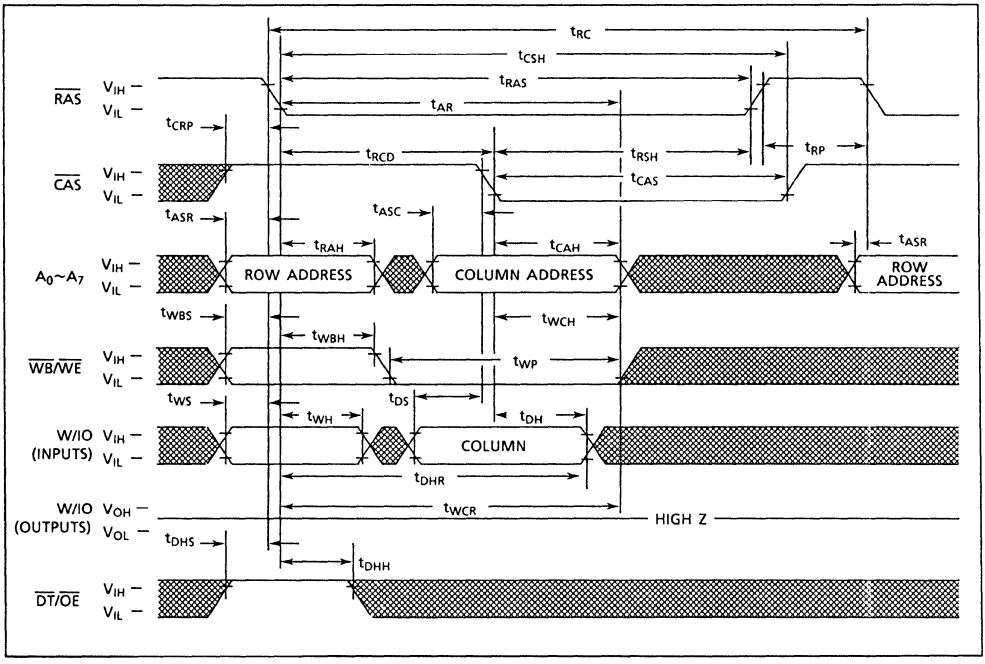
e: t_{LZ} is referenced to the lesser of $\overline{CAS}$, and $\overline{OE}$ low transition.

f: t_{HZ} and t_{OH} are referenced to one earlier of $\overline{CAS}$ or $\overline{OE}$ high transition.

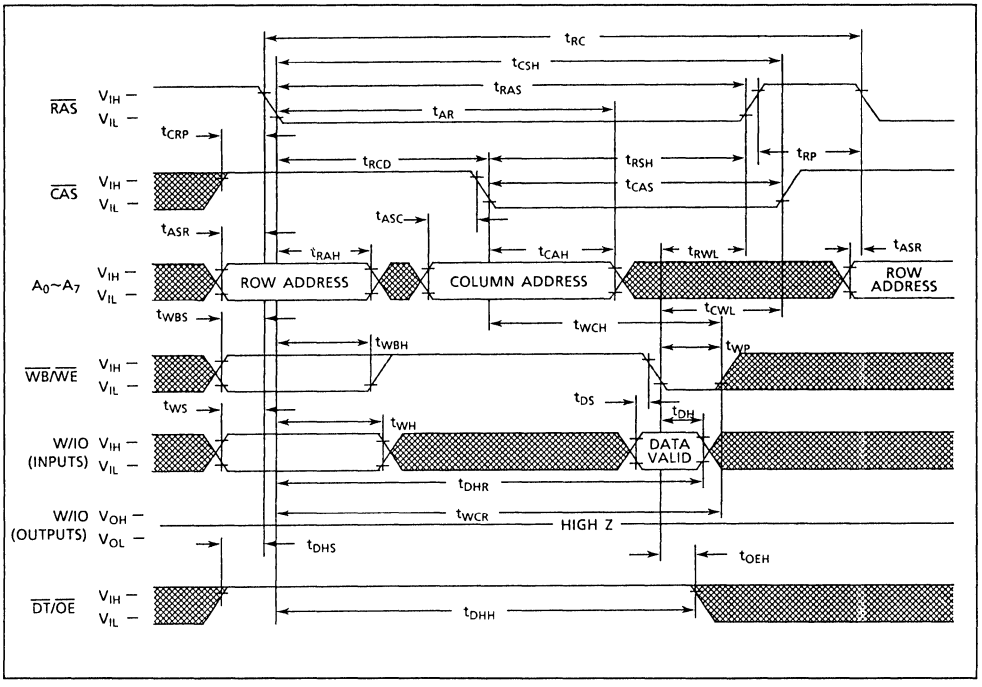
g: Transition is measured + 500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

h: Either t_{RCH} or t_{RRH} must be specified.

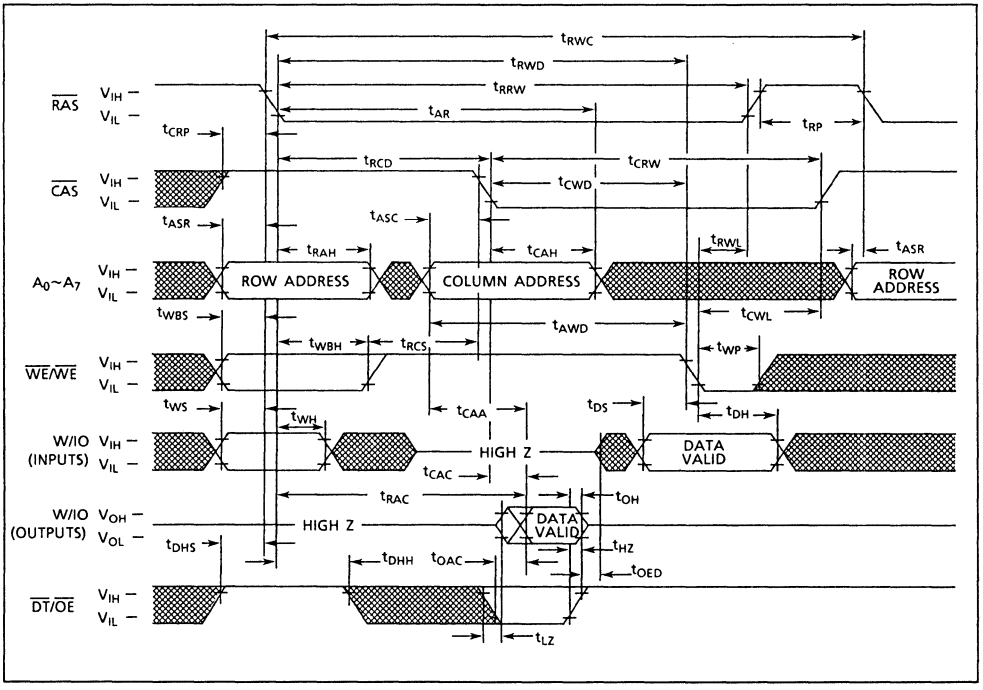
Write Cycle (Early Write)



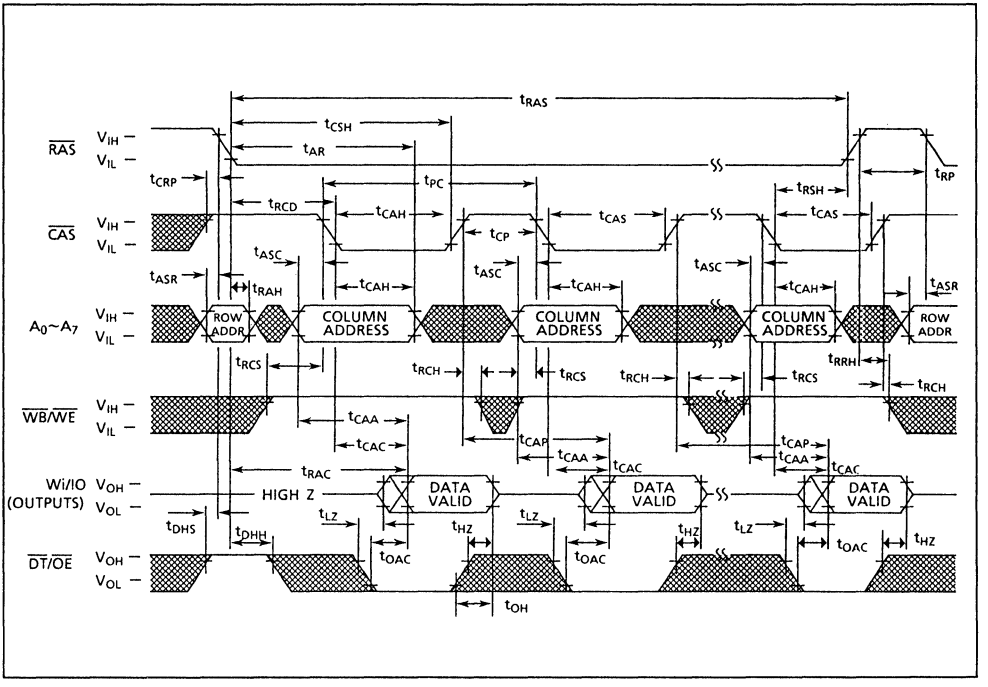
Write Cycle (Delayed Write)



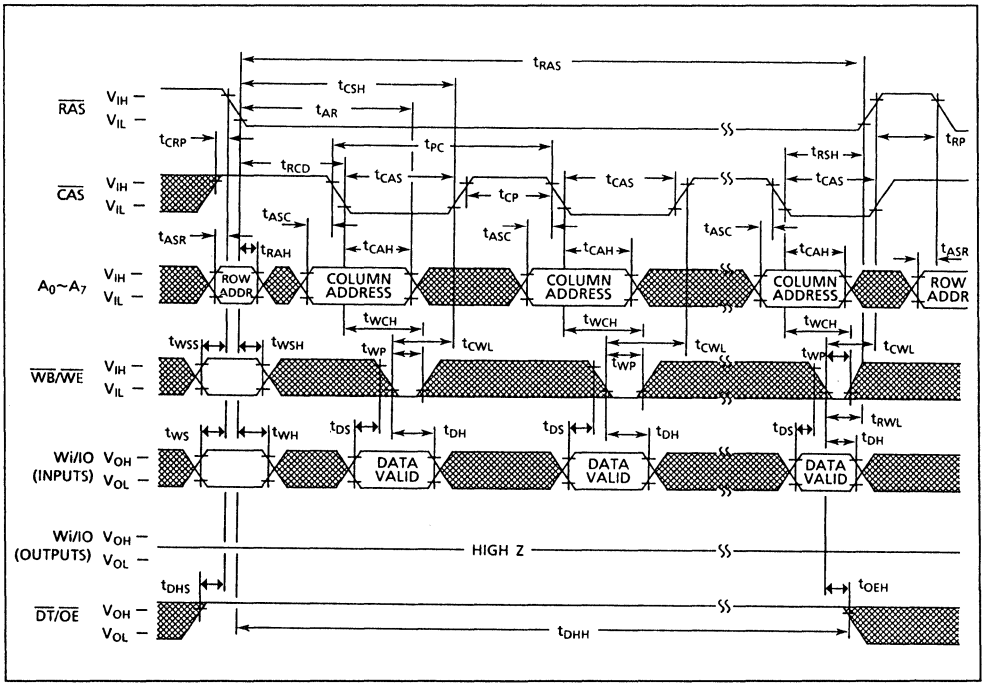
Read-Modify-Write Cycle



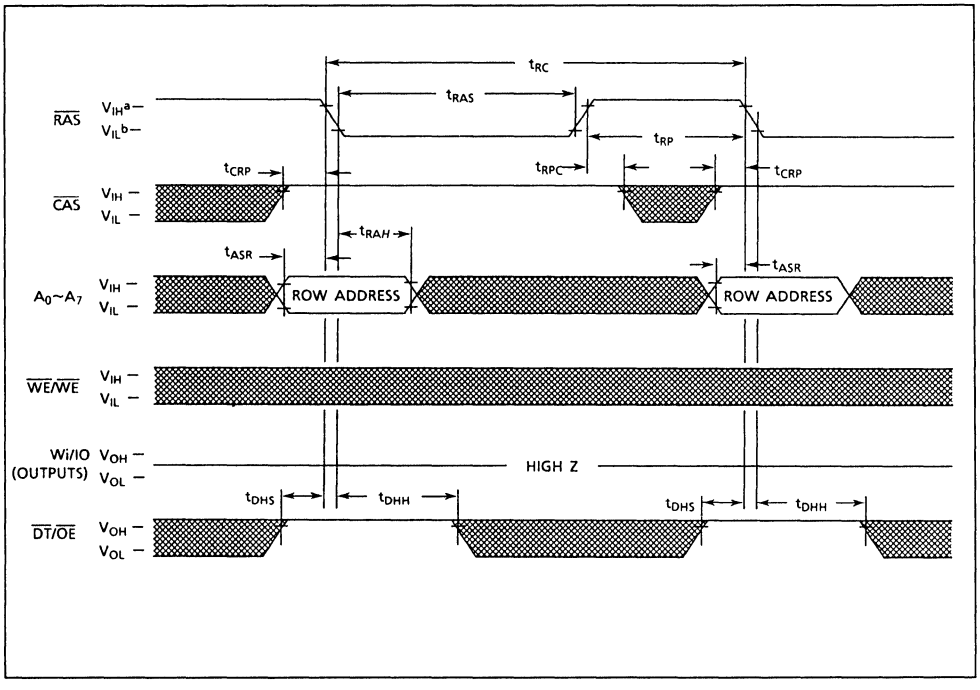
Waveforms of Fast Page Read Cycle



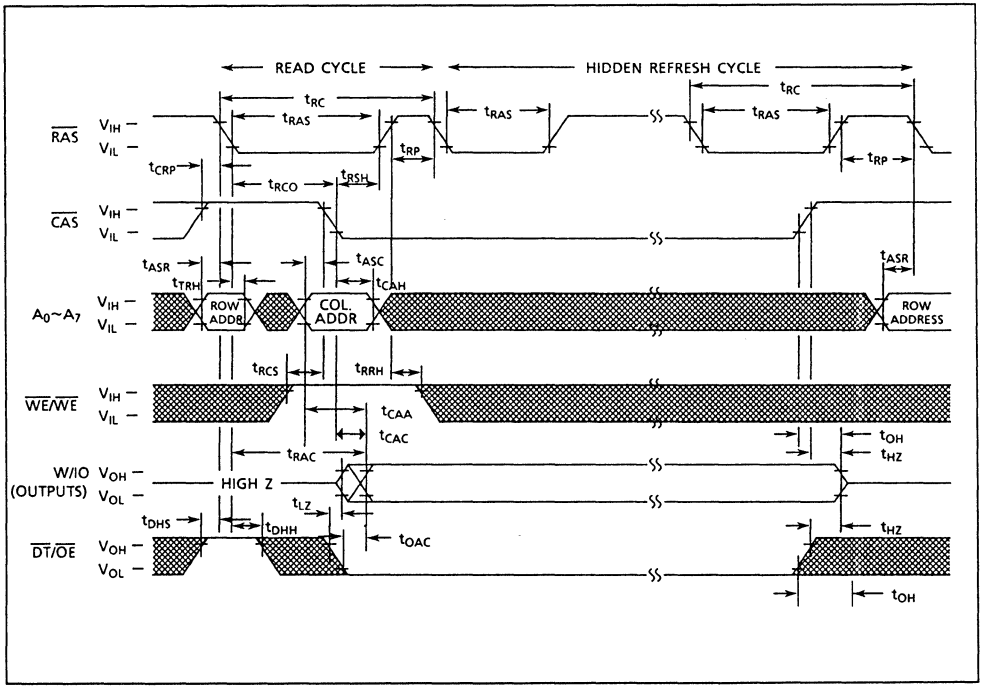
Waveforms of Fast Page Mode Write Cycle



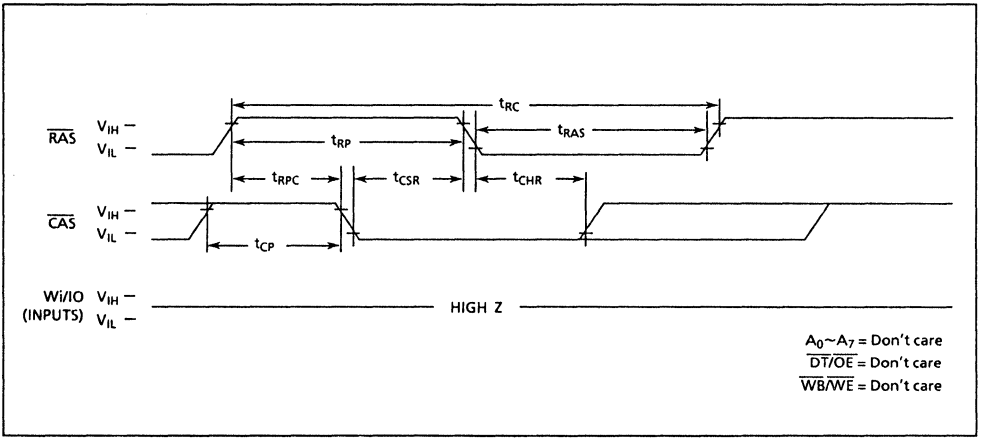
$\overline{RAS}$-Only Refresh Cycle



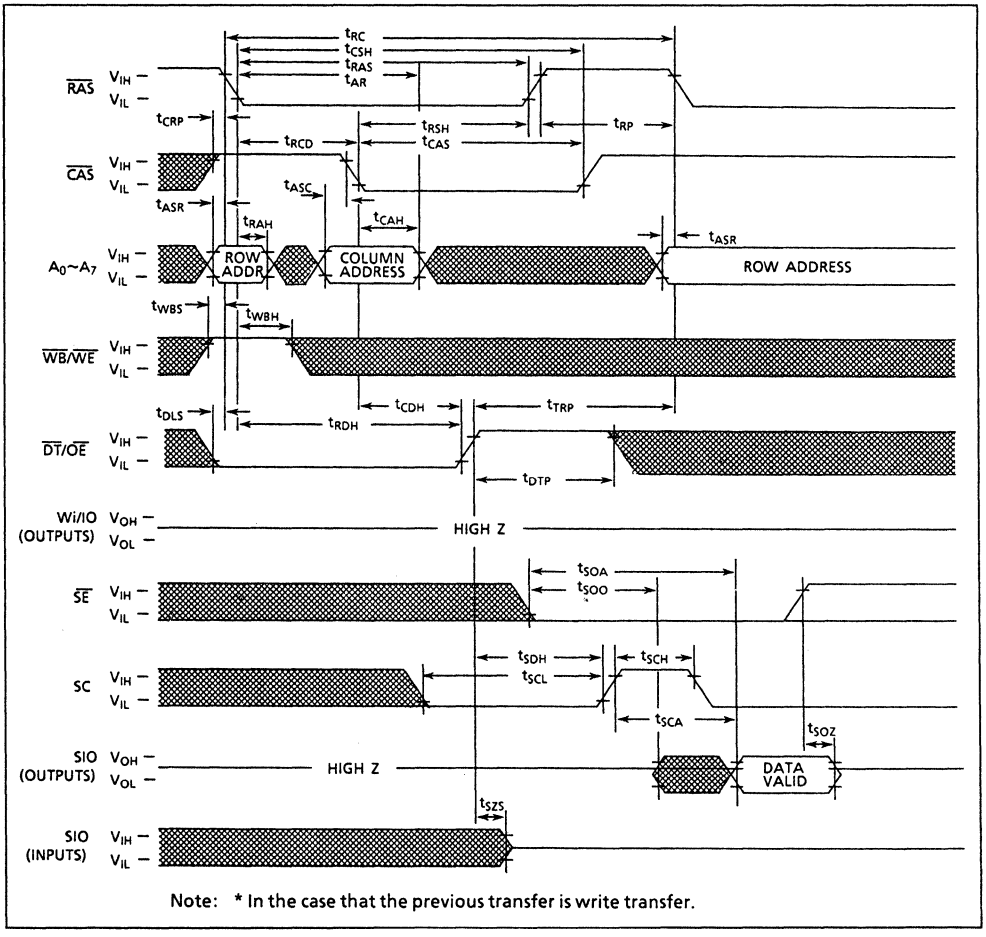
Hidden Refresh Cycle



$\overline{CAS}$ before RAS Refresh Cycle

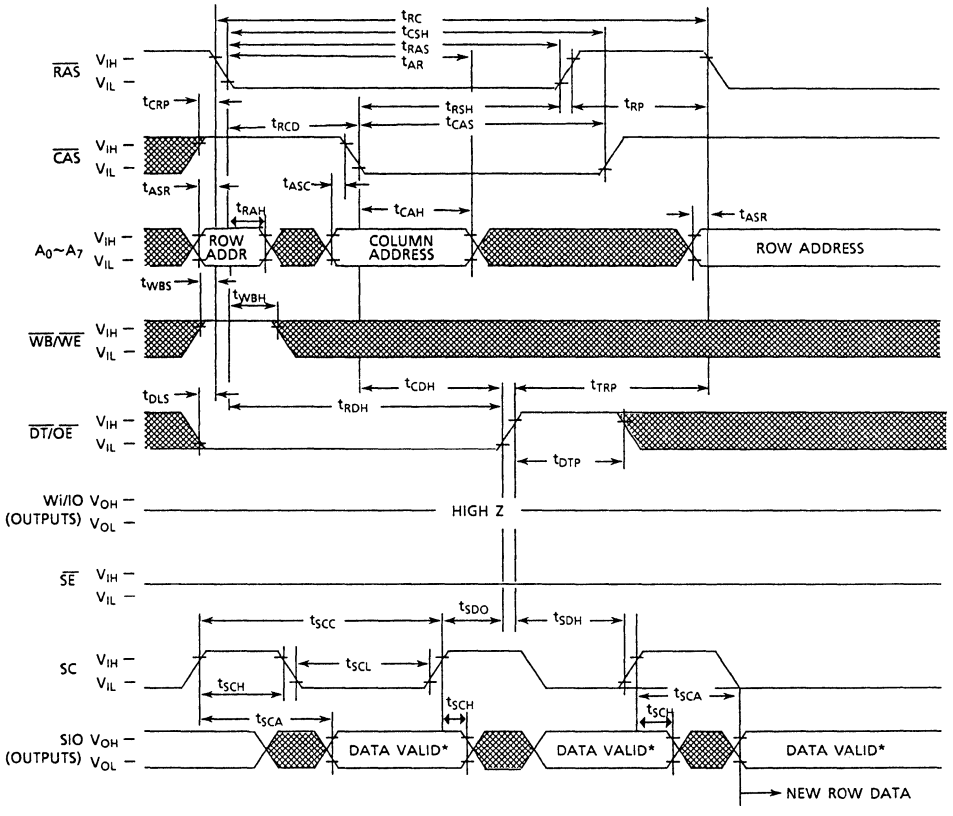


Read Transfer Cycle (RAM → SAM) Serial Read Setup*



Note: * In the case that the previous transfer is write transfer.

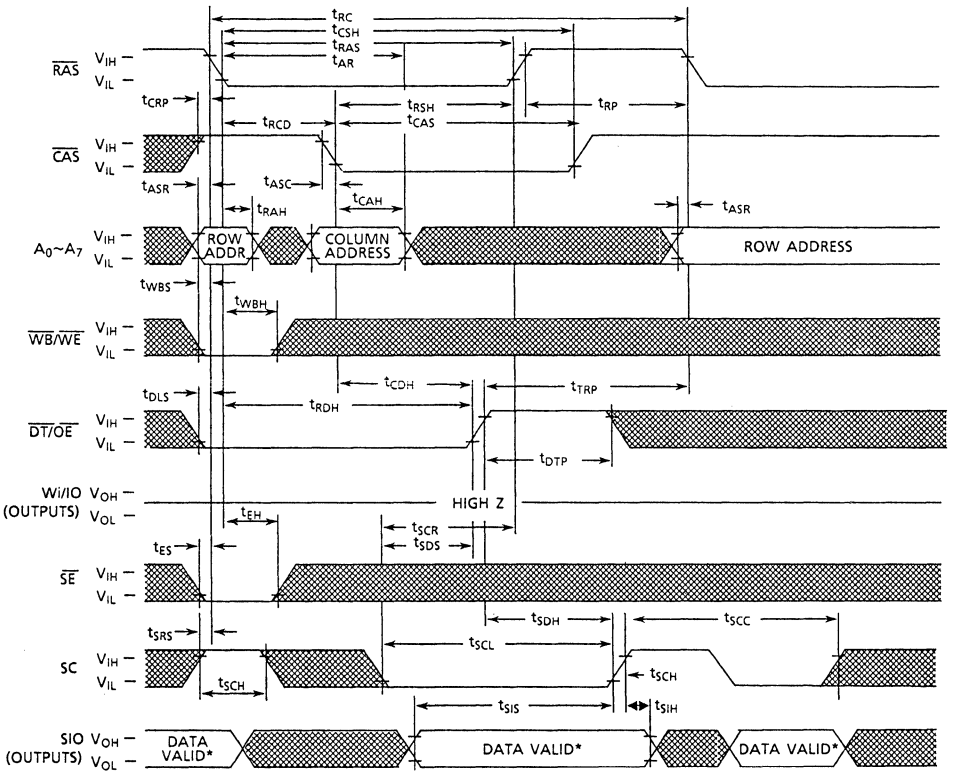
Read Transfer Cycle (RAM → SAM)



* Note: If SE is "H" level the serial input data are not written into the data register, but the serial data selector continues to function.

9

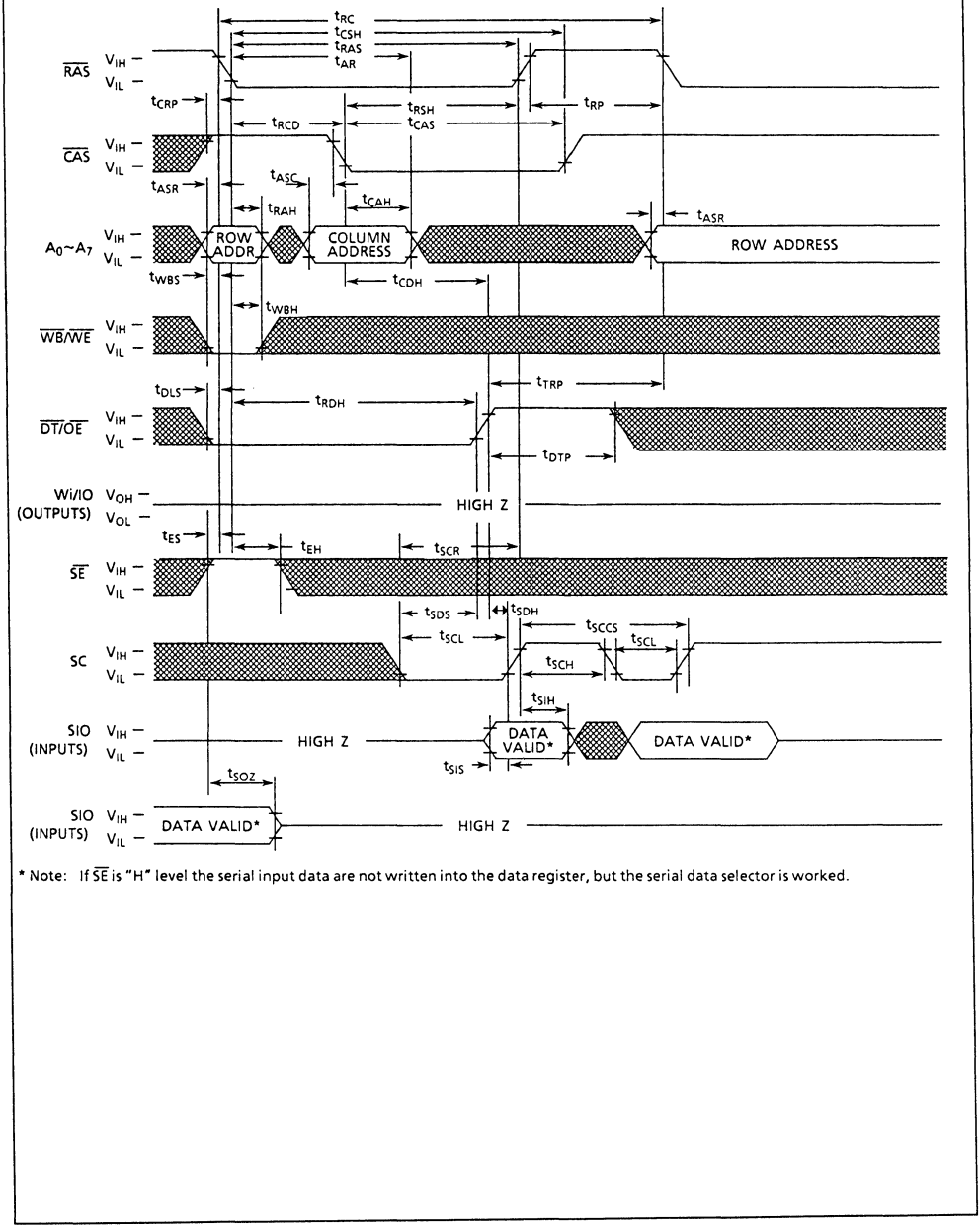
Write Transfer Cycle (SAM → RAM)



* Note: If SE is "H" level the serial input data are not written into the data register, but the serial data selector continues to function.

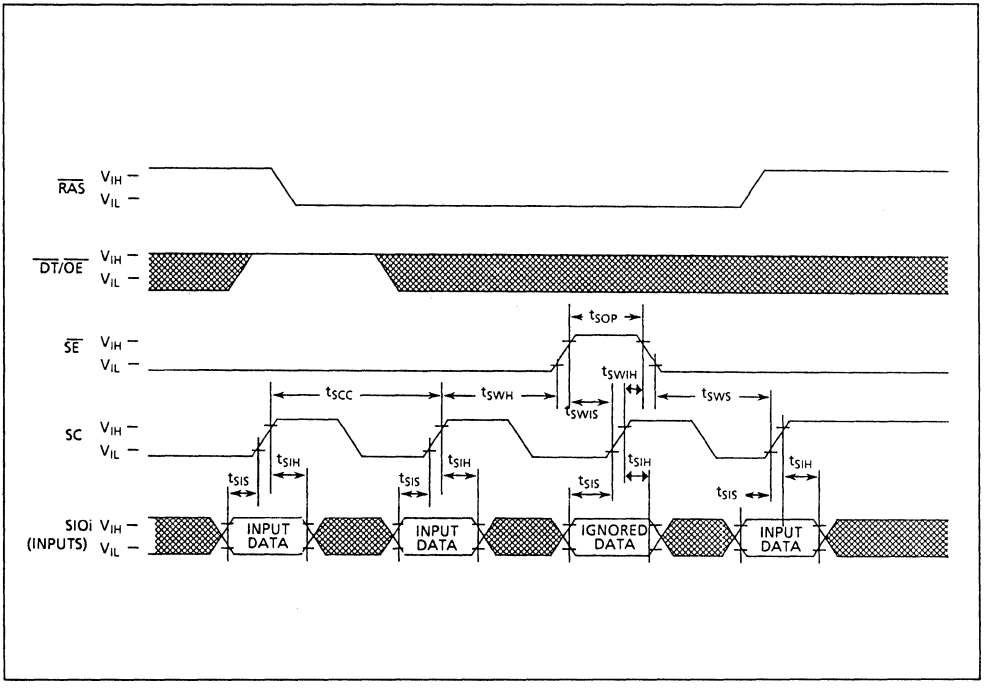
9

Pseudo Write Transfer Cycle Serial Write Setup

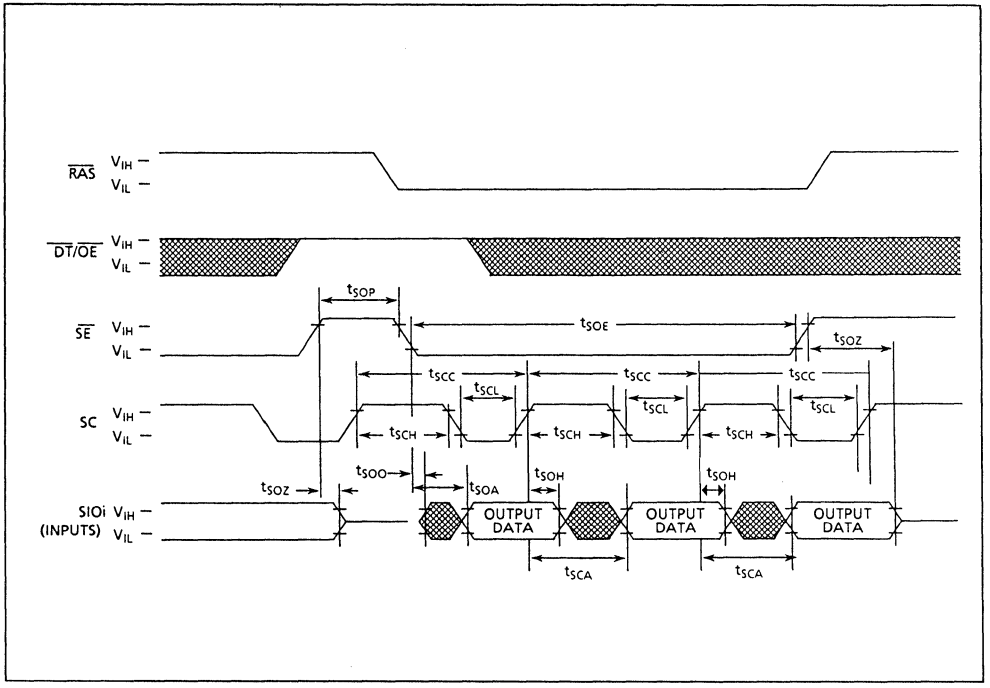


* Note: If $\overline{SE}$ is "H" level the serial input data are not written into the data register, but the serial data selector is worked.

Serial Write Cycle

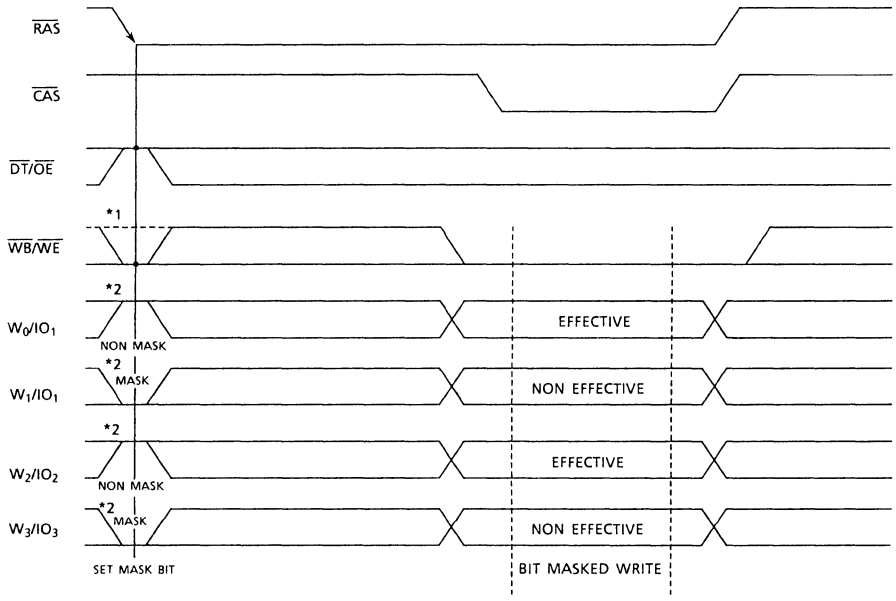


Serial Read Cycle



9

Bit Masked Write

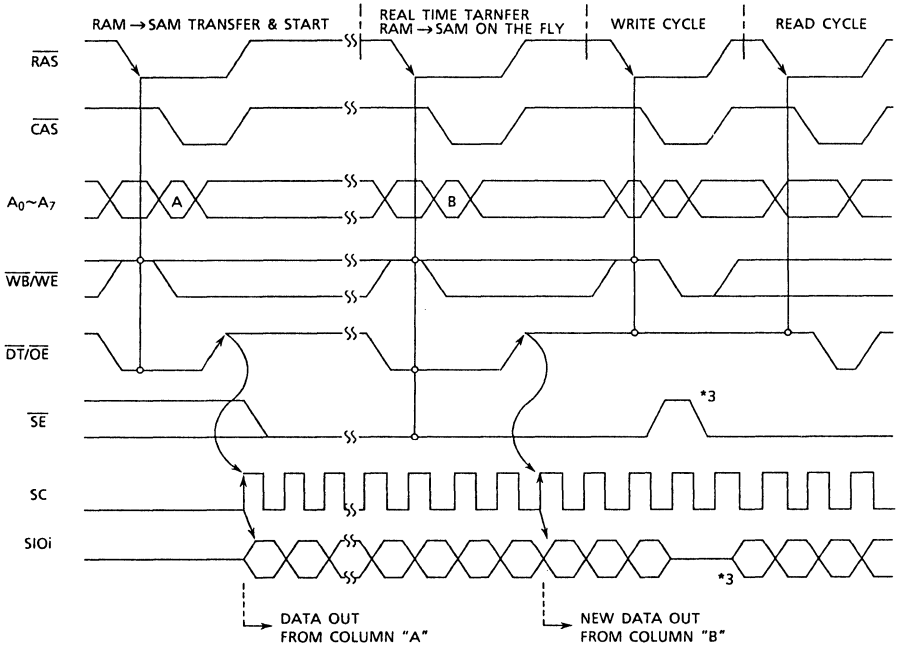


*1 If $\overline{WB}/\overline{WE}$ = "H" all 4 bits of data are written into RAM

*2 $W_{0\sim3}/IO_{0\sim3}$ = "H" Non masked
$W_{0\sim3}/IO_{0\sim3}$ = "L" Masked

9

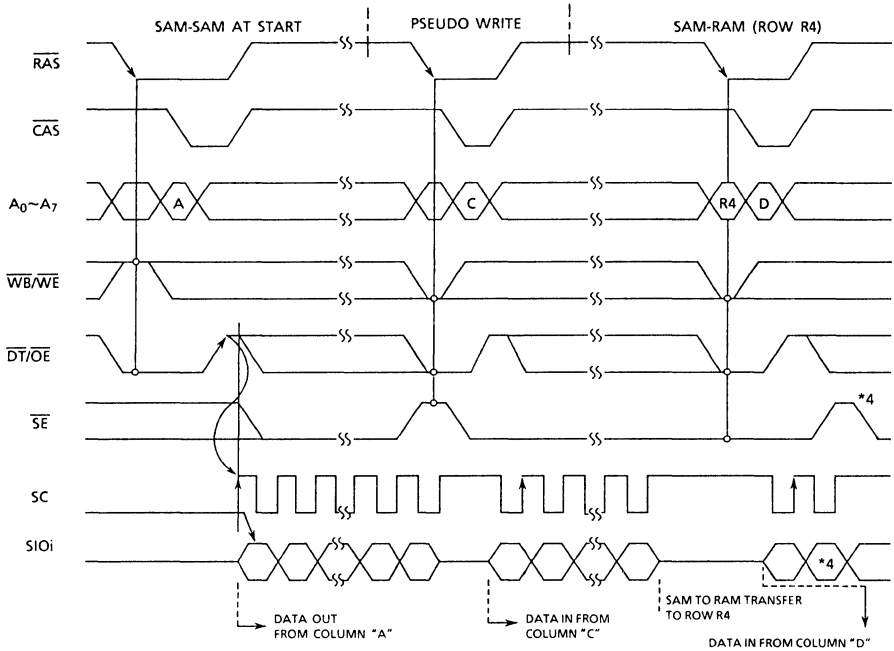
Serial Output Mode



*3 If $\overline{SE}$ goes "H" level SIOi enters the high impedance state, but the serial data selector continues to function.

9

Serial Input Mode



*4 If $\overline{SE}$ goes "H" level SIOi input data is ignored, but the serial data selector continues to function.

FUNCTIONAL DESCRIPTION

RAM Operation

The MSM51C262 is a CMOS dynamic memory with 2 ports. One port, the RAM port, operates in the same way as the 64K x 4 DRAM. The other port, the Serial Access Port (SAM), allows data to be either read from or written to the memory at very high data rates.

The MSM51C262 reads and writes data via the RAM port by multiplexing a 16 bit address into an 8 bit row and an 8 bit column address. The Row Address Strobe ($\overline{RAS}$) latches the row address on chip. The column address, however, flows through the internal column address buffer and is latched by the Column Address Strobe ($\overline{CAS}$) signal. Because column access time becomes primarily dependent upon a valid column address rather than the falling edge of $\overline{CAS}$, signal timing restrictions on $\overline{CAS}$ can be greatly loosened with no effect on access time.

Memory Cycle

A memory cycle is initiated by the falling edge of $\overline{RAS}$. A memory cycle may not be ended or aborted prior to fulfilling the t_{RAS} (min.) timing specification once it has been started. This precaution is necessary for proper device operation and integrity. A new memory cycle may not be started until the minimum precharge time t_{RP}/t_{CP} has been satisfied.

Read Cycle

A read cycle is a memory cycle in which data are retrieved from the memory array and presented on the Wi/IOi pins. Read cycles can take the form of single operations to a specific row and column address or page mode accesses to any of 256 column addresses within a single row.

Write Cycle

A write cycle is a memory cycle in which data supplied externally to Wi/IOi are written into the location in memory specified by the address. Using the masked write function, any combination of Wi/IOi lines may be written and the remainder ignored. Write cycles can take the form of single operations to a specific row and column address or page mode accesses to any of 256 column addresses within a single row.

Refresh Cycle

To retain the data in a MSM51C262 DRAM a refresh operation activating each of the 256 row addresses must be performed at least once every 4 ms. Any operation such as read, write, RMW, $\overline{RAS}$ only cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle or transfer cycle refreshes the addressed row.

Fast Page Mode Operation

Fast Page Mode permits an 256 columns of 4 bits within a selected row of the MSM51C262 to be randomly accessed at a high data rate. After a normal cycle initiation, maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to resupply it. The column buffer acts as a transparent latch data while $\overline{CAS}$ is high and, when $\overline{CAS}$ goes low, holds the addresses applied. Because of the transparent latches, the column address "flows through" and the read access begins upon stable addresses rather that the falling $\overline{CAS}$ edge. This eliminates t_{ASC} and t_T from the critical timing path and helps to speed up access while making operation simpler.

During a Fast Page Mode operation, read, write, read-modify-write, or read write-read cycles are possible to random addresses within a selected row. Multiple operations to the same address are permitted as well as more than 256 accesses to any combination of addresses within the selected row. The only limiting factor to the number of such Page Mode accesses is consideration of refresh timing. Following the entry cycle into Page Mode, access time is t_{CAA} or t_{CAP}-dependent. If the column address is valid before or coincident with the rising edge of $\overline{CAS}$, then t_{CAP} is the access controlling parameter. If the column address is valid after the rising edge of $\overline{CAS}$, access time is determined by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output buffers.

With Fast Page Mode, very high sustained data rates can be achieved. The following equation can be used to calculate the data rate possible:

$$\text{Data Rate} = \frac{256}{t_{RC} + 255t_{PC}}$$

Mode Selection

RAM Operation to be Performed	SAM Mode to be Entered	AControl Signals (Sampled at the falling edge of $\overline{RAS}$)					A_0~A_7 Sample Time	
		$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	$\overline{SE}$	$W/IO_{0\sim3}$	$\overline{RAS}$	$\overline{CAS}$
Read	Mode not affected	H	H	X	X	X	Row	Column Add.
Write	Mode not affected			H	X	X	Row	Column Add.
Bit Masked Write	Mode not affected			L	X	H*	Row	Column Add.
	Mode not affected			L	X	L*	Row	Column Add.
RAM → SAM Transfer	Output Mode		L	H	X	X	Row	SAM Start**
SAM → RAM Transfer	Input Mode			L	L	X	Row	SAM Start**
Pseudo Transfer	Input Mode			L	H	X	X	SAM Start**
$\overline{CAS}$-before-$\overline{RAS}$ or Hidden Refresh	Mode not affected	L	X	X	X	X	X	X

X = Don't care

* The state of the W/IO lines is sampled at the falling edge of $\overline{RAS}$ to set the Write Bit Mask Register. If W/IO is high at the falling edge of $\overline{RAS}$, no masking action is taken and the corresponding data bit will be subject to change by a write operation. If W/IO is low at the falling edge of $\overline{RAS}$, the corresponding bit is masked and will not be altered by a write operation.

** The 8 address signals, A_0 to A_7, are used to select the RAM row address that will be affected by a transfer to or from the SAM and the starting address for a SAM read or write operation. The falling edge of $\overline{RAS}$ strobes the row address, and the falling edge of $\overline{CAS}$ strobes the SAM starting address.

COMBINED RAM-SAM OPERATION

Transfer

The transfer operation of the MSM51C262 allows a row (256 bits) of data to be transferred between RAM and SAM in either direction. The signals and states that control the transfer operation are specified in the Mode Selection Table.

To start a serial write operation, it is necessary to cause the SIO_0 to SIO_3 pins of the SAM, port to be in a high-Z state. The pseudo write transfer cycle accomplishes this purpose and must be performed any time the SAM mode is to be changed from read to write. No data transfer takes place, but addresses are set up as in any other transfer cycle. A read transfer cycle (RAM to SAM) changes the mode from write to read.

SAM OPERATION

General

The Serial Access Memory (SAM) of the MSM51C262 is organized as 256 words x 4 bits per word. It is possible to load the SAM from two sources: the RAM and the external serial I/O lines, SIOi. SAM has two operational modes, read and write (viewed externally). Mode changes were described in the previous section.

When the SAM is in the read mode, data are first transferred from the RAM to SAM and then can be accessed serially via the SIOi lines beginning with any SAM address. The progression of data output is from lower to higher numbered bits and addresses are module 256.

When the SAM is in the write mode, data are captured into the SAM using the SIOi lines and can be written into a selected row in the RAM by a write transfer operation.

Read/Write

The SC pin is used as a 'shift clock' for the SAM port. Serial access is triggered by the rising edge of SC. When the SAM is in the write mode, the rising edge of SC causes data to be strobed into the selected cell of the SAM. In the read cycle, output data become valid after t_{SCA} from the rising edge of SC and remain valid until the next cycle. The SAM address is automatically incremented by SC.

The $\overline{SE}$ pin is used as an output/input enable pin for the SAM. It does not, however, gate the SC signal and the SAM address counter for read or write operations will continue to increment regardless of the state of $\overline{SE}$.

Real-time Read Transfer

The MSM51C262 offers real-time read transfer between RAM and SAM. By using this feature, a continuous data stream can be generated even if the row address must be changed. No loss of timing is caused by this transfer. The data transfer from the RAM to SAM is triggered by the rising edge of $\overline{DT}/\overline{OE}$ after the $\overline{RAS}/\overline{CAS}$ cycle has set up the data to be transferred and the start address. New row data is available for SAM output after DT/OE returns to a high state in compliance with specification parameters t_{SDD} and t_{SDH}. SC should be applied continuously and $\overline{DT}/\overline{OE}$ timed from SC to achieve non-stop transfer.

Write Transfer

When the SAM has been placed into a write mode, and the required data have been captured via SIOi, the write transfer operation will cause the content of the SAM to be written into the selected RAM row. After the write transfer cycle has been completed, more data can be written to the SAM via SIOi.

Power On

After application of the V_{CC} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified refresh interval. During Power On, the V_{CC} current requirement of the MSM51C262 is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is Low during Power On, the device will go into an active cycle, and I_{CC} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} or be held at a valid V_{IH} during Power On to avoid current surges.

OKI semiconductor
MSM514201

1,048,576-WORD x 1-BIT SERIAL REGISTER

GENERAL DESCRIPTION

MSM514201 is a serial register in 1,048,576 words x 1 bit configuration featuring medium speed operation with low power consumption.

MSM514201 has a built-in internal address generator circuit allowing continuous serial read/write operation by single external clock input. The internal address is automatically incremented or decremented by one by read/write operation. Address increment or decrement can be selected by external input.

Address designation in units of 1024 words in the direction of words is possible by an external serial address input.

A refresh timer and refresh counter are built in to eliminate the need of the external refresh circuit and to realize low power ocnsumption.

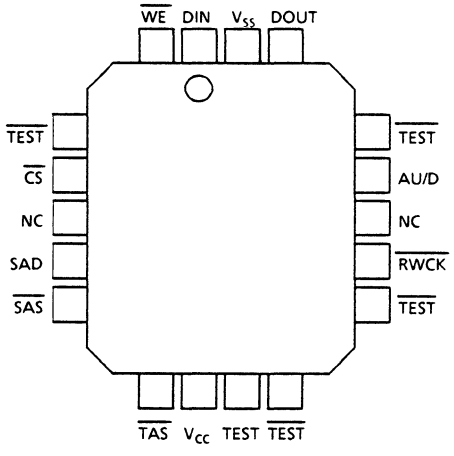
The standard 300 mil 18-pin plastic LCC is used as the package and the operating temperature range is between 0°C and 70°C.

MSM514201 is best suitable for holding large capacity data with battery backup. As solid state recording and playback system can easily be realized by combination with OKI's voice synthesizer LSI, MSM6388.

FEATURES

- Configuration : 1,048,576 x 1 bit
- Serial access operation : Serial access time 3.0 µs
  Serial read/write cycle time 4.0 µs
- Low current consumption : 100 µA max. (for data holding, V_{CC} = 4.0V)
- Wide operating supply voltage range : Single 3.5 to 5.5V
- Package : 18-pin PLCC
- Refresh operation : Self-refresh (refresh-free)
- Process : 1.2 µm standard N well CMOS process

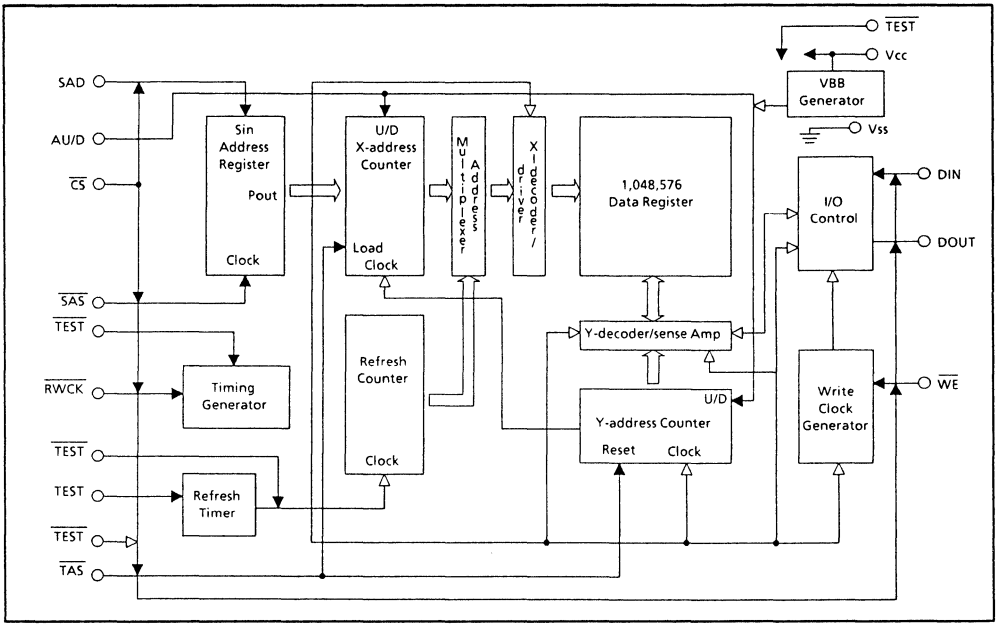
PIN ASSIGNMENT (Top View)



1 : Data input
2 : Write enable
3 : Test input
4 : Chip select
5 : No connection
6 : Serial address data
7 : Serial address strobe
8 : Transfer address strobe
9 : Power supply (+ 5V)
10 : Test input
11 : Test input
12 : Test input
13 : Read/write clock
14 : No connection
15 : Address up/down select
16 : Test input
17 : Data output
18 : Ground (0V)

9

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTIC

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating
Terminal voltage	V_T	Ta = 25°C, relative to V_{SS}	− 1.0~7.0V
Output short-circuit current	I_{OS}	Ta = 25°C	50 mA
Power dissipation	P_D	Ta = 25°C	1W
Operating temperature	Top	−	0~70°C
Storage temperature	Tstg	−	− 55~150°C

9

Recommended Operating Conditions

(Ta = 0~70°C)

Parameter	Symbol	MIN	TYP	MAX	Unit
Terminal voltage	V_{CC}	3.5	4.5	5.5	V
Terminal voltage	V_{SS}	0	0	0	V
"H" input voltage	V_{IH}	V_{CC} − 0.5	V_{CC}	V_{CC} + 0.5	V
"L" input voltage	V_{IL}	− 0.5	0	0.5	V

DC Characteristics

(V_{CC} = 3.5V~5.5V, Ta = 0~70°C)

Parameter	Symbol	Conditions	MIN	MAX	Unit
"H" output voltage	V_{OH}	I_{OH} = −0.5mA	V_{CC} − 0.5	−	V
"L" output voltage	V_{OL}	I_{OL} = 0.5mA	−	0.4	V
Input leakage current	I_{IL}	V_I = 0V~V_{CC}	−1	1	μA
Output leakage current	I_{OL}	V_O = 0V~V_{CC}	−1	1	μA
Supply current (in operating state)	I_{CC1}	V_{CC} = 4V, t_{RC} = 4μs	−	5	mA
Supply current (in standby state)	I_{CC2}	V_{CC} = 4V	−	100	μA

AC Characteristics

(V_{CC} = 3.5V~5.5V, Ta = 0~70°C)

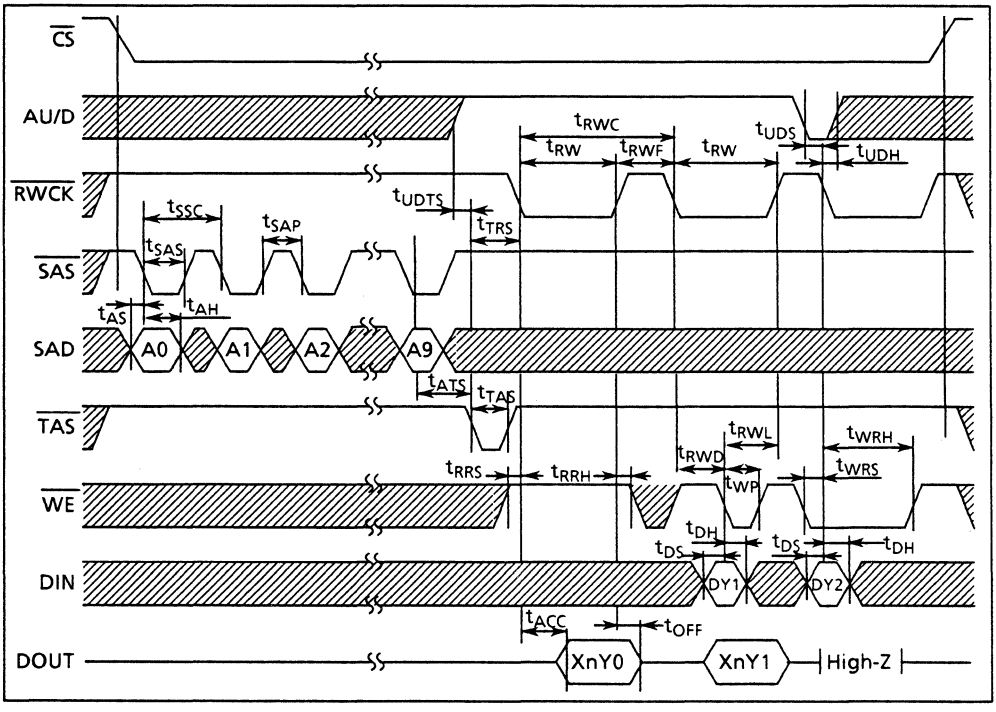
Parameter	Symbol	MSM514201		Unit
		MIN.	MAX.	
Refresh cycle	t_{REF}	−	−	ms
Read/write cycle time	t_{RWC}	4,000	−	ns
Access time	t_{ACC}	−	3,000	ns
Output turn off delay time	t_{OFF}	0	50	ns
Input signal rise/fall time	t_T	3	50	ns
$\overline{RWCK}$ precharge time	t_{RWP}	1,000	−	ns
$\overline{RWCK}$ pulse width	t_{RW}	3,000	10,000	ns
$\overline{SAS}$ cycle time	t_{SSC}	100	−	ns
$\overline{SAS}$ pulse width	t_{SAS}	50	−	ns
$\overline{SAS}$ precharge time	t_{SAP}	50	−	ns
Address setup time	t_{AS}	0	−	ns
Address hold time	t_{AH}	50	−	ns
$\overline{TAS}$ setup time	t_{ATS}	50	−	ns
$\overline{TAS}$ to $\overline{RWCK}$ setup time	t_{TRS}	50	−	ns
$\overline{TAS}$ pulse width	t_{TAS}	50	−	ns

AC Characteristics (Continued)

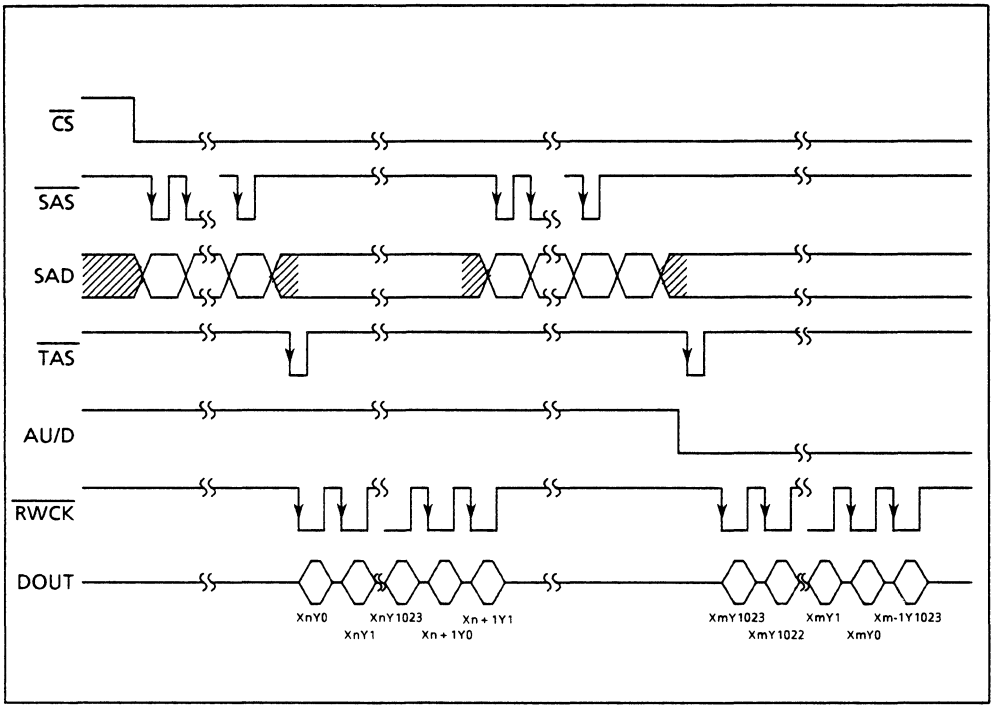
(V_{CC} = 3.5V~5.5V, Ta = 0~70°C)

Parameter	Symbol	MSM514201		Unit
		MIN.	MAX.	
Read command setup time	t_{RRS}	0	–	ns
Read command hold time	t_{RRH}	250	–	ns
Write command setup time	t_{WRS}	0	–	ns
Write command hold time	t_{WRH}	50	–	ns
Write command pulse width	t_{WP}	50	–	ns
Write command to $\overline{RWCK}$ lead time	t_{RWL}	50	–	ns
Data setup time	t_{DS}	0	–	ns
Data hold time	t_{DH}	50	–	ns
$\overline{RWCK}$ to $\overline{WE}$ delay time	t_{RWD}	100	–	ns
AU/D setup time	t_{UDS}	0	–	ns
AU/D hold time	t_{UDH}	50	–	ns
AU/D to $\overline{TAS}$ setup time	t_{UDTS}	0	–	ns

Read/Write/Read Modify Write Cycle



Address Up/Down Select Mode



PIN FUNCTIONS AND OPERATION MODES

Serial Address Input (SAD)

Pin for inputting the read/write starting address-Designation in units of 1024 words is possible. The 1,024 address data can be input as 10-bit (A0-A9) serial data from the SAD pin.

Serial address strobe ($\overline{SAS}$)

Pin for the clock used to store the serial address data into the internal register.

Address transfer strobe ($\overline{TAS}$)

Input pin for setting the serial address data stored in the address register to the internal address counter.

When the $\overline{TAS}$ falls, and the Y address is set to address 0 in the increment mode or to address 1023 in the decrement mode.

Read/write clock ($\overline{RWCK}$)

Input pin for the data register information read/write clock.

Internal operation starts at the following edges of $\overline{RWCK}$. The information in the data register is output to the DOUT pin in the read mode, and the information at the DIN pin is written into the data register in the write mode. The internal address counter is automatically incremented or decremented also when $\overline{RWCK}$ falls.

Write enable ($\overline{WE}$)

Input pin for selecting the read mode, write mode or read modify write mode.

The read mode is set when $\overline{WE}$ is "H", and the write mode is set when $\overline{WE}$ is "L". When $\overline{WE}$ falls from "H" to "L" while $\overline{RWCK}$ is active, the read modify write mode is set.

Data input (DIN)

Input pin for write data.

The information at the data input pin is stored at the falling edge of $\overline{RWCK}$ in the write mode, and at the falling edge of $\overline{WE}$ in the read modify write mode.

Data output (DOUT)

The data output pin is always in kept in the high impedance state when $\overline{RWCK}$ or $\overline{CS}$ is kept at "H". When "H" or "L" information is read in the read operation, the output pin is set to "H" or "L" and holds the read information until $\overline{RWCK}$ is again set to "H". In the early write mode the output pin maintains the high impedance state, so I/O common operation by connecting DIN and DOUT is possible.

Address up/down select (AU/D)

Input pin for selecting the direction of automatic address updating.

When the $\overline{TAS}$ signal is input with the AU/D pin set to "H", the internal address counters are set to the externally set address for X and to address 0 for Y. Then the address is incremented by 1 every time $\overline{RWCK}$ is input.

When the $\overline{TAS}$ signal is input with the AU/D pin set to "L", the internal address counters are set to the externally set address in the same way for X but set to address 1023 for Y. Then the address is decremented by 1 every time $\overline{RWCK}$ is input. In either case, the X address is automatically incremented or decremented by 1 when read/write operation for 1024 words ends. The AU/D pin setting change is possible in any read/write cycle so long as the timing specifications for t_{UDS}, t_{UDH} are satisfied.

Chip select ($\overline{CS}$)

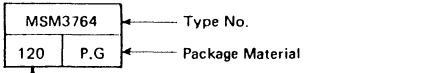
Input pin for disabling all input and output pins. This pin enables parallel use of multiple MSM514201s by connecting the data input and output pins.

CROSS REFERENCE LIST

10 CROSS REFERENCE LIST

1. DYNAMIC RAM 765
2. STATIC RAM 770
3. MASK ROM 771
4. EPROM 772
5. E^2 PROM (serial) 774
6. E^2 PROM 774
7. OTP 775

(Note)



1. DYNAMIC RAM (1/5)

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	64k	65536 x 1	16/18	MSM3764A-12	HM4864A-1		TMS4164A-12	MCM6665A-12	μPD4164A-4	TMM4164A-2	M5K4164A-12	MB8264A-12
				120 P.J	120 P.G		120 P.C	120 C	120 P.G.C	120 P	120 P.C	120 P.G
				MSM3764A-15	HM4864A-2		TMS4164A-15	MCM6665A-15	μPD4164A-3	TMM4164A-3	M5K4164A-15	MB8264A-15
				150 P.J	150 P.G		150 P.C	150 C	150 P.G.C	150 P	150 P.C	150 P.G
NMOS	256k	262144 x 1	16/18	MSM41256A-10				MCM6256-10				MB81256-10
				100 P.J				100 P.C				100 P
				MSM41256A-12	HM50256-12		TMS4256-12	MCM6256-12	μPD41256-12	TMM41256C-12	M5M4256S-12	MB81256-12
				120 P.J	120 P.G		120 P	120 P.C	120 P.G.C	120 P.G	120 P.C	120 P
				MSM41256A-15	HM50256-15		TMS4256-15	MCM6256-15	μPD41256-15	TMM41256C-15	M5M4256S-15	MB81256-15
				150 P.J	150 P.G		150 P	150 P.C	150 P.G.C	150 P.G	150 P.C	150 P
				MSM41257A-10					μPD41257-10			MB81257-10
				100 P.J					100 P.C			100 P.C
				MSM41257A-12	HM50257-12		TMS4257-12	MCM6257-12	μPD41257-12	TMM41257-12	M5M41257-12	MB81257-12
				120 P.J	120 P.C		120 P	120 P.C	120 P.C	120 P.C	120 P.C	120 P.C
				MSM41257A-15	HM50257-15		TMS4257-15	MCM6257-15	μPD41257-15	TMM41257-15	M5M41257-15	MB81257-15
				150 P.J	150 P.C		150 P	150 P.C	150 P.C	150 P.C	150 P.C	150 P.C

1. DYNAMIC RAM (2/5)

Structure	Total Bit	Organization	Number of Pin	Oki		Hitachi		Intel	Texas		Motorola	NEC		Toshiba		Mitsubishi		Fujitsu	
NMOS	256k	65536 x 4	18	MSM41464-10		HM50464P-10						μPD41464C-10						MB81464-10	
				100	P.J	100	P.J					100	P.J					100	P.J
				MSM41464-12		HM50464P-12						μPD41464C-12		TMM41464P-12				MB81464-12	
				120	P.J	120	P.J					120	P.J	120	P.J			120	P.J
				MSM41464-15		HM50464P-15						μPD41464C-15		TMM41464P-15				MB81464-15	
				150	P.J	150	P.J					150	P.J	150	P.J			150	P.J
CMOS	256K	262144 x 1	16(P) 18(J)	MSM51C256-8															
				80	P.J														
				MSM51C256-10															
				100	P.J														
CMOS	1M	1048576 x 1	18(P) 20(J) 20(Z)	MSM511000-10		HM511000-10			TMS4C1024-10					TC511000-10		M5M4C1000-10		M81C1000-10	
				100	P.J.Z	100	P		100	P				100	P	100	P	100	P
				MSM511000-12		HM511000-12			TMS4C1024-12					TC511000-12		M5M4C1000-12		M81C1000-12	
				120	P.J.Z	120	P		120	P				120	P	120	P	120	P
				MSM511001-10					TMS4C1025-10					TC511001-10		M5M4C1001-10		M81C1001-10	
				100	P.J.Z				100	P				100	P	100	P	100	P
				MSM511001-12		HM511001-12			TMS4C1025-12					TC511001-12		M5M4C1001-12		M81C1001-12	
				120	P.J.Z	120	P.J.Z		120	P				120	P	120	P	120	P

1. DYNAMIC RAM(3/5)

Structure	Total Bit	Organization	Number of Pin	Oki		Hitachi		Intel	Texas		Motorola	NEC		Toshiba		Mitsubishi		Fujitsu	
CMOS	1M	1,048,576 ×1	18(P)	MSM511002-10		HM511002-10			TMS4C1027-10					TC511002-10		M5M4C1002-10		MB81C1002-10	
				100	P.J.Z	100	P		100	P				100	P	100	P	100	P
			20(J)	MSM511002-12		HM511002-12			TMS4C1027-12					TC511002-12		M5M4C1002-12		MB81C1002-12	
			20(Z)	120	P.J.Z	120	P		120	P				120	P	120	P	120	P
		262,144 ×4	20	MSM514256-10		HM514256-10								TC514256-10		M5M44C256-10		MB81C4256-10	
				100	P.J.Z	100	P							100	P	100	P	100	P
				MSM514256-12		HM514256-12								TC514256-12		M5M44C256-12		MB81C4256-12	
				120	P.J.Z	120	P							120	P	120	P	120	P
				MSM514258-10		HM514258-10								TC514258-10		M5M44C258-10		MB81C4258-10	
				100	P.J.Z	100	P							100	P	100	P	100	P
				MSM514258-12		HM514258-12								TC514258-12		M5M44C258-12		MB81C4258-12	
				120	P.J.Z	120	P							120	P	120	P	120	P
		262,263 ×4	16	MSM514221-3					TMS4C1050-3										
				25	P.G				25	P.G.									
				MSM514221-6					TMS4C1050-6										
				30	P.G				50	P.G.									
		1,048,576 ×1	18(P) 20(J) 20(Z)	MSM511000A-80		HM511000A-8						μPD421000-80		TC511000A-80		M5M41000A-8		MB81C1000-80	
				80	P.J.Z	80	P.JP.ZP					80	C.LA.V	80	P.J.Z	80	P.J.L	80	C.P
				MSM511000A-10		HM511000A-10						μPD421000-10		TC511000A-10		M5M41000A-10		MB81C1000-10	
				100	P.J.Z	100	P.JP.ZP					100	C.LA.V	100	P.J.Z	100	P.J.L	100	C.P
				MSM511001A-80		HM511001A-8						μPD421001-80		TC511001A-80		M5M41001A-8		MB81C1001-80	
				80	P.J.Z	80	P.JP.ZP					80	C.LA.V	80	P.J.Z	80	P.J.L	80	C.P
				MSM511001A-10		HM511001A-10						μPD421001-10		TC511001A-10		M5M41001A-10		MB81C1001-10	
				100	P.J.Z	100	P.JP.ZP					100	C.LA.V	100	P.J.Z	100	P.J.L	100	C.P
				MSM511002A-80		HM511002A-8						μPD421002-80		TC511002A-80		M5M41002A-8		MB81C1002-80	
				80	P.J.Z	80	P.JP.ZP					80	C.LA.V	80	P.J.Z	80	P.J.L	80	C.P
				MSM511002A-10		HM511002A-10						μPD421002-10		TC511002A-10		M5M41002A-10		MB81C1002-10	
				100	P.J.Z	100	P.JP.ZP					100	C.LA.V	100	P.J.Z	100	P.J.L	100	C.P

1. DYNAMIC RAM (4/5)

Structure	Total Bit	Organization	Number of Pin	Oki	Hitachi	Intel	Texas	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
CMOS	1M	262,144 ×4	20	MSM514256A-80	HM514256A-8				μPD424256-80	TC514256A-80	M5M44256A-8	MB81C4256-80
				80 P.J.Z	80 P.JP.ZP				80 C.LA.V	80 P.J.Z	80 P.J.L	80 C.P
				MSM514256A-10	HM514256A-10				μPD424256-10	TC514256A-10	M5M44256A-10	MB81C4256-10
				100 P.J.Z	100 P.JP.ZP				100 C.LA.V	100 P.J.Z	100 P.J.L	100 C.P
				MSM514258A-80	HM514258A-8				μPD424258-80	TC514258A-80	M5M44258A-8	MB81C4258-80
				80 P.J.Z	80 P.JP.ZP				80 C.LA.V	80 P.J.Z	80 P.J.L	80 C.P
				MSM514258A-10	HM514258A-10				μPD424258-10	TC514258A-10	M5M44258A-10	MB81C4258-10
				100 P.J.Z	100 P.JP.ZP				100 C.LA.V	100 P.J.Z	100 P.J.L	100 C.P
NMOS	2048k	262,144 ×8	30	MSC2304-10								
				100 YS.KS								
				MSC2304-12								
				120 YS.KS								
				MSC2304-15								
				150 YS.KS								
	2304k	262,144 ×9	30	MSC2304-10								
				100 YS.KS								
				MSC2304-12	HM561003-12						MH25609-12	
				120 YS.KS	120 YS.KS						120 YS	
				MSC2304-15	HM561003-15						MH25609-15	
				150 YS.KS	150 YS.KS.						150 YS	
		262,144 ×8	30	MSC2307-10								
				100 YS.KS								
				MSC2307-12								
				120 YS.KS								
				MSC2307-15								
				150 YS.KS								
	2304k	264,144 ×9	30	MSC2307-10								
				100 YS.KS								

1. DYNAMIC RAM (5/5)

Structure	Total Bit	Organization	Number of Pin	Oki		Hitachi	Intel	Texas	Motorola	NEC	Toshiba	Mitsubishi	Fujitsu
NMOS	2304k	262,144 ×9	30	MSC2307-12									
				120	YS.KS								
				MSC2307-15									
				150	YS.KS								
CMOS	8M	1,048,576 ×8	30	MSC2313-10									
				100	YS.KS								
				MSC2313-12									
				120	YS.KS								
	9M	1,048,576 ×9	30	MSC2312-10									
				100	YS.KS								
				MSC2312-12									
				120	YS.KS								

2. STATIC RAM

Structure	Total Bit	Organi-zation	Number of Pin	Oki		Hitachi		NEC		Toshiba		Mitsubishi		Fujitsu		SONY		SHARP		Motorola	
CMOS	64k	8192 ×8	28	MSM5165A-10		HM6264-10		μPD4364-10		TC5565-10		M5M5165-10		MB8464-10		CXK5864-10				MCM6064-10	
				100	P	100	P	100	P	100	P	100	P	100	P	100	P			100	P
				MSM5165A-12		HM6264-12		μPD4364-12		TC5565-12		M5M5165-12				CXK5864-12				MCM6064-12	
				120	P	120	P	120	P	120	P	120	P			120	P			120	P
				MSM5165A-15		HM6264-15		μPD4364-15		TC5565-15		M5M5165-15		MB8464-15		CXK5864-15					
				150	P	150	P	150	P	150	P	150	P	150	P	150	P				
		16384 ×4	22	MSM5188-45		HM6288-45		μPD4362-45				M5M5188-45				CXK5464-45					
				45	P	45	P	45	P			45	P			45	P				
				MSM5188-55				μPD4362-55				M5M5188-55				CXK5464-55					
				55	P			55	P			55	P			55	P				
				MSM5188-70				μPD4362-70								CXK5464-70					
				70	P			70	P							70	P				
	256k	32768 ×8	28	MSM51257L-85		HM62256-85		μPD43256-85		TC55257-85		M5M5256-85								MCM60256-85	
				85	P	85	P	85	P	85	P	85	P							85	P
				MSM51257L-10		HM62256-10		μPD43256-10		TC55257-10		M5M5256-10		MB84256-10		CXK58256-10				MCM60256-10	
				100	P	100	P	100	P	100	P	100	P	100	P	100	P			100	P
				MSM51257L-12		HM62256-12		μPD43256-12		TC55257-12		M5M5256-12		MB84256-12		CXK58256-12		LH52256-12		MCM60256-12	
				120	P	120	P	120	P	120	P	120	P	120	P	120	P	120	P	120	P
Full CMOS	256k	32768 ×8	28	MSM51256-10						TC55256-10											
				100	P					100	P										
				MSM51256-12						TC55256-12											
				120	P					120	P										

3. MASK ROM

Structure	Total Bit	Organization	Number of Pin	Oki	Fujitsu	Hitachi	Matsushita	Mitsubishi	NEC	Suwaseiko	Sharp	Toshiba
NMOS	64K	8192 x 8	28	MSM3864				M5M2364	μPD2364E		LH2369	TMM2365
				250 P				250 P	200 P		200 P	200 P
	128k	16384 x 8	28	MSM38128A			MN23128	M5M23128	μPD23128A		LH23126	TMM23128
				250 P			200 P	250 P	200 P		200 P	200 P
	256k	32767 x 8	28	MSM38256A					μPD23256A			TMM23256
				150 P					200 P			150 P
				MSM38256			MN23257	M5M23256	μPD23256		LH23257	
				250 P			200 P	200 P	250 P		200 P	
CMOS	256k	32767 x 8	28	MSM53256	MB83256	HN623257			μPD23C256E	SMM6325	LH53257	TC53257
				150 P	250 P	150 P			150 P	250 P	250 P	150 P
	1M	131072 x 8	28	MSM531000	MB831000	HN62321	MN231000	M5M23C100	μPD23C1000	SMM23100	LH531000	TC531000C
				250 P	150 P	150 P	250 P	150 P	200 P	450 P	250 P	150 P
			32	MSM531001		HN62321A			μPD23C1001E		LH530800	TC531001C
				200 P		150 P			200 P		150 P	150 P
	4M	262144 x 16	40	MSM534000	MB834100A							
				200 P	200 P							
				MSM53400A	MB834100A							
				150 P	200 P							
		524288 x 8	32	MSM534001A	MB834000A	HN62304B	MN234002	M5M23C401	μPD23C4001E		LH534300	TC53400F
				150 P	200 P	200 P	200 P	250 P	250 P		150 P	200 P
		262144 x 16 or 524288 x 8	40	MSM534002A	MB834200A	HN62404	MN234000	M5M23C400	μPD23C4000A		LH534500	
				150 P	200 P	200 P	200 P	250 P	200 P		150 P	

CROSS REFERENCE

4. EPROM

Structure	Total Bit	Organization	Number of Pin	Oki		Hitachi		Intel		AMD		ATMEL		WSI		NEC		Toshiba		Mitsubishi		Fujitsu	
NMOS	64K	8192×8	28	MSM2764A		HN482764		i2764A		Am2764						μPD2764D		TMM2764AD		M5L2764K		MBM2764	
				120 150 200 250	G	200 250	G	200 250	G	200 250	G					200 250	G	150 200	G	200 250	G	200 250	G
	128K	16384×8	28	MSM27128A		HN4827128		i27128A		Am27128A						μPD27128D		TMM27128AD		M5L27128K		MBM27128	
				120 150 200 250	G	200 250	G	200 250	G	150 200	G					200 250	G	150 200	G	200 250	G	200 250	G
	256K	32768×8	28	MSM27256		HN27256		i27256		Am27256						μPD27256AD		TMM27256AD		M5L27256K		MBM27256	
				120 150 200 250	G	200 250	G	250	G	250	G					200 250	G	150 200	G	150 200 250	G	200 250	G
	512K	65536×8	28	MSM27512		HN27512		i27512		Am27512								TMM27512D		M5L27512K		MBM27512	
				120 150 200 250	G	250	G	250	G	250	G							150 200	G	250	G	250	G
CMOS	256K	32768×8	28	MSM27C256		HN27C256		i27C256				AT27C256				μPD27C256AD		TC57256AD		M5M27C256K		MBM27C256A	
				100 120 150 200	G	200 250	G	250	G			120 150 170 200	G			120 150 200	G	120 150	G	120 150 250	G	150 200 250	G
	256K	32768×8	28	MSM27C256H		HN27C256H						AT27HC256		WS57C256F									
				55 70	G	70 85	G					55 70 90	G	70	G								

EPROM

Structure	Total Bit	Organization	Number of Pin	Oki		Hitachi		Intel		AMD		ATMEL		WSI		NEC		Toshiba		Mitsubishi		Fujitsu	
NMOS / CMOS	1M	131072 ×8	32	MSM271000		HN27C101G		i27010		Am27C010						μPD27C1001D		TC571000D		M5M27C101		MBM27C1001	
				120 150 200	G	170 200 250	G	200	G	150 170 200	G					120 150 200	G	150 200	G	120 150 200	G	150 200 250	G
		65536 ×16	40	MSM271024 MSM27C1024		HN27C1024H		i27210		Am27C1024		AT27C1024				μPD27C1024D		TC571024D		M5M27C102		MBM27C1024	
				120 150 200	G	85 100	G	150	G	200 250 300	G	150 170 200	G			150 200	G	150 200	G	120 150 200	G	150 200 250	G
CMOS	2M	262144 ×8	32	MSM27C2000																M5M27C201			
				100 120 150	G															100 120 150	G		
		131072 ×16	40	MSM27C2048																M5M27C202			
				120 150 200	G															100 120 150	G		

5. E²PROM (SERIAL)

Structure	Total Bit	Organization	Number of Pin	Oki		ASAHI KASEI		HYUNDAI		GI		NS		CATALYST		EXEL		ICT		SEIKO		ROHM	
CMOS CMOS	1k	128 x 8 or 64 x16	8	MSM16811		AK93C46		HY93C46				NMC9346		CAT93C46		LX93C46		93C46		S-2914R		BR93C46	
				250	P	250	P	250	P			250	P	250	P	250	P	250	P	250	P	250	P
				MSM16911						ER5911				CAT59C11						S-2911R			
				250	P					250	P			250	P					250	P		
	2k	256 x 8 or 128 x 16	8	MSM16812		AK93C56								CAT35C102						S-2924R		BR93C56	
				250	P	250	P							250	P					250	P	250	P
				MSM16911						ER5912				CAT35C202						S-2921R			
				250	P					250	P			250	P					250	P		

6. E²PROM

Structure	Total Bit	Organization	Number of Pin	Oki		XICOR		SEEQ		ATMEL		CATALYST		Hitachi		NEC		Fujitsu		Mitsubishi		intel	
CMOS	16k	2048 x 8	24	MSM28C16A		X2816A		2816A				CAT28C16A											
				150 200	P	200 250 300	P	250 300 350	P			150 200	P										
	64k	8192 x 8	28	MSM28C64A		X28C64		28C64		AT28C64		CAT28C64A		HN58C65		μPD28C64C		MBM28C64		M5M28C64AP		2864A	
				120 150 200	P	150	P	250 300 350	P	150 200 250	—	150 200 250	P	250	P	200 250	P	250 350	P	150 200	P	200 250 350	P

7. OTP

Structure	Total Bit	Organization	Number of Pin	Oki		Hitachi		Intel		AMD		ATMEL		WSI		NEC		Toshiba		Mitsubishi		Fujitsu	
NMOS	64K	8192×8	28	MSM2764AZB				P2764A										TMM2464AP					
				150	P			250	P									200	P				
	128K	16384×8	28	MSM27128AZB		HN27128AP		P27128A										TMM24128AP					
				150	P	200	P	250	P									200	P				
	256K	32768×8	28	MSM27256ZB		HN27256P		P27256A										TMM24256BP		M5M27256P			
				170	P	250	P	250	P									170 200	P	250	P		
	512K	65536×8	28	MSM27512ZB		HN27512P		P27512								µPD27C512C		TMM24512AP		M5M27512P			
				200	P	250	P	250	P							150 200	P	200 250	P	250	P		
CMOS	256K	32768×8	28	MSM27C256ZB														TC54256AP		M5M27C256P		MBM27C256AP	
				150	P													200	P	200	P	200	P
NMOS / CMOS	1M	131072 ×8	32	MSM271000ZB		HN27C101												TC541000P		M5M27C100P			
				200	P	200	P											200	P	200	P		
		65536 ×16	40	MSM271024ZB																M5M27C102P			
				170	P															200	P		

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APPLICATIONS

11 APPLICATIONS

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CMOS RAM BATTERY BACK-UP

A practical example of formation of non-volatile data by CMOS static RAM battery back-up is outlined below.

1. System power and battery switching circuit

The simplest RAM power supply (CMOS Vcc) is outlined in Fig. 1. In this case, the CMOS Vcc for normal operation is kept at a voltage 0.7V below the system voltage by the voltage drop across a diode (forward direction).

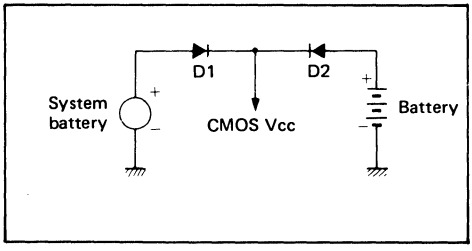


Fig. 1

Fig. 2 is an example of use of a chargeable Ni-Ca battery as the back-up battery. While the system power is being employed, the Ni-Ca battery is gradually charged up via Rc. As in Fig. 1, the diode voltage drop also poses a problem in this circuit.

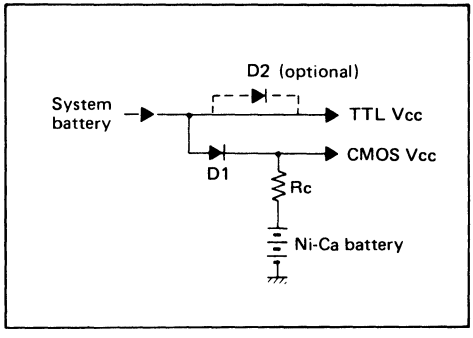


Fig. 2

The conditions for formation of non-volatile data (data retention) by battery back-up are listed below.

(1) The input signal H level must not exceed Vcc + 0.3V when the CMOS RAM Vcc power voltage is dropped.

(2) $\overline{CE}$ (or $\overline{CS}$) must maintain CMOS Vcc "H" level.

(3) In order to minimize power consumption, $\overline{WE}$, AD, DIN (or I/O) must be set to GND level or to the same "H" level as CMOS Vcc. (This is not necessary, however, for CMOS RAMs with chip select floating capability).

Note: $\overline{CS}$ floating capability
Power down possible irrespective of other input levels when memory has not been selected (i.e. when $\overline{CS}$ = H).

Consequently, if the TTL Vcc level is greater than the CMOS RAM supply voltage, and the RAM driver is at the TTL Vcc level, the CMOS RAM input voltage will exceed CMOS Vcc + 0.3V (a situation which must be avoided). Therefore, in order to reduce the voltage difference between CMOS Vcc and TTL Vcc with the battery voltage set to at least 4.5V or 4.75V (due to the RAM operating supply voltage range), the D2 diode may be added to obtain a system voltage level at least 0.7V above 4.5 ~ 4.75V (which will keep CMOS Vcc and TTL Vcc within the respective CMOS and TTL operating supply voltage ranges).
To cope with (1) and (3), a CMOS driver which will also operate at a low voltage Vcc during data hold may be employed, or else, the open collector and open drain buffer may be pulled up to CMOS Vcc in order to drive the RAM.
A control circuit for coping with (2) when an abnormal system power supply is detected is also required.

2. Switching Circuit Modifications

Modification of the diode switching circuit can employ PNP transistors. Voltage drops by PNP transistor V_{CE} are smaller by about 0.2V, and this can lead to the generation of a system "power fail" signal.

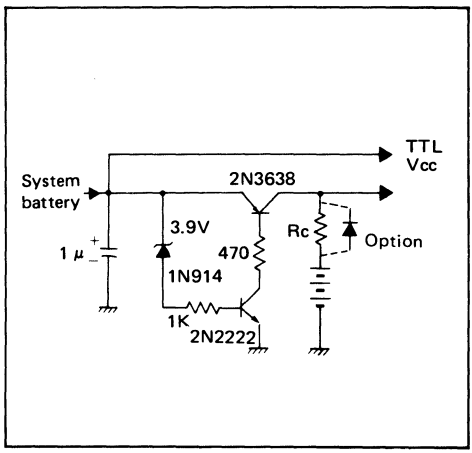
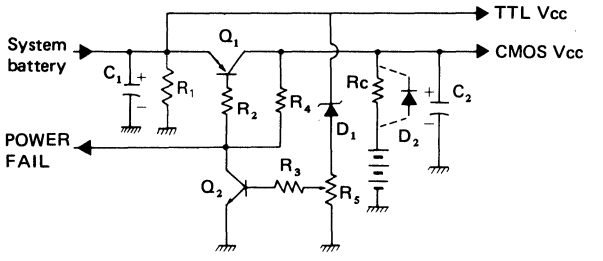


Fig. 3

Fig. 3 outlines a switching circuit employing a PNP transistor. The Rc used when a chargeable battery is employed is replaced by a diode when a non-chargeable battery is used. In this case, switching occurs at the zener diode voltage, so "power fail" must be detected by another circuit, and $\overline{CE}$ set to CMOS Vcc "high" level.

■ APPLICATIONS ■

Figs. 4 and 5 are examples of circuits capable of generating a POWER FAIL output signal. In these circuits, the C2 capacitance must be rather large, the important point being the need for a smooth gradual change in CMOS Vcc when the system power is cut. See next page for further details.



Q_1 : 2N2907 or 2SA495
Q_2 : 2N2222 or 2SC372
R_1 : 10K
R_3 : 1K R2 : 100
R_5 : 500 R4 : 47K
D_1 : 3.6V Rc : 200
Ni-Cad : 3.6V (70mAH)

Fig. 4

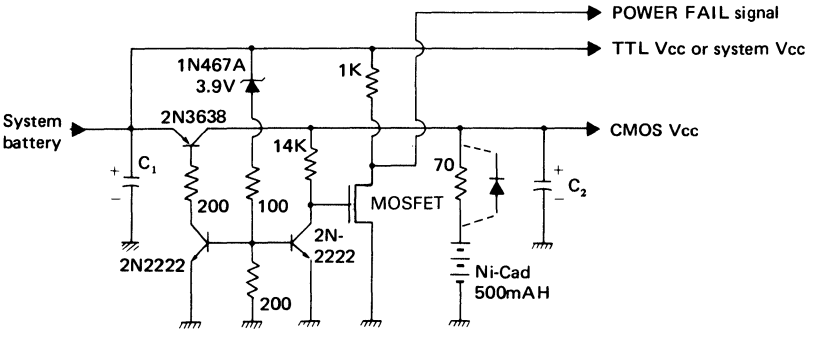
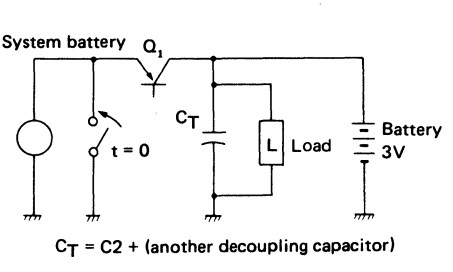


Fig. 5



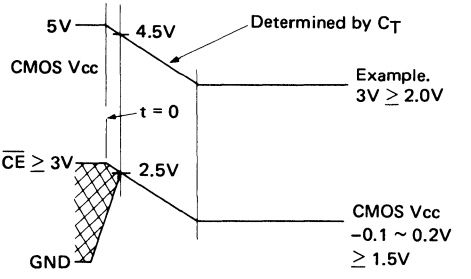


Fig. 6

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3. Data Retention Mode

The RAM driver (peripheral circuit) is determined according to conditions (1) and (3) required for data retention. In Oki Electric CMOS RAMs, the power voltage during data retention is kept at a minimum of 2.0V. The $\overline{CE}$ (or $\overline{CS}$) voltage at this time has to be kept at about Vcc −0.2V. And as was mentioned earlier, the CMOS Vcc must drop smoothly when the system power is cut until it reaches the power voltage for data retention (practically equivalent to the battery voltage, or else reduced by the diode voltage drop). And although $\overline{CE}$ traces the slope of CMOS Vcc reduction at this time, a smooth change in $\overline{CE}$ is also a necessary condition for actual circuits.

(4) When switching to retention mode, or from retention mode to operation mode, $\overline{CE}$ must exhibit a smooth change. If noise is generated in $\overline{CE}$ in this case, the data will be subject to rewriting.

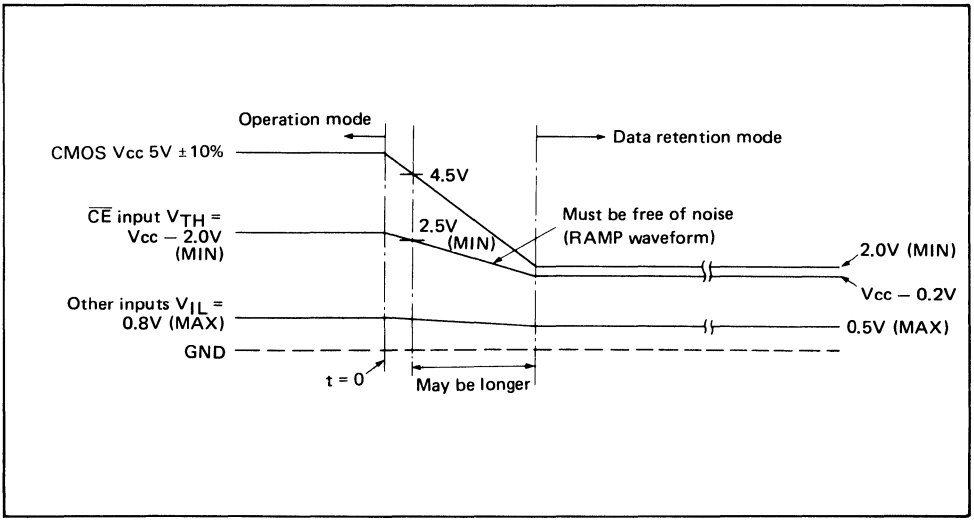

Fig. 7

(5) When switching to operation mode, commence operation after elapse of t_{RC} (read cycle time) following Vcc reaching the operating power voltage range.

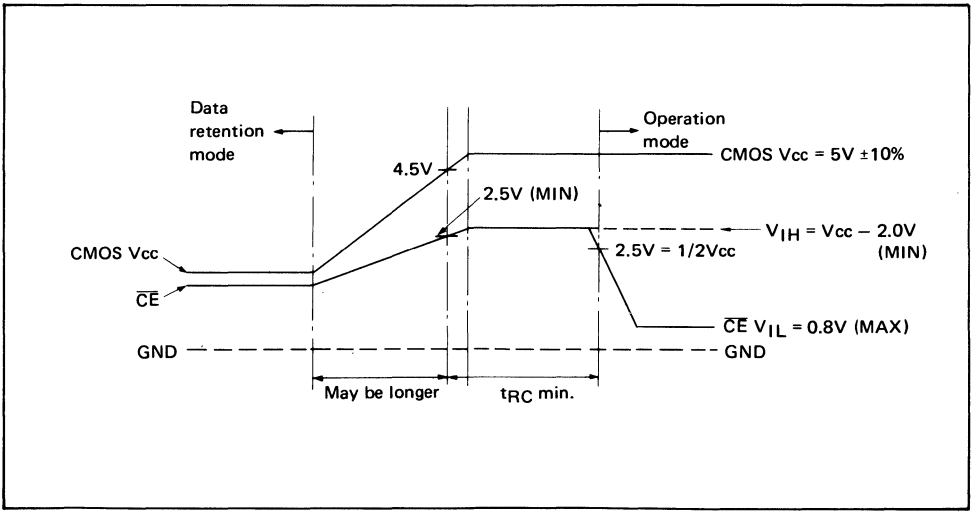

Fig. 8

4. Interfacing

A) TTL Interface

In the case of CMOS RAM drive by TTL, use an open-collector type TTL according to conditions (1) and (3).

When the system power line (i.e. TTL Vcc) is cut, the open-collector TTL Q2 in Fig. 9 is turned off, followed by Q1 also being turned off, resulting in the CMOS RAM input being pulled-up to CMOS Vcc.

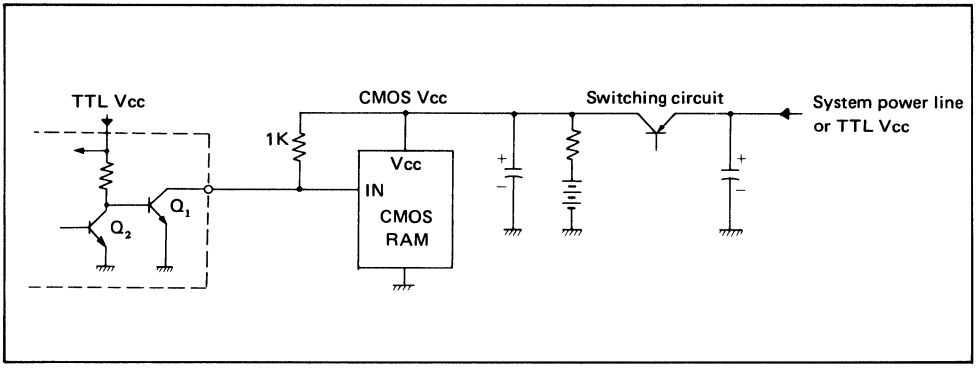

Fig. 9

When the power line voltage in LS type TTL is dropped to ground, the output is also dropped to ground, thereby making the pull-up resistors for address line buffers etc no longer necessary. In this case, however, it will not be possible to employ this as a control line buffer which must be switched to "high" during $\overline{CE}$ (or $\overline{CS}$) data retention.

(6) In order to minimize the consumption current during data retention, all inputs except $\overline{CE}$ (or $\overline{CS}$, this being designated as either "high" or "low") must be maintained at either GND or CMOS Vcc. (This does not apply, however, for CMOS RAMs equipped with $\overline{CS}$ floating function).

B) CMOS Interface

In systems where the CMOS RAM is driven by CMOS buffer, operation must be at the data retention power voltage, and the corresponding output voltage must satisfy the requirements indicated in Figs. 7 and 8.

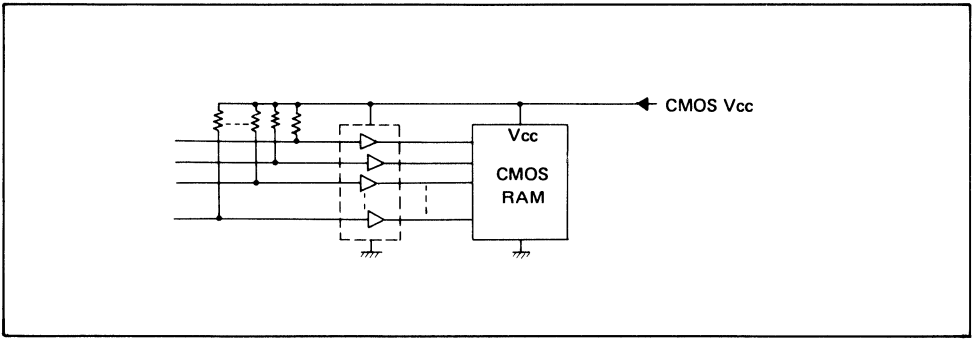

Fig. 10

5. Miscellaneous

In order to further reduce power consumption during data retention by even a small margin, the use of a MOS FET as the transistor generating the POWER FAIL output signal is recommended. This is in order to prevent flow of current from the 14kΩ resistor.

APPLICATION NOTE OF KANJI GENERATION MASK ROM

1. KANJI GENERATION MEMORIES

	IC models	Number of codes	Character storing capacity	Config-uration	Character style	Bit capacity	Access time	Scan system
Middle speed memories	MSM38256-19 ~ MSM38256-22	4	JIS standard No. 1	15 x 16	OKI gothic	256K bits	250ns	Row scan system
	MSM38256-32 ~ MSM38256-35	4	JIS standard No. 2	15 x 16	OKI gothic			
	MSM38256-10 ~ MSM38256-18	9	JIS new standard No. 1	24 x 24	JIS new standard character style C6234-1983			
	MSM38256-38 ~ MSM38256-46	9	JIS new standard No. 2	24 x 24				
	MSM531000-11	1	JIS new standard No. 1	15 x 16	OKI gothic	1M bits		
	MSM531000-12,13	2	JIS new standards No. 1 and No. 2					
	MSM531000-05 ~ MSM531000-07	3	JIS new standard No. 1	24 x 24	JIS new standard character style C6234-1983			
	MSM531000-08 ~ MSM531000-10	3	JIS new standard No. 2					

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2. MSM38256 SERIES

2-1 15 x 16 Font

(1) Model names

MSM38256-19~22 (four codes); JIS standard No. 1 (2,965 characters) + Non-kanji (524 characters)

MSM38256-32~35 (four codes); JIS standard No. 2 (3,384 characters)

These models are similar in electrical characteristics to the MSM38256 mask ROM. The CS and OE signals became active at "LOW".

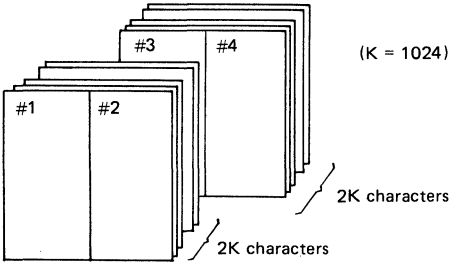
(2) Split character patterns, and their storage

• Split character patterns

				#1, #3								#2, #4							
A_3	A_2	A_1	A_0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	■									■						
0	0	0	1		■								■						
0	0	1	0			■							■						
0	0	1	1										■						
0	1	0	0	■				■	■	■	■	■	■	■	■	■	■	■	■
0	1	0	1		■			■	■	■	■	■	■	■	■	■	■	■	■
0	1	1	0			■		■	■	■	■	■	■	■	■	■	■	■	■
0	1	1	1					■	■	■	■	■	■	■	■	■	■	■	■
1	0	0	0					■	■	■	■	■	■	■	■	■	■	■	■
1	0	0	1			■		■	■	■	■	■	■	■	■	■	■	■	■
1	0	1	0			■							■						
1	0	1	1			■							■						
1	1	0	0		■								■						
1	1	0	1		■								■						
1	1	1	0	■									■						
1	1	1	1										■						

- The character patterns are standard OKI character patterns.
- Each character consists of two chips.
- Character data is generated at high level, and background data is generated at low level.
- Character data is stored in a 16 x 16 dot pattern area, left-justified.

• Storage



- Each group of four chips forms one set to store about 4K characters.

	#1	#2	#3	#4
JIS standard No. 1	MSM38256-19	MSM38256-20	MSM38256-21	MSM38256-22
JIS standard No. 2	MSM38256-32	MSM38256-33	MSM38256-34	MSM38256-35

(3) Address code conversions

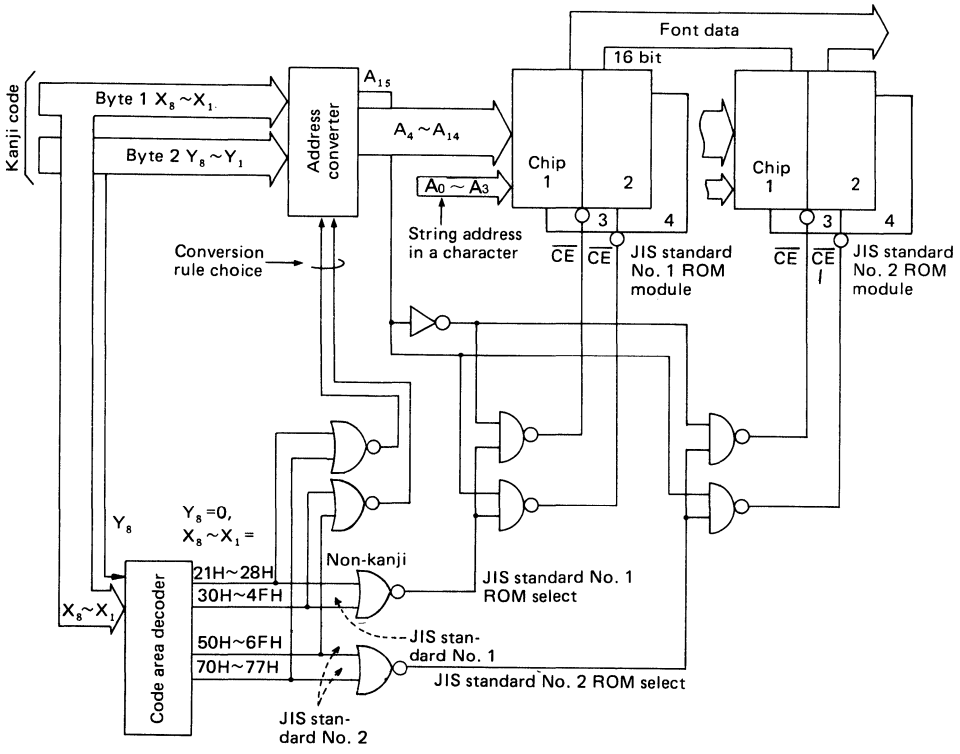
Convert the address code as indicated below to access character patterns with the kanji codes JIS 6226 and JIS 6220.

	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

Type of character \ code	C6226			ROM address											
	X_7	X_6	X_5	A_{15}*	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4
Non-kanji (sections 1 ~ 15)	0	1	0	Y_7	Y_6	X_3	X_2	X_1	0	0	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 1 kanji (sections 16 ~ 31)	0	1	1	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 1 kanji (sections 32 ~ 47)	1	0	0	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 2 kanji (sections 48 ~ 63)	1	0	1	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 2 kanji (sections 64 ~ 79)	1	1	0	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 2 kanji (sections 80 ~ 90)	1	1	1	Y_7	Y_6	X_3	X_2	X_1	0	0	Y_5	Y_4	Y_3	Y_2	Y_1

* Use A_{15} as a CE control signal because it is not supported as a ROM address. (For further details, see the circuit example.)

(4) 15 x 16 font circuit configuration example



2-1 24 x 24 Font

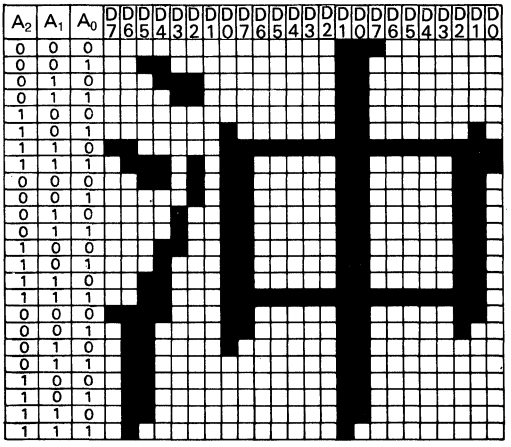
(1) Model names

MSM38256-10~18 (nine codes); JIS new standard No. 1 (2,965 characters) + Non-kanji (524 characters) + Half-size characters (159 characters).

These models are similar in electrical characteristics to the MSM38256 mask ROM. The CS and OE signals became active at "LOW".

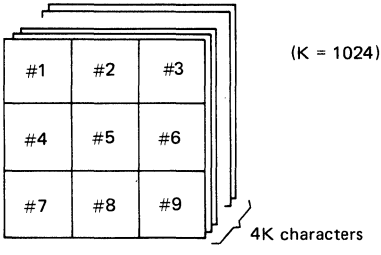
(2) Split character patterns, and their storage

• Split character patterns



- The character patterns are standard JIS character patterns.
- Each character consists of nine chips.
- Character data is generated at high level, and background data is generated at low level.

• Storage



	JIS standard No. 1	JIS standard No. 2
#1	MSM38256-10	MSM38256-38
#2	MSM38256-11	MSM38256-39
#3	MSM38256-12	MSM38256-40
#4	MSM38256-13	MSM38256-41
#5	MSM38256-14	MSM38256-42
#6	MSM38256-15	MSM38256-43
#7	MSM38256-16	MSM38256-44
#8	MSM38256-17	MSM38256-45
#9	MSM38256-18	MSM38256-46

(3) Address code conversions

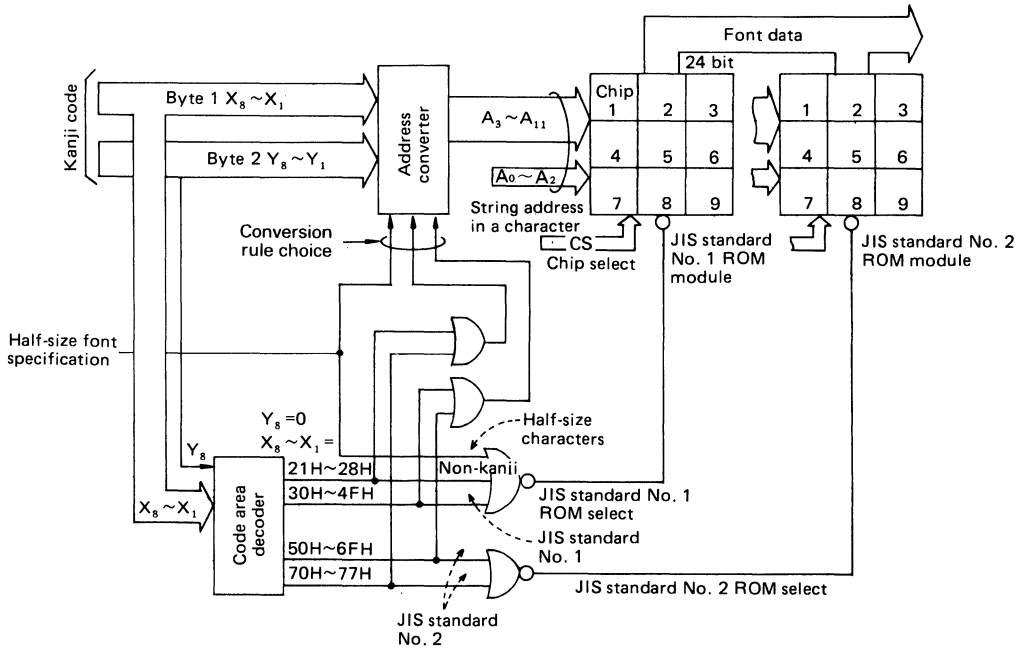
Convert the address code as indicated below to access character patterns with the kanji codes JIS6226 and JIS6220.

	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

C6220	Z_8	Z_7	Z_6	Z_5	Z_4	Z_3	Z_2	Z_1

Type of character \ code	C6226			ROM address											
	X_7	X_6	X_5	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3
Non-kanji (sections 1 ~ 15)	0	1	0	Y_7	Y_6	X_3	X_2	X_1	0	0	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 1 kanji (sections 16 ~ 31)	0	1	1	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 1 kanji (sections 32 ~ 47)	1	0	0	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 2 kanji (sections 48 ~ 63)	1	0	1	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 2 kanji (sections 64 ~ 79)	1	1	0	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 2 kanji (sections 80 ~ 94)	1	1	1	Y_7	Y_6	X_3	X_2	X_1	0	0	Y_5	Y_4	Y_3	Y_2	Y_1
Half size character	—	—	—	0	0	Z_8	Z_7	Z_6	0	0	Z_5	Z_4	Z_3	Z_2	Z_1

(4) 24 x 24 font circuit configuration example



3. MSM531000 SERIES

3-1 15 x 16 Font

(1) Model names

MSM531000-11RS (one code); JIS standard No. 1 (2,965 characters) + Non-kanji (524 characters) + Half-size character (204 characters) + Special character (200 characters)

(2) Split character patterns, and their storage

• Split character patterns

				$A_{16}=0$								$A_{16}=1$							
A_3	A_2	A_1	A_0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	■										■					
0	0	0	1		■									■					
0	0	1	0			■								■					
0	0	1	1											■					
0	1	0	0	■								■	■	■	■	■	■	■	■
0	1	0	1		■							■	■	■	■	■	■	■	■
0	1	1	0			■						■	■	■	■	■	■	■	■
0	1	1	1									■	■	■	■	■	■	■	■
1	0	0	0									■	■	■	■	■	■	■	■
1	0	0	1				■					■	■	■	■	■	■	■	■
1	0	1	0				■					■	■	■	■	■	■	■	■
1	0	1	1				■					■	■	■	■	■	■	■	■
1	1	0	0			■						■	■	■	■	■	■	■	■
1	1	0	1			■						■	■	■	■	■	■	■	■
1	1	1	0	■								■	■	■	■	■	■	■	■
1	1	1	1									■	■	■	■	■	■	■	■

- The character patterns are standard OKI character patterns.
- Each character consists of one chip.
- Character data is generated at high level, and background data is generated at low level.
- Character data is stored, right-justified.

(3) Address code conversions

Convert the address code as indicated below to access character patterns with the kanji codes JIS6226 and JIS6220.

	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

C6220	Z_8	Z_7	Z_6	Z_5	Z_4	Z_3	Z_2	Z_1

Type of character \ code	C6226			ROM address											
	X_7	X_6	X_5	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4
Non-kanji (sections 1 ~ 15)	0	1	0	Y_7	Y_6	X_3	X_2	X_1	0	0	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 1 kanji (sections 16 ~ 31)	0	1	1	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 1 kanji (sections 32 ~ 47)	1	0	0	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
Half size character	—	—	—	0	0	Z_8	Z_7	Z_6	0	0	Z_5	Z_4	Z_3	Z_2	Z_1

3-2 15 x 16 Font

(1) Model names
MSM531000-12, 13RS (two codes); JIS standard No. 1 (2,965 characters) + Non-kanji (524 characters) + JIS standard No. 2 (3,388 characters) + Special graphic characters (404 characters) + IBM kanji (360 characters)

(2) Split character patterns, and their storage
• Split character patterns

				531000-12								531000-13							
A_3	A_2	A_1	A_0	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	■										■					
0	0	0	1		■									■					
0	0	1	0			■								■					
0	0	1	1				■							■					
0	1	0	0	■				■	■	■	■	■	■	■	■	■	■	■	■
0	1	0	1		■			■	■	■	■	■	■	■	■	■	■	■	■
0	1	1	0			■		■	■	■	■	■	■	■	■	■	■	■	■
0	1	1	1				■	■	■	■	■	■	■	■	■	■	■	■	■
1	0	0	0					■	■	■	■	■	■	■	■	■	■	■	■
1	0	0	1					■	■	■	■	■	■	■	■	■	■	■	■
1	0	1	0					■						■					
1	0	1	1					■						■					
1	1	0	0						■					■					
1	1	0	1						■					■					
1	1	1	0	■										■					
1	1	1	1											■					

- The character patterns are standard OKI character patterns.
- Each character consists of two chips.
- Character data is generated at high level, and background data is generated at low level.
- Character data is stored, right-justified.

(3) Address code conversions
Convert the address code as indicated below to access the character patterns with the kanji code of JIS 6226.

	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

Type of character \ code	C6226			ROM address												
	X_7	X_6	X_5	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4
Non-kanji (sections 1 ~ 15)	0	1	0	X_7	Y_7	Y_6	X_3	X_2	X_1	0	0	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 1 kanji (sections 16 ~ 31)	0	1	1	X_7	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 1 kanji (sections 32 ~ 47)	1	0	0	$\overline{X_7}$	X_5	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 2 kanji (sections 48 ~ 63)	1	0	1	X_7	X_5	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 2 kanji (sections 64 ~ 79)	1	1	0	X_7	X_5	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 2 kanji (sections 80 ~ 94)	1	1	1	X_7	Y_7	Y_6	X_3	X_2	X_1	0	0	Y_5	Y_4	Y_3	Y_2	Y_1

3-3 24 x 24 Font

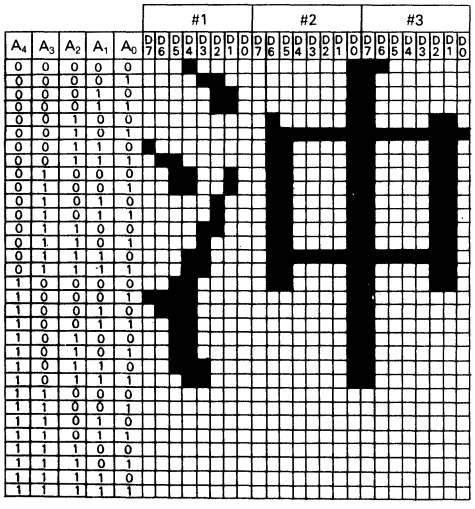
(1) Model names

MSM531000-05~07 (three codes): JIS standard No. 1 (2,965 characters) + Non-kanji (524 characters) + half-size characters (159 characters)

MSM531000-08~10 (three codes): JIS standard No. 2 (3,388 characters)

(2) Split character patterns, and their storage

• Split character patterns



- The character patterns are in accordance with the requirements of JIS C6234.
- Each character consists of three chips.
- Character data is generated at high level, and background data is generated at low level.

	JIS standard No. 1	JIS standard No. 2
#1	MSM531000-05	MSM531000-08
#2	MSM531000-06	MSM531000-09
#3	MSM531000-07	MSM531000-10

(3) Address code conversions

Convert the address code as indicated below to access character patterns with the kanji codes JIS6226 and JIS6220.

	Byte 1								Byte 2							
C6226	X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	Y_8	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1

C6220	Z_8	Z_7	Z_6	Z_5	Z_4	Z_3	Z_2	Z_1

Type of character \ code	C6226			ROM address											
	X_7	X_6	X_5	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5
Non-kanji (sections 1 ~ 15)	0	1	0	Y_7	Y_6	X_3	X_2	X_1	0	0	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 1 kanji (sections 16 ~ 31)	0	1	1	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 1 kanji (sections 32 ~ 47)	1	0	0	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 2 kanji (sections 48 ~ 63)	1	0	1	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 2 kanji (sections 64 ~ 79)	1	1	0	$\overline{X_5}$	X_4	X_3	X_2	X_1	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1
JIS standard No. 2 kanji (sections 80 ~ 94)	1	1	1	Y_7	Y_6	X_3	X_2	X_1	0	0	Y_5	Y_4	Y_3	Y_2	Y_1
Half size character	—	—	—	0	0	Z_8	Z_7	Z_6	0	0	Z_5	Z_4	Z_3	Z_2	Z_1

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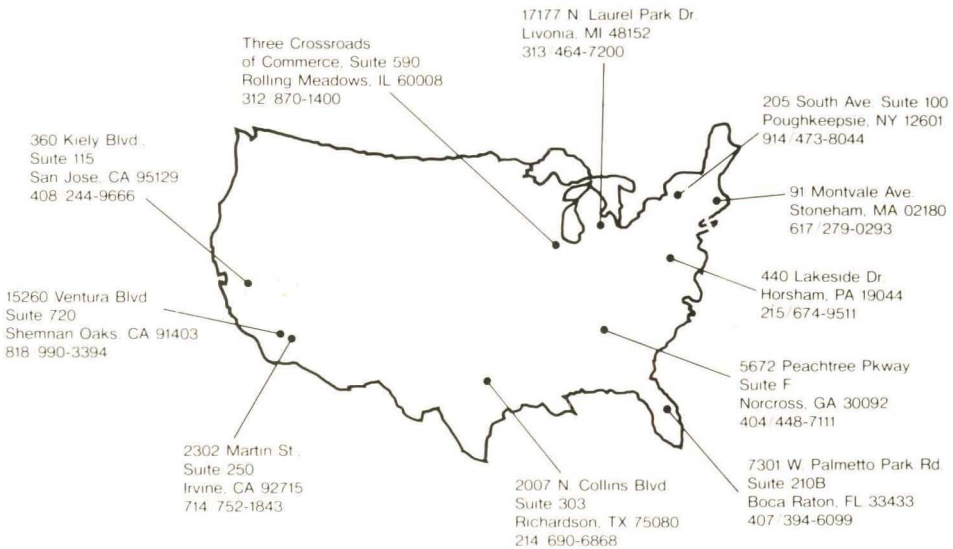

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